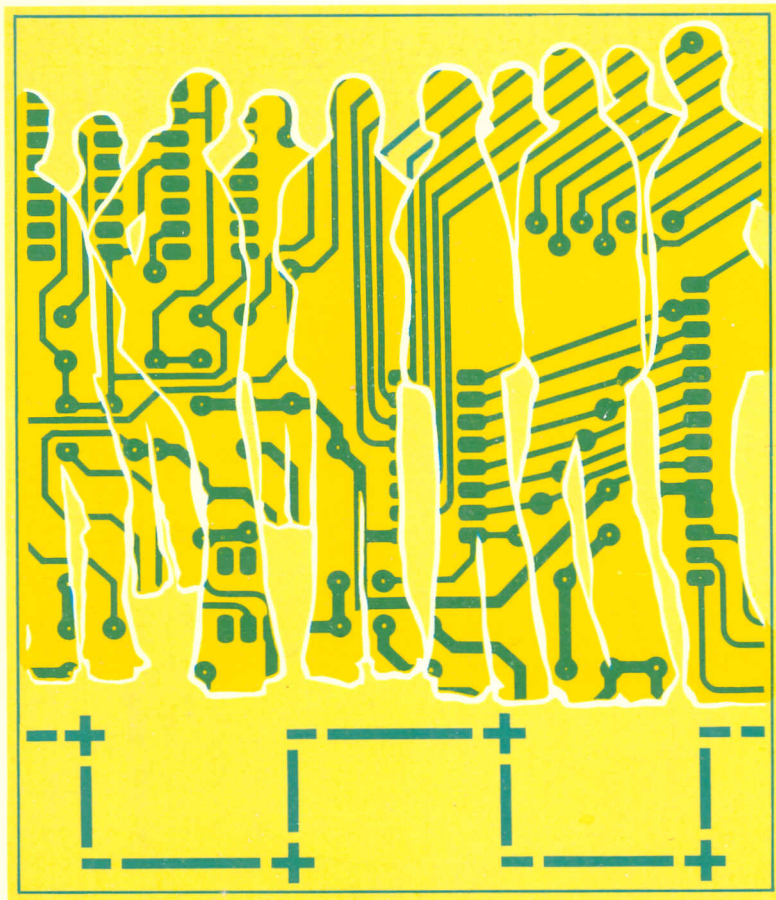


INTEGRATED CIRCUITS

81-82




EUROPEAN
HOME ELECTRONICS
DATA BOOK



MOTOROLA Semiconductors

INDRODUCTION — CONTENTS

 quantum electronics
Box 391262
Bramley,
2018

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EUROPEAN HOME ELECTRONICS DATA BOOK

INTEGRATED CIRCUITS

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Since the publication of the Motorola European Consumer Selection in 1977, the influence of electronics on the consumer has become more comprehensive and pervasive than anyone could have believed possible at that time.

Thus, for the sake of clarity, a certain amount of re-arrangement has been found desirable. Re-named European Home Electronics Data Book, the 1981 edition encompasses all those applications found within the home: entertainment, appliances, tools, toys, etc.

To facilitate access whilst maintaining as large a selection as possible, the European Home Electronics Data Book is published in two volumes:

- DISCRETE DEVICES
- INTEGRATED CIRCUITS

This volume covers integrated circuits and distinguishes between standard integrated circuits and integrated circuits dedicated to TV, radio or appliance applications. A section on microcomputers has been included in recognition of the increasing importance of these devices in home electronics.

An alpha-numeric index in Section 1 lists all devices recommended for use in home electronics whilst a synoptic table precedes each product section to aid in locating devices required.

The increasing number of new devices facing the designer makes the task of selection extremely difficult and time-consuming. We believe the arrangement of the Motorola Home Electronics Data Book will help to alleviate this problem.

Naturally, the devices listed in this Data Book represent only a small part of the Motorola product range and in the event that you are unable to find the device to suit your particular application, please consult the comprehensive Motorola Data Library or your nearest Motorola Sales Office. A list of Motorola Sales Offices and Franchised Distributors is to be found in the final section of this volume.

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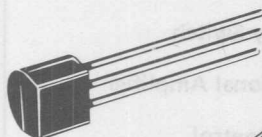
STANDARD INTEGRATED CIRCUITS

- Devices for general consumer applications
- Fixed voltage regulators

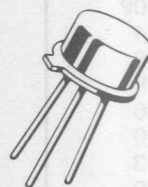
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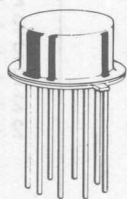
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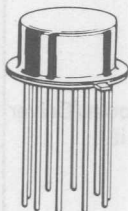
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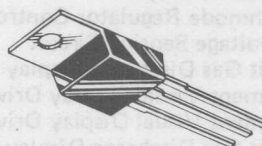
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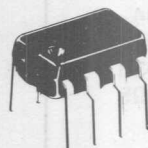
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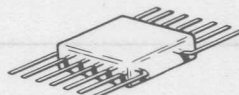
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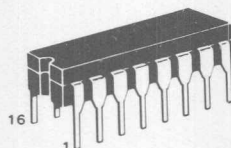
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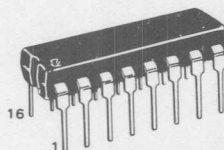
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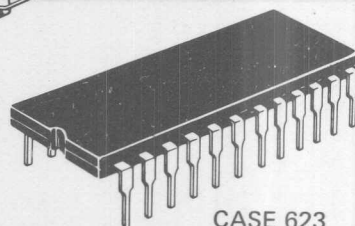
CASE 607



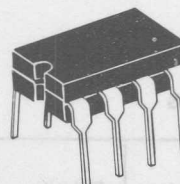
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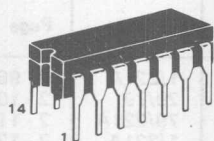
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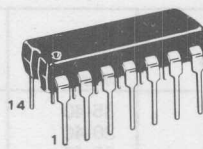
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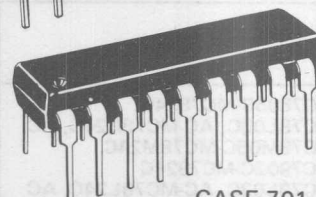
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CASE 648



CASE 701

DEVICES FOR GENERAL APPLICATIONS

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LM2903	Quad Comparator	626	2 - 7
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MC1412	Peripheral Driver Array	620/648	2 - 13
MC1413	Peripheral Driver Array	620/648	2 - 13
MC1416	Peripheral Driver Array	620/648	2 - 13
MC1417	Peripheral Driver Array	646	2 - 17
MC1445	Wideband Amplifier	603/607/632	2 - 22
MC3301	Quad Operational Amplifier	632/646	2 - 28
MC3302	Quad Comparator	632/646	2 - 36
MC3310P	Wideband Amplifier	626	2 - 40
MC3344	Programmable Frequency Switch	632/646	2 - 44
MC3346	Transistor Array	646	2 - 49
MC3358	Dual Low Power Operational Amplifier	601/626/693	2 - 52
MC3386	Transistor Array	646	2 - 49
MC3420	Switchmode Regulator Control	620/648	2 - 58
MC3423	Overvoltage Sensing Circuit	626/693	2 - 77
MC3490	7-Digit Gas Discharge Display Driver	648	2 - 83
MC3491	8-Segment Visual Display Driver	701	2 - 89
MC3492	8-Segment Visual Display Driver	701	2 - 89
MC3494	7-Digit Gas Discharge Display Driver	648	2 - 83
MC14066B	Quad Analog Switch	632/646	2 - 138
MC14433	Dual Ramp A/D Converter	623/709	2 - 142
MC14495	CMOS BCD-to-7-Segment Latch/Decoder/Driver	620/648	2 - 155
TL494	Switchmode Regulator Control Circuit	620/648	2 - 158

Fixed voltage Regulators

Device	Polarity	V _O Nom V	V _{IN} V Max.	I _O Max. mA	Package	Page
MC7805C-MC7824C	Positive	5-24	35-40	1500	1/221 A	2 - 96
MC78L05C, AC-MC78L24C, AC	Positive	5-24	30-40	100	29/79	2 - 108
MC78M05C-MC78M24C	Positive	5-24	35-40	750	79/221 A	2 - 115
MC7902C-MC7924C	Negative	2-24	35-40	1500	1/221 A	2 - 123
MC79L03C, AC-MC79L24C, AC	Negative	3-24	35-40	100	29/79	2 - 132

LM2901N

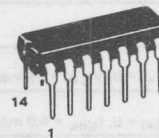
QUAD SINGLE-SUPPLY COMPARATOR

This comparator is designed for use in level detection and low-level sensing applications in Consumer, Automotive and Industrial electronic applications.

- Power Supply Options –
Single Supply = 2.0 to 36 Vdc
Split Supplies = ± 1.0 to ± 18 Vdc
- Wide Operating Temperature Range – -40 to $+85^{\circ}\text{C}$
- Low Supply Current Drain – 2.0 mA (Max)
- Low Input Biasing Current – 25 nA (Typ)
- Low Input Offset Voltage – 2.0 mV (Max)
- TTL and CMOS Compatible

QUAD COMPARATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



N SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or +18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Output Sink Current	I_{sink}	20	mA
Power Dissipation @ $T_A = 25^{\circ}\text{C}$	P_D		
Plastic Package		1.25	Watts
Derate above 25°C		10	mW/ $^{\circ}\text{C}$
Operating Ambient Temperature Range	T_A	-40 to $+85$	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$	$^{\circ}\text{C}$

PIN CONNECTIONS

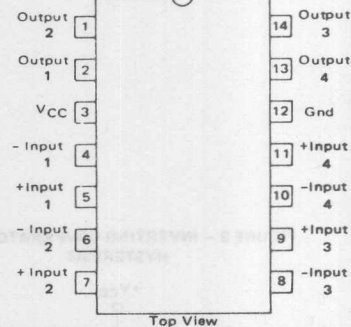
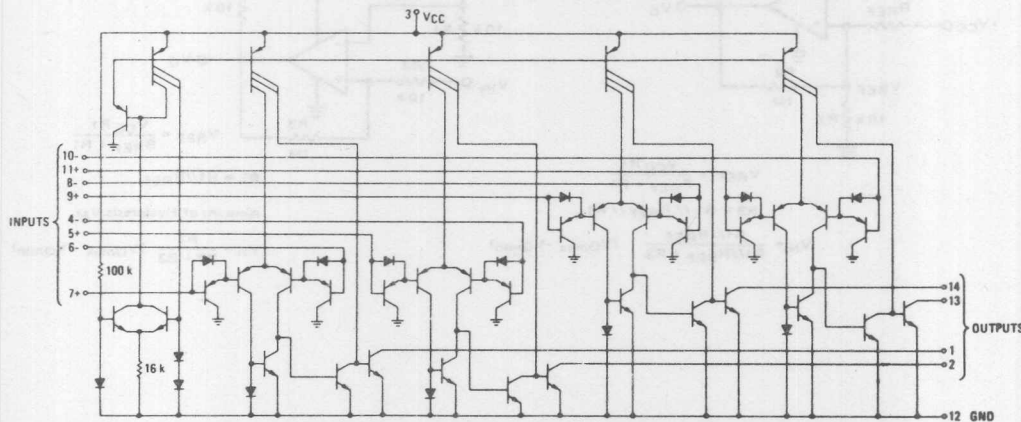


FIGURE 1 – CIRCUIT SCHEMATIC



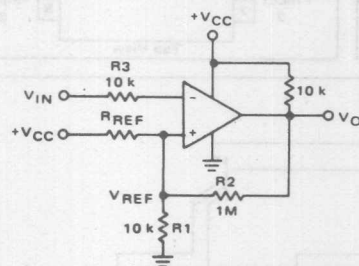
LM2901N

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($V_{ref} = 1.4$ Vdc, $V_O = 1.4$ Vdc, $R_S = 0$)	V_{IO}	—	2.0	7.0	mVdc
Input Offset Current	I_{IO}	—	± 5.0	± 50	nA
Input Bias Current	I_{IB}	—	25	250	nA
Input Common Mode Voltage Range (Note 1)	V_{ICR}	0	—	$V_{CC} - 1.5$	V
Supply Current ($R_L = \infty$)	I_{CC} I_{EE}	—	0.8	2.0	mA
Response Time (Note 2) ($V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω)	—	—	1.3	—	μs
Output Sink Current ($V_{I(-)} \geq +1.0$ Vdc, $V_{I(+)} = 0$, $V_O \leq +1.5$ Vdc)	I_{sink}	6.0	16	—	mA
Saturation Voltage ($V_{I(-)} \geq +1.0$ Vdc, $V_{I(+)} = 0$, $I_{sink} = 4.0$ mAdc)	V_{sat}	—	—	400	mV
Output Leakage Current ($V_{I(+)} \geq +1.0$ Vdc, $V_{I(-)} = 0$, $V_O = 5.0$ Vdc)	I_{OL}	—	0.1	—	μA

- Notes 1. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 300 mV. The upper end of the common-mode voltage range is $V_{CC} - 1.5$ V, but either or both inputs can go to +30 Vdc without damage.
2. The response time specified is for a 100 mV input step with 5 mV overdrive. For large signals, 300 ns is typical.

FIGURE 2 – INVERTING COMPARATOR WITH HYSTERESIS

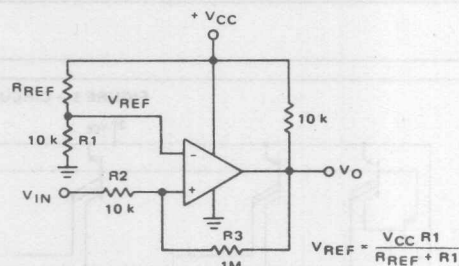


$$V_{REF} \approx \frac{V_{CC} R_1}{R_{REF} + R_1}$$

$$R_3 \approx R_1 \parallel R_{REF} \parallel R_1$$

$$V_H = \frac{R_1 / R_{REF}}{R_1 / R_{REF} + R_2} (V_{Omax} - V_{Omin})$$

FIGURE 3 – NON-INVERTING COMPARATOR WITH HYSTERESIS



$$V_{REF} = \frac{V_{CC} R_1}{R_{REF} + R_1}$$

$$R_2 \approx R_1 \parallel R_{REF}$$

Amount of Hysteresis V_H

$$V_H = \frac{R_2}{R_2 + R_3} (V_{Omax} - V_{Omin})$$

TYPICAL CHARACTERISTICS
($V_{CC} = +15$ Vdc, $T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 4 – NORMALIZED INPUT OFFSET VOLTAGE

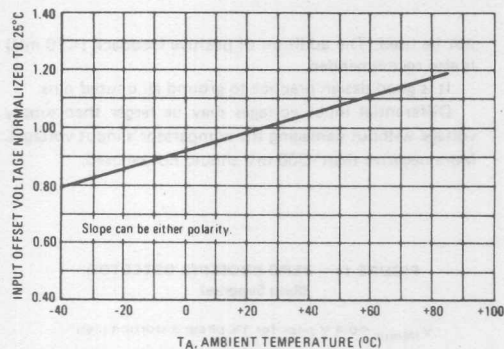


FIGURE 5 – INPUT BIAS CURRENT

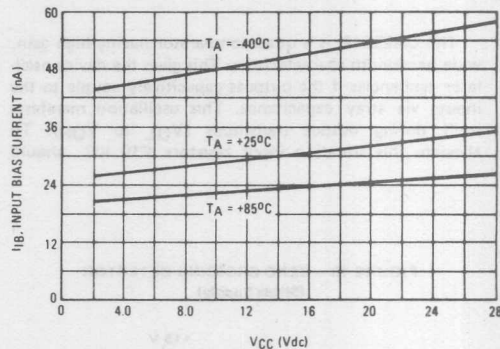


FIGURE 6 – NORMALIZED OFFSET CURRENT

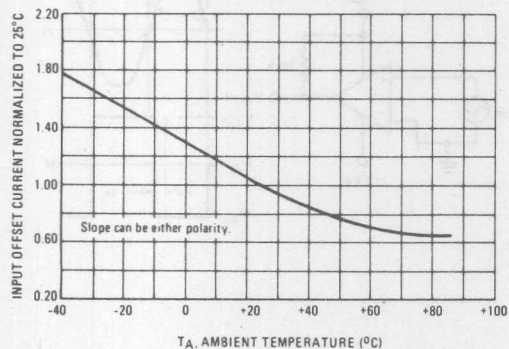


FIGURE 7 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE

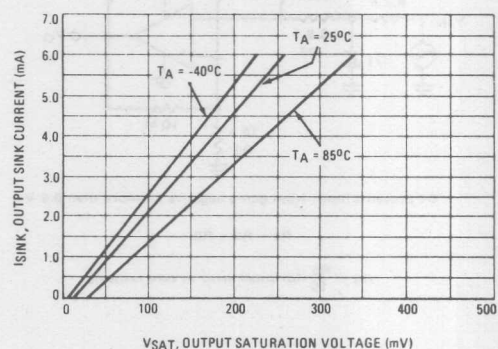
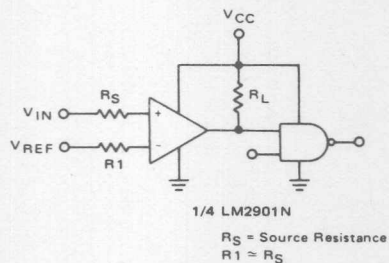
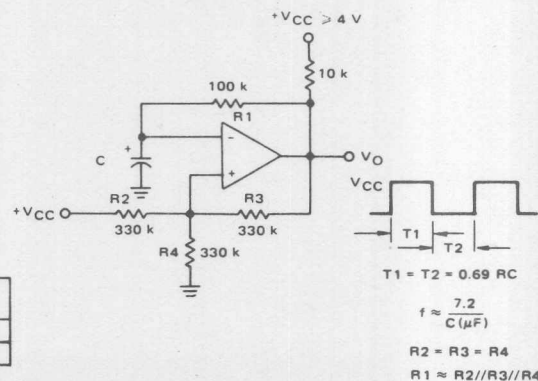


FIGURE 8 – DRIVING LOGIC



LOGIC	DEVICE	V_{CC} Volts	R_L k Ω
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5	10

FIGURE 9 – SQUAREWAVE OSCILLATOR



APPLICATIONS INFORMATION

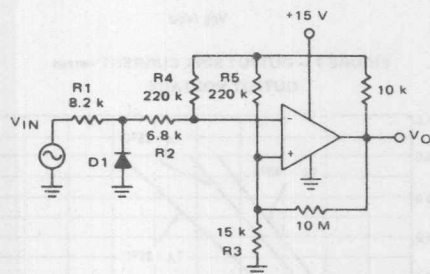
The LM2901N is a quad comparator having high gain, wide bandwidth characteristics. This gives the device oscillator tendencies if the outputs capacitively couple to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors $<10\text{ k}\Omega$ should

not be used. The addition of positive feedback ($<10\text{ mV}$) is also recommended.

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than -300 mV should not be used.

FIGURE 10 — ZERO CROSSING DETECTOR
(Single Supply)



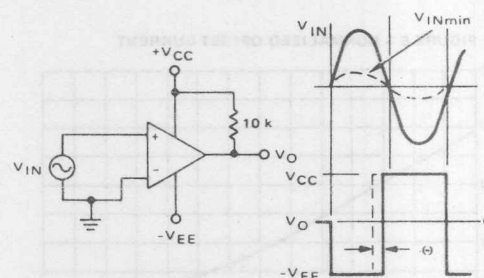
D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing}$$

FIGURE 11 — ZERO CROSSING DETECTOR
(Split Supplies)

$V_{INmin} \approx 0.4\text{ V}$ peak for 1% phase distortion ($\approx \theta$).



**LM193 LM193A
LM293 LM293A
LM393 LM393A
LM2903**

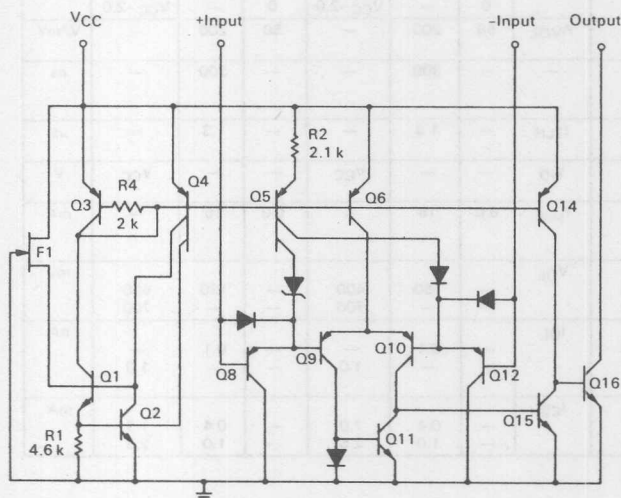
Advance Information

SINGLE-SUPPLY, LOW-POWER, LOW-OFFSET-VOLTAGE DUAL COMPARATORS

The LM193 series are dual independent precision voltage comparators capable of single- or split-supply operation. These devices are designed to permit a common mode range-to-ground level with single-supply operation. Input offset-voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer automotive, and industrial electronics.

- Wide Single-Supply Range — 2.0 Vdc to 36 Vdc
- Split-Supply Range — ± 1.0 Vdc to ± 18 Vdc
- Very Low Current Drain Independent of Supply-Voltage — 0.4 mA
- Low Input Bias Current — 25 nA
- Low Input Offset Current — 5.0 nA
- Low Input Offset Voltage — 2.0 mV (max) LM193A/293A/393A
— 5.0 mV (max) LM193/293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS and CMOS Logic Levels

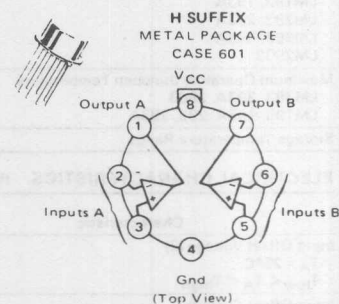
FIGURE 1 — CIRCUIT SCHEMATIC
(Diagram shown is for 1 comparator)



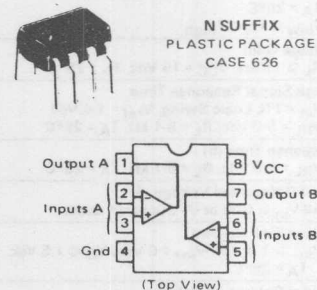
This is advance information and specifications are subject to change without notice.

DUAL COMPARATORS

SILICON MONOLITHIC
INTEGRATED CIRCUIT



2



ORDERING INFORMATION

Device	Temperature Range	Package
LM193AH,H	-55 to +125°C	Metal Can
LM293AH,H	-25 to +85°C	Metal Can
LM393AH,H	0 to +70°C	Metal Can
LM393AN,N	0 to +70°C	Plastic Mini DIP
LM2903N	-40 to +85°C	Plastic Mini DIP

LM193, LM193A, LM293, LM293A, LM393, LM393A, LM2903

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ± 18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Input Current (1) ($V_{in} < -0.3$ Vdc)	I_{in}	50	mA
Output Short Circuit-to-Ground Output Sink Current	I_{SC} I_{sink}	Continuous 20	mA
Power Dissipation @ $T_A = 25^\circ\text{C}$ Molded DIP Derate above 25°C Metal Can Derate above 25°C	P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JA}$	570 5.7 830 6.64	mW mW/ $^\circ\text{C}$ mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range LM193, 193A LM293, 293A LM393, 393A LM2903	T_A	-55 to +125 -25 to +85 0 to +70 -40 to +85	$^\circ\text{C}$
Maximum Operating Junction Temperature LM393, 393A, 2903 LM193, 193A, 293, 293A	$T_{J(max)}$	125 150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ Vdc; $*T_{low} \leq T_A \leq T_{high}$ unless otherwise stated.)

Characteristic	Symbol	LM193A			LM293A, LM393A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (2) $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	V_{IO}	—	± 1.0	± 2.0 4.0	—	± 1.0	± 2.0 4.0	mV
Input Offset Current $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{IO}	—	± 3.0	± 25 ± 100	—	± 5.0	± 50 ± 150	nA
Input Bias Current (3) $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{IB}	—	25	100 300	—	25	250 400	nA
Input Common Mode Voltage Range (4) $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	V_{ICR}	0 0	—	$V_{CC} - 1.5$ $V_{CC} - 2.0$	0 0	—	$V_{CC} - 1.5$ $V_{CC} - 2.0$	Volts
Voltage Gain $R_L \geq 15$ k Ω , $V_{CC} = 15$ Vdc, $T_A = 25^\circ\text{C}$	A_{VOL}	50	200	—	50	200	—	V/mV
Large Signal Response Time $V_{in} = \text{TTL Logic Swing}$, $V_{ref} = 1.4$ Vdc $V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$	—	—	300	—	—	300	—	ns
Response Time (5) $V_{RL} = 5.0$ Vdc, $R_L = 5.1$ k Ω , $T_A = 25^\circ\text{C}$	t_{TLH}	—	1.3	—	—	1.3	—	μs
Input Differential Voltage (6) All $V_{in} \geq \text{Gnd}$ or V_- Supply (if used)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	V
Output Sink Current $V_{in-} \geq 1.0$ Vdc, $V_{in+} = 0$ Vdc, $V_O \leq 1.5$ Vdc $T_A = 25^\circ\text{C}$	I_{sink}	6.0	16	—	6.0	16	—	mA
Output Saturation Voltage $V_{in-} \geq 1.0$ Vdc, $V_{in+} = 0$, $I_{sink} \leq 4.0$ mA, $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	V_{OL}	— —	150 —	400 700	— —	150 —	400 700	mV
Output Leakage Current $V_{in-} = 0$ V, $V_{in+} \geq 1.0$ Vdc, $V_O = 5.0$ Vdc, $T_A = 25^\circ\text{C}$ $V_{in-} = 0$ V, $V_{in+} \geq 1.0$ Vdc, $V_O = 30$ Vdc, $T_{low} \leq T_A \leq T_{high}$	I_{OL}	— —	0.1 —	— 1.0	— —	0.1 —	— 1.0	nA
Supply Current $R_L = \infty$ Both Comparators, $T_A = 25^\circ\text{C}$ $R_L = \infty$ Both Comparators, $V_{CC} = 30$ V	I_{CC}	— —	0.4 1.0	1.0 2.5	— —	0.4 1.0	1.0 2.5	mA

*LM193/193A — $T_{low} = -55^\circ\text{C}$, $T_{high} = +125^\circ\text{C}$
 LM293/293A — $T_{low} = -25^\circ\text{C}$, $T_{high} = +85^\circ\text{C}$
 LM393/393A — $T_{low} = 0^\circ\text{C}$, $T_{high} = +70^\circ\text{C}$
 LM2903 — $T_{low} = -40^\circ\text{C}$, $T_{high} = +85^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ Vdc}$; $T_{low} \leq T_A \leq T_{high}$ unless otherwise stated.)

Characteristic	Symbol	LM193			LM293, LM393			LM2903			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (2) $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	V_{IO}	—	± 1.0	± 5.0 9.0	—	± 1.0	± 5.0 9.0	—	± 2.0 9.0	± 7.0 15	mV
Input Offset Current $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{IO}	—	± 3.0	± 25 ± 100	—	± 5.0	± 50 ± 150	—	± 5.0 ± 50	± 50 ± 200	nA
Input Bias Current (3) $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	I_{IB}	—	25	100 300	—	25	250 400	—	25 200	250 500	nA
Input Common Mode Voltage Range (4) $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	V_{ICR}	0 0	—	$V_{CC} - 1.5$ $V_{CC} - 2.0$	0 0	—	$V_{CC} - 1.5$ $V_{CC} - 2.0$	0 0	—	$V_{CC} - 1.5$ $V_{CC} - 2.0$	Volts
Voltage Gain $R_L \geq 15 \text{ k}\Omega$, $V_{CC} = 15 \text{ Vdc}$, $T_A = 25^\circ\text{C}$	A_{VOL}	50	200	—	50	200	—	25	200	—	V/mV
Large Signal Response Time $V_{in} = \text{TTL Logic Swing}$, $V_{ref} = 1.4 \text{ Vdc}$ $V_{RL} = 5.0 \text{ Vdc}$, $R_L = 5.1 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$	—	—	300	—	—	300	—	—	300	—	ns
Response Time (5) $V_{RL} = 5.0 \text{ Vdc}$, $R_L = 5.1 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$	t_{TLH}	—	1.3	—	—	1.3	—	—	1.5	—	μs
Input Differential Voltage (6) All $V_{in} \geq G_{nd}$ or V_{-} Supply (if used)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	V
Output Sink Current $V_{in-} \geq 1.0 \text{ Vdc}$, $V_{in+} = 0 \text{ Vdc}$, $V_O \leq 1.5 \text{ Vdc}$, $T_A = 25^\circ\text{C}$	I_{sink}	6.0	16	—	6.0	16	—	6.0	16	—	mA
Output Saturation Voltage $V_{in-} \geq 1.0 \text{ Vdc}$, $V_{in+} = 0$, $I_{sink} \leq 4.0 \text{ mA}$, $T_A = 25^\circ\text{C}$ $T_{low} \leq T_A \leq T_{high}$	V_{OL}	—	150	400	—	150	400	—	—	400	mV
Output Leakage Current $V_{in-} = 0 \text{ V}$, $V_{in+} \geq 1.0 \text{ Vdc}$, $V_O = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$ $V_{in-} = 0 \text{ V}$, $V_{in+} \geq 1.0 \text{ Vdc}$, $V_O = 30 \text{ Vdc}$, $T_{low} \leq T_A \leq T_{high}$	I_{OL}	—	0.1	—	—	0.1	—	—	0.1	—	nA
Supply Current $R_L = \infty$ Both Comparators, $T_A = 25^\circ\text{C}$ $R_L = \infty$ Both Comparators, $V_{CC} = 30 \text{ V}$	I_{CC}	—	0.4	1.0	—	0.4	1.0	—	0.4	1.0	mA

*LM193/193A — $T_{low} = -55^\circ\text{C}$, $T_{high} = +125^\circ\text{C}$

LM293/293A — $T_{low} = -25^\circ\text{C}$, $T_{high} = +85^\circ\text{C}$

LM393/393A — $T_{low} = 0^\circ\text{C}$, $T_{high} = +70^\circ\text{C}$

NOTES:

- (1) This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector-base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomena can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become $> -0.3 \text{ V}$ of ground or negative supply.
- (2) At output switch point, $V_O \approx 1.4 \text{ Vdc}$, $R_s = 0 \Omega$ with V_{CC} from 5.0 Vdc to 30 Vdc , and over the full input common-mode range (0 volts to $V_{CC} - 1.5$ volts)
- (3) Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
- (4) Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is $V_{CC} - 1.5 \text{ V}$, but either or both inputs can be taken to as high as 30 volts without damage.
- (5) Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive, faster response times are obtainable.
- (6) The comparator will exhibit proper output state, if one of the inputs become greater than V_{CC} , the other input must remain within the common mode range. The low input state must not be less than -0.3 volts of ground or minus supply.
- (7) If input signals exceed V_{CC} , only the overdriven comparator is affected.
- (8) Overdriven inputs should be limited to 25 V when using a 5.0 V supply. Input current limiting resistors should be used when inputs are likely to exceed supply positive supply voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

LM193,A/293,A/393,A

FIGURE 2 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

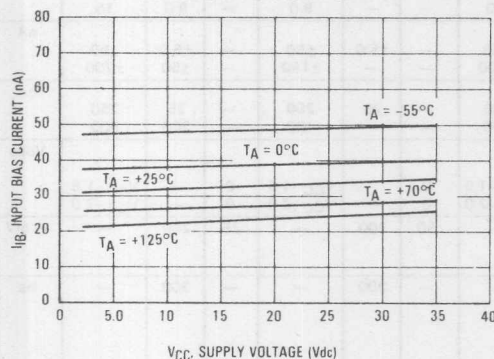


FIGURE 3 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

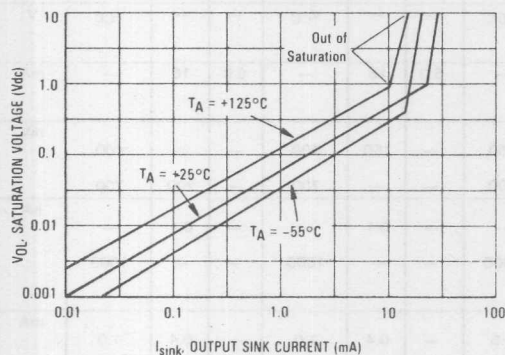
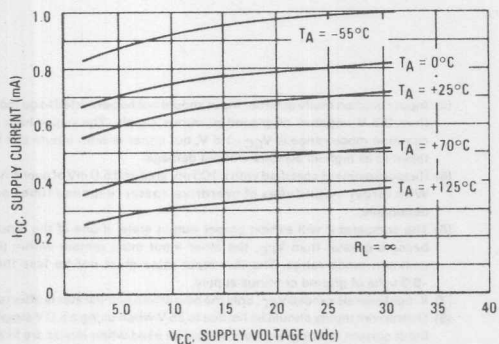


FIGURE 4 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE



LM2903

FIGURE 5 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

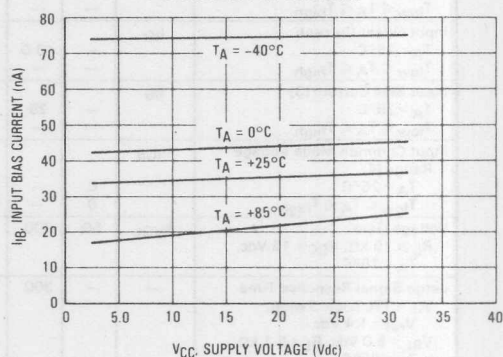


FIGURE 6 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

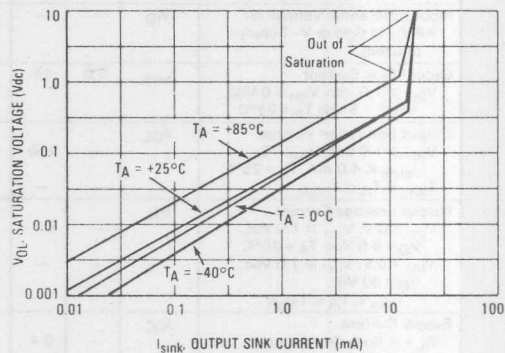
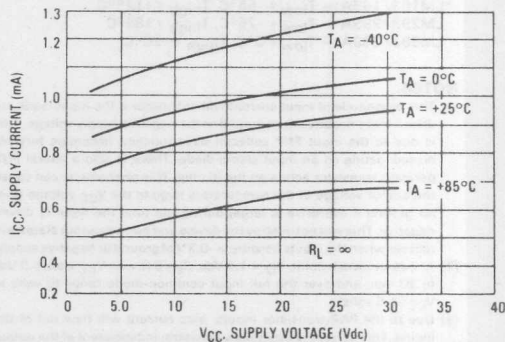


FIGURE 7 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE



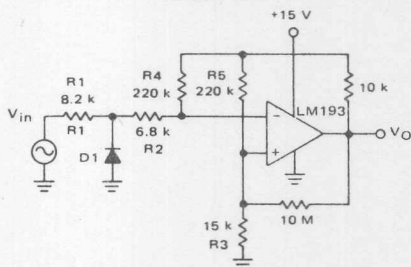
APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors $< 10\text{ k}\Omega$ should be used. The

addition of positive feedback ($< 10\text{ mV}$) is also recommended.

It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than -0.3 V should not be used.

FIGURE 8 — ZERO CROSSING DETECTOR
(Single Supply)



D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing}$$

FIGURE 9 — ZERO CROSSING DETECTOR
(Split Supplies)

$$V_{INmin} \approx 0.4\text{ V peak for } 1\% \text{ phase distortion } (-49)$$

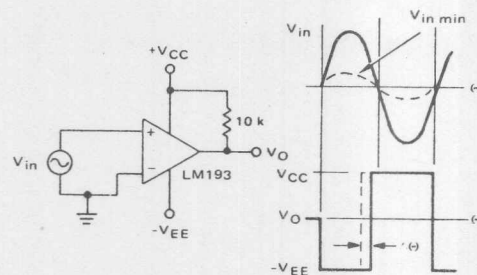


FIGURE 10 — FREE-RUNNING SQUARE-WAVE OSCILLATOR

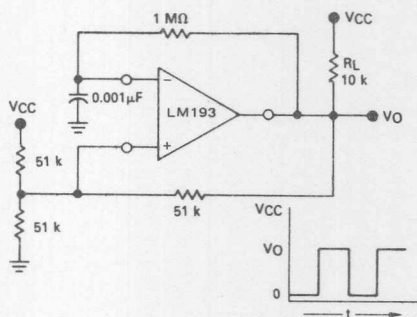
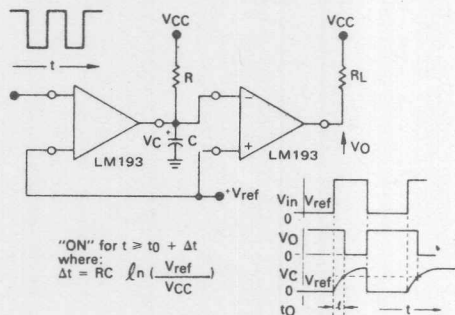


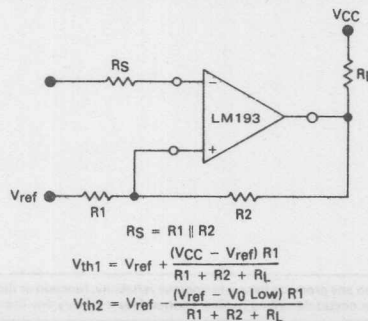
FIGURE 11 — TIME DELAY GENERATOR



$$\text{"ON" for } t \geq t_0 + \Delta t$$

$$\text{where: } \Delta t = RC \ln \left(\frac{V_{ref}}{V_{CC}} \right)$$

FIGURE 12 — COMPARATOR WITH HYSTERESIS



$$R_S = R1 \parallel R2$$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref}) R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{OL}) R1}{R1 + R2 + R_L}$$

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_D(T_A) = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)}$$

Where: $P_D(T_A)$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than

the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

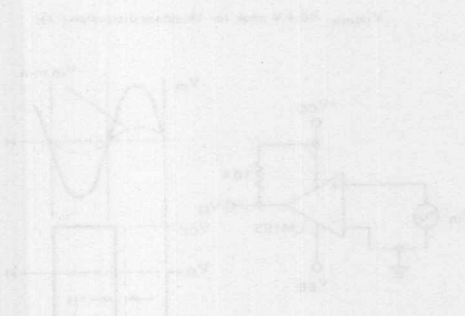
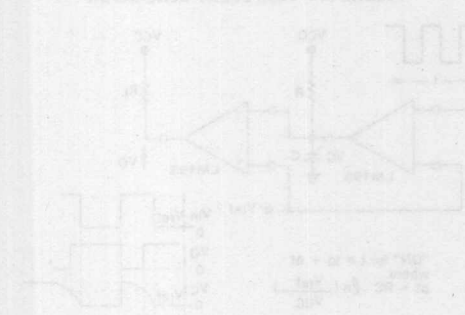


FIGURE 11 — TWO DELAY GENERATOR



$10 - 0.1 \mu s$
 $1 \mu s$
 $10 \mu s$
 $100 \mu s$
 $1 ms$
 $10 ms$
 $100 ms$
 $1 s$

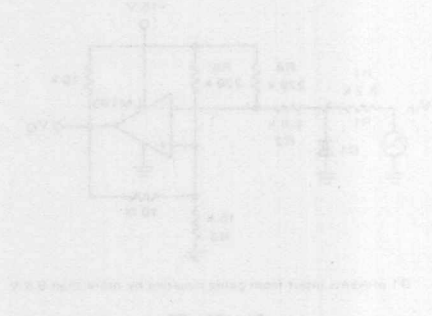


FIGURE 13 — PRECISION SQUARE-WAVE OSCILLATOR

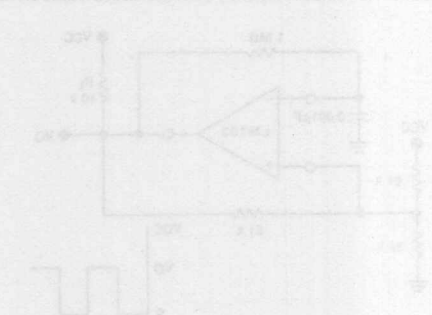
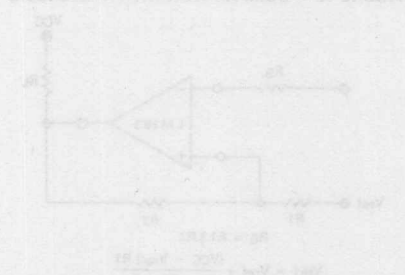


FIGURE 14 — PRECISION SQUARE-WAVE OSCILLATOR



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HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The seven NPN Darlington-connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high break-down voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 600 mA permit them to drive incandescent lamps.

The MC1411 device is a general-purpose array for use with DTL, TTL, PMOS, or CMOS Logic. The MC1412 contains a zener diode and resistor in series with the input to limit input current for use with 14 to 25 Volt PMOS Logic. The MC1413 with a 2.7 k Ω series input resistor is well suited for systems utilizing 5 Volt TTL or CMOS Logic. The MC1416 uses a series 10.5 k Ω resistor and is useful in 8–18 Volt MOS systems.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50*	V
Input Voltage (Except MC1411)	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$
Junction Temperature	T_J	150	$^\circ\text{C}$

Maximum Package Power Dissipation (See Thermal Information Section)

*Higher voltage selection available. See your local representative.

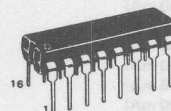
DEVICE CROSS-REFERENCE LISTING

9665 – SN75476 – ULN2001A – order MC1411P
 9666 – SN75477 – ULN2002A – order MC1412P
 9667 – SN75478 – ULN2003A – order MC1413P
 9668 – – ULN2004A – order MC1416P

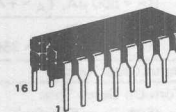
MC1412 (ULN2002A)
MC1413 (ULN2003A)
MC1416 (ULN2004A)

PERIPHERAL DRIVER ARRAYS

SILICON MONOLITHIC INTEGRATED CIRCUITS

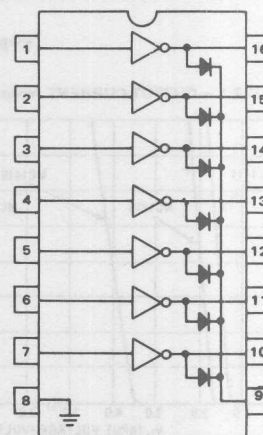


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



MC1411, MC1412, MC1413, MC1416

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Leakage Current *($V_O = 50\text{ V}$, $T_A = +70^\circ\text{C}$) *($V_O = 50\text{ V}$, $T_A = +25^\circ\text{C}$) *($V_O = 50\text{ V}$, $T_A = +70^\circ\text{C}$, $V_I = 6.0\text{ V}$) *($V_O = 50\text{ V}$, $T_A = +70^\circ\text{C}$, $V_I = 1.0\text{ V}$)	I_{CEX}	— — — —	— — — —	100 50 500 500	μA
Collector-Emitter Saturation Voltage ($I_C = 350\text{ mA}$, $I_B = 500\text{ }\mu\text{A}$) ($I_C = 200\text{ mA}$, $I_B = 350\text{ }\mu\text{A}$) ($I_C = 100\text{ mA}$, $I_B = 250\text{ }\mu\text{A}$)	$V_{CE(sat)}$	— — —	1.1 0.95 0.85	1.8 1.3 1.1	V
Input Current — On-Condition ($V_I = 17\text{ V}$) ($V_I = 3.85\text{ V}$) ($V_I = 5.0\text{ V}$) ($V_I = 12\text{ V}$)	$I_{I(on)}$	— — — —	0.85 0.93 0.35 1.0	1.3 1.35 0.5 1.45	mA
Input Voltage — On Condition ($V_{CE} = 2.0\text{ V}$, $I_C = 300\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 200\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 250\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 300\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 125\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 200\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 275\text{ mA}$) ($V_{CE} = 2.0\text{ V}$, $I_C = 350\text{ mA}$)	$V_{I(on)}$	— — — — — — — —	— — — — — — — —	13 2.4 2.7 3.0 5.0 6.0 7.0 8.0	V
Input Current — Off Condition ($I_C = 500\text{ }\mu\text{A}$, $T_A = +70^\circ\text{C}$)	$I_{I(off)}$	50	100	—	μA
DC Current Gain ($V_{CE} = 2.0\text{ V}$, $I_C = 350\text{ mA}$)	h_{FE}	1000	—	—	—
Input Capacitance	C_i	—	15	30	pF
Turn-On Delay Time (50% E_I to 50% E_O)	t_{on}	—	0.25	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)	t_{off}	—	0.25	1.0	μs
Clamp Diode Leakage Current ($V_R = 50\text{ V}$)	I_R	—	—	50 100	μA
Clamp Diode Forward Voltage ($I_F = 350\text{ mA}$)	V_F	—	1.5	2.0	V

*Higher voltage selections available, contact your local representative.

TYPICAL PERFORMANCE CURVES — $T_A = 25^\circ\text{C}$

FIGURE 1 — OUTPUT CURRENT versus INPUT VOLTAGE

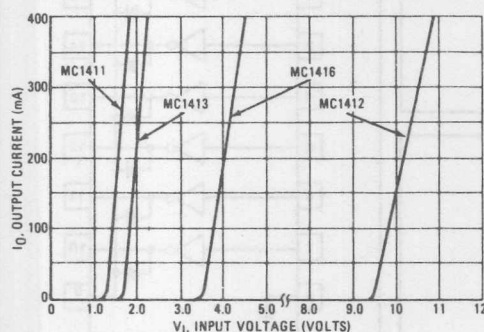
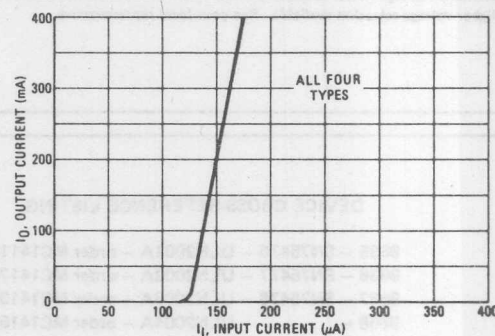


FIGURE 2 — OUTPUT CURRENT versus INPUT CURRENT



MC1411, MC1412, MC1413, MC1416

TYPICAL CHARACTERISTIC CURVES — $T_A = 25^\circ\text{C}$ (continued)

FIGURE 3 — TYPICAL OUTPUT CHARACTERISTICS

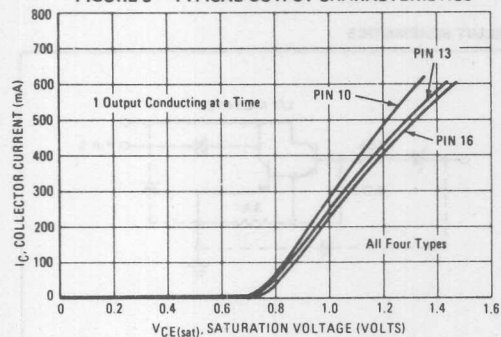


FIGURE 4 — INPUT CHARACTERISTICS — MC1412

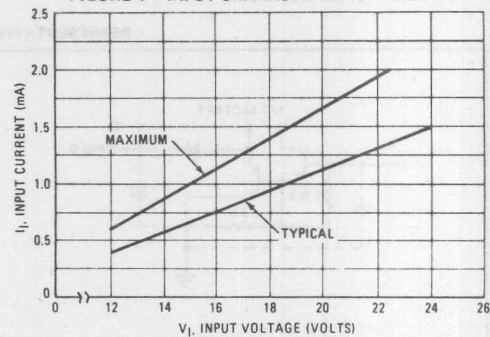


FIGURE 5 — INPUT CHARACTERISTICS — MC1413

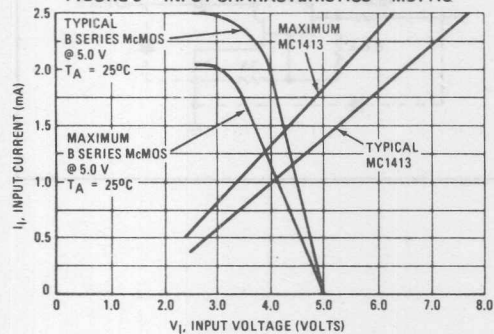


FIGURE 6 — INPUT CHARACTERISTICS — MC1416

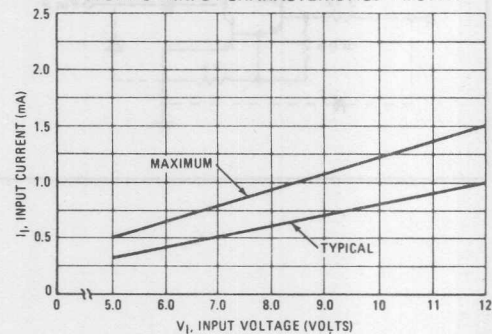
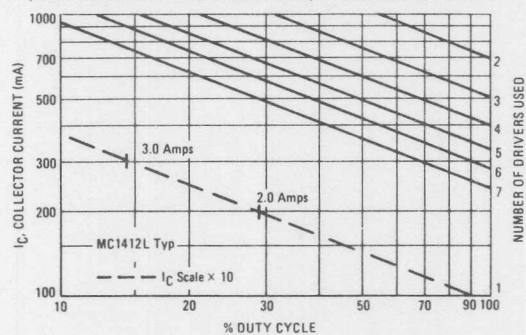
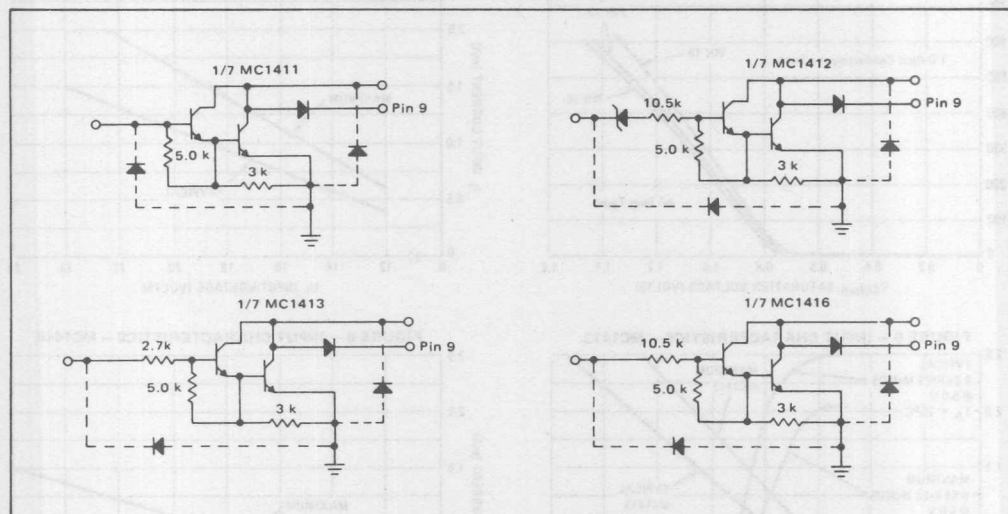


FIGURE 7 — MAXIMUM COLLECTOR CURRENT
versus DUTY CYCLE
(AND NUMBER OF DRIVERS IN USE) — CERAMIC or PLASTIC



MC1411, MC1412, MC1413, MC1416

REPRESENTATIVE CIRCUIT SCHEMATICS



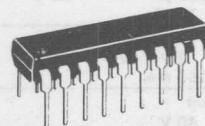
MC1417

ADVANCE INFORMATION

HIGH VOLTAGE—HIGH CURRENT 8 DARLINGTON TRANSISTOR ARRAYS

The eight NPN Darlington connected transistors in these arrays are intended for use as an interface between NMOS output and driving lamps, relays or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to -300 mA permit them to drive incandescent lamps. Each drive has an output stage capable of sourcing 250 mA and a input configuration allowing operation from 3.7 V to 15 V with less than 1.6 mA of input current.

PERIPHERAL DRIVER ARRAYS SILICON MONOLITHIC INTEGRATED CIRCUITS

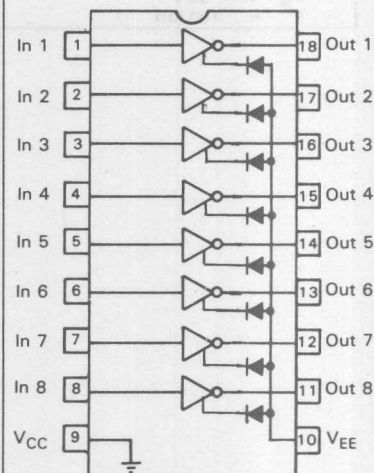


P SUFFIX
PLASTIC
PACKAGE
CASE 701-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum output voltage	V_{OUT}	-40	V
Maximum input voltage	V_{IN}	-20	V
Maximum output current	I_{OUT}	-300	mA
Maximum ground current	I_{CC}	2.4	A
Operating temp. range	T_A	0 to 85	$^{\circ}$ C
Storage temp. range	T_{STR}	-55 to $+150$	$^{\circ}$ C
Junction temperature	T_J	150	$^{\circ}$ C
Continuous power dissipation per stage at 25° C ambient	P_D	600	mW
Continuous power dissipation per package at 25° C ambient	P_D	1.8	W
Thermal resistance junction to ambient	θ_{JA}	70	$^{\circ}$ C/W
Peak dissipation for total package at 50° C ambient (input pulse 40 mS, duty cycle 20%)	P_{DPK}	4	W

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature range	Package
MC1417P	0 to 85° C	Plastic dip

MC1417

Due to the advanced nature of this specification, final electrical limits are not yet given on all parameters

ELECTRICAL CHARACTERISTICS (T_A = 25° C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Output leakage current V _{out} = - 40 V T _A = 70° C I _{in} = - 10 μA	- I _{OH}	-	-	150	μA
Output low level voltage I _{out} = - 250 mA V = - 30 V I _{in} = - 400 μA I _{out} = - 100 mA V = - 30 V I _{in} = - 300 μA	- V _{OL}	-	-	2 1.8	V
Input current - High logic state V _{in} = - 15 V V = - 30 V	- I _{IH}	-	-	1.6	mA
Input current - Low logic state I _{out} = - 500 μA V = - 40 V T _A = 70° C	- I _{IL}	50	-	-	μA
Input voltage - High logic state V _{ol} = - 2 V V = - 30 V I _{out} = - 250 mA	- V _{IH}	-	-	3.7	V
Quiescent current V _{EE} = - 40 V	- I _S	-	-	100	μA
Diode clamping voltage Figure 1	- V _F	-	-	2.9	V
Diode leakage current V _{out} = - 5 V V _{EE} = - 40 V T _A = 70° C	I _R	-	-	100	μA
Input capacitance V _{EE} = - 30 V F = 100 KHz	C _{IN}	-	-	30	pF

SWITCHING CHARACTERISTICS $V_{EE} = -30\text{ V}$ — $T_A = 25^\circ\text{ C}$

Characteristic	Symbol	Min	Typ	Max	Unit
Turn on delay	t on	—	—	5	us
Turn off delay	t off	—	—	5	us

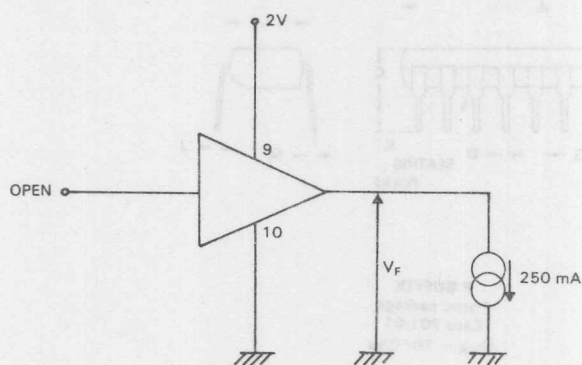
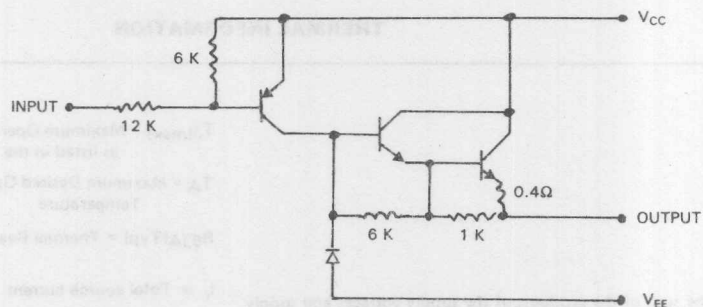
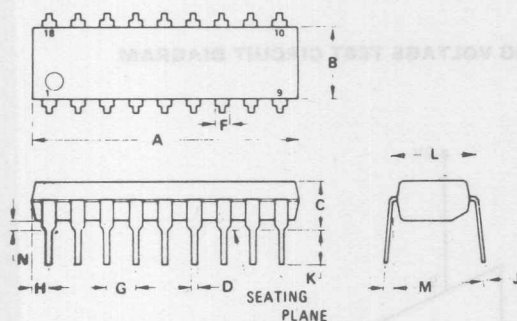
DIODE CLAMPING VOLTAGE TEST CIRCUIT DIAGRAM

FIG. 1

$\frac{1}{8}$ MC 1417

REPRESENTATIVE CIRCUIT SCHEMATIC

OUTLINE DIMENSIONS



P SUFFIX
Plastic package
Case 701-01
 $R_{\theta JA} = 70^{\circ}\text{C/W}$

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G")
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

THERMAL INFORMATION

the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(\max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(\text{Typ})$ = Thermal Resistance Junction to Ambient

I_c = Total source current

V_{ce} = Collector voltage

FIG. 2 OUTPUT CURRENT VERSUS DUTY CYCLE

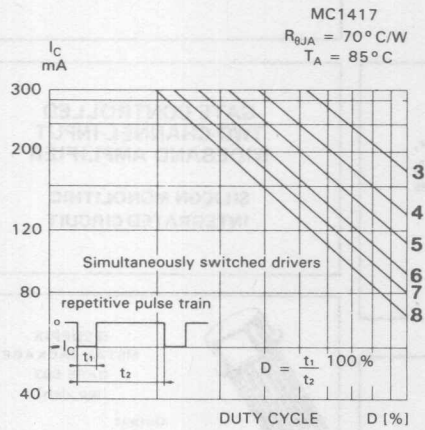


FIG. 3 TYPICAL OUTPUT CHARACTERISTICS

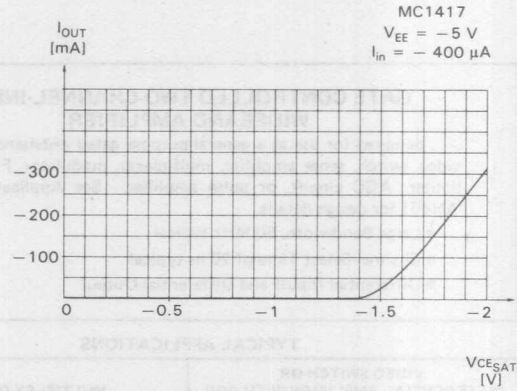


FIG. 4 OUTPUT CURRENT VERSUS INPUT VOLTAGE

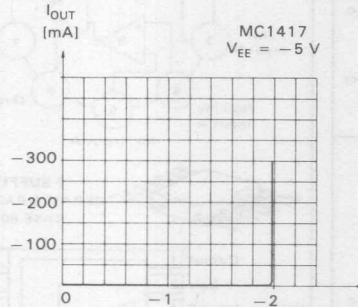


FIG. 5 INPUT CHARACTERISTICS

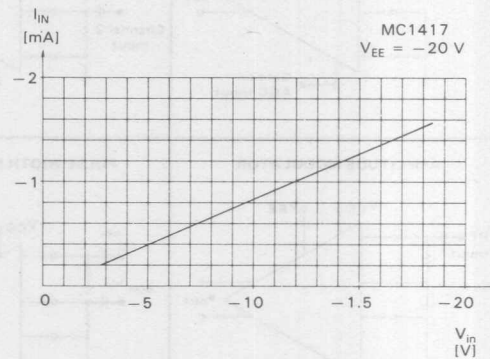
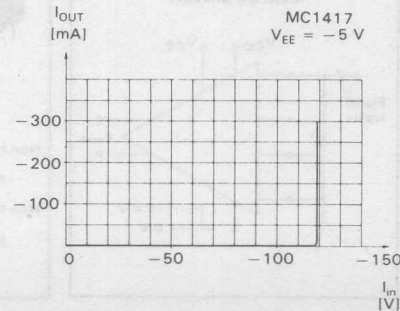


FIG. 6 OUTPUT CURRENT VERSUS INPUT CURRENT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1445F	0°C to +75°C	Ceramic Flat
MC1445G	0°C to +75°C	Metal Can
MC1445L	0°C to +75°C	Ceramic DIP
MC1545F	-55°C to +125°C	Ceramic Flat
MC1545G	-55°C to +125°C	Metal Can
MC1545L	-55°C to +125°C	Ceramic DIP

MC1445
MC1545

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

... designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN491 for design details.

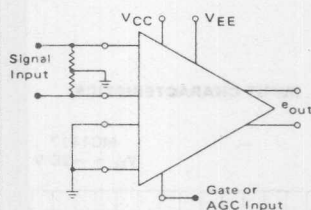
- Large Bandwidth; 50 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

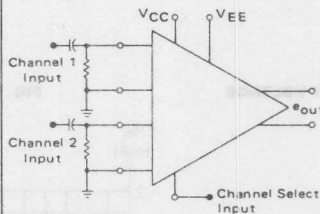
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

TYPICAL APPLICATIONS

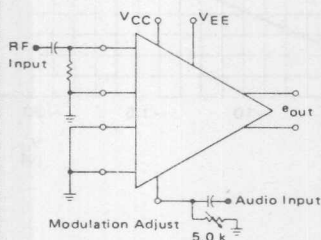
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



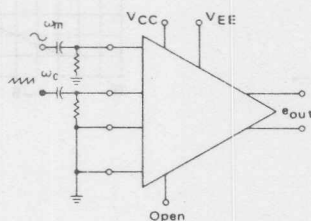
MULTIPLEX OR FSK



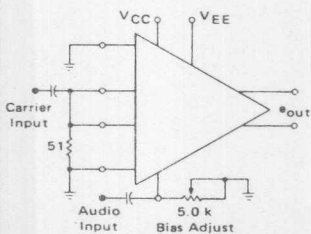
AMPLITUDE MODULATOR



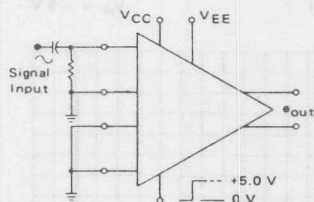
PULSE-WIDTH MODULATOR



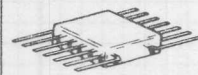
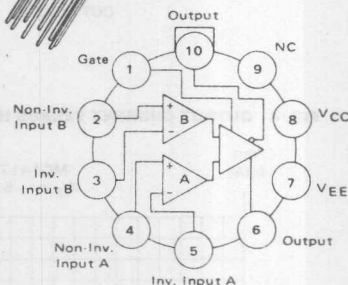
BALANCED MODULATOR



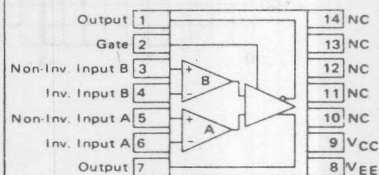
ANALOG SWITCH



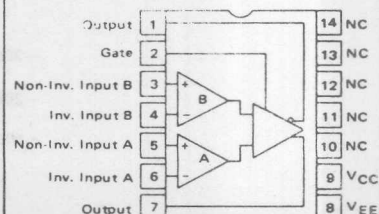
G SUFFIX
METAL PACKAGE
CASE 603
(top view)



F SUFFIX
CERAMIC PACKAGE
CASE 607



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



MC1445, MC1545

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC} V _{EE}	+12 -12	V _{dc} V _{dc}
Input Differential Voltage Range	V _{IDR}	±5.0	Volts
Load Current	I _L	25	mA
Power Dissipation (Package Limitation)	P _D		
Flat Package Derate above T _A = +25°C		500 3.3	mW mW/°C
Ceramic Dual In Line Package Derate above T _A = +25°C		625 5.0	mW mW/°C
Metal Can Derate above T _A = +25°C		680 4.6	mW mW/°C
Operating Ambient Temperature Range MC1445 MC1545	T _A	0 to +75 -55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V_{dc}, V_{EE} = -5.0 V_{dc}, at T_A = +25°C, specifications apply to both input channels unless otherwise noted.)

Characteristic	Fig. No.	Symbol	MC1545			MC1445			Unit
			Min	T _{yp}	Max	Min	T _{yp}	Max	
Single-Ended Voltage Gain	1,12	A _{VS}	16	19	21	16	19.5	23	dB
Bandwidth	1,12	BW	40	50	—	—	50	—	MHz
Input Impedance (f = 50 kHz)	5,14	Z _i	4.0	10	—	3.0	10	—	k ohms
Output Impedance (f = 50 kHz)	6,15	Z _o	—	25	—	—	25	—	Ohms
Output Differential Voltage Range (R _L = 1.0 k ohm, f = 50 kHz)	4,13	V _{ODR}	1.5	2.5	—	1.5	2.5	—	V _{p-p}
Input Bias Current	16	I _{IB}	—	15	25	—	15	30	μA _{dc}
Input Offset Current	16	I _{IO}	—	2.0	—	—	2.0	—	μA _{dc}
Input Offset Voltage	17	V _{IO}	—	1.0	5.0	—	—	7.5	mV _{dc}
Quiescent Output dc Level	17	V _O	—	0.1	—	—	0.1	—	V _{dc}
Output dc Level Change (Gate Input Voltage Change +5.0 V to 0 V)	17	ΔV _O	—	15	—	—	15	—	mV
Common-Mode Rejection Ratio (f = 50 kHz)	9,18	CMRR	—	85	—	—	85	—	dB
Input Common Mode Voltage Range	18	V _{ICR}	—	2.5	—	—	2.5	—	V _o
Gate Characteristics	8	V _{IL(G)}	0.40	0.70	—	0.2	0.4	—	V _{dc}
Gate Input Voltage — Low Logic State (Note 1)		V _{IL(G)}	—	1.5	2.2	—	1.3	3.0	
Gate Input Voltage — High Logic State (Note 2)		V _{IH(G)}	—	—	—	—	—	—	
Gate Input Current — Low Logic State (V _{IL(G)} = 0 V)	18	I _{IL(G)}	—	—	2.5	—	—	4.0	mA
Gate Input Current — High Logic State (V _{IH(G)} = +5.0 V)	18	I _{IH(G)}	—	—	2.0	—	—	4.0	μA
Step Response (e _{in} = 20 mV)	19	t _{PLH}	—	6.5	10	—	6.5	—	ns
		t _{PHL}	—	6.3	10	—	6.3	—	
		t _{TLH}	—	6.5	15	—	6.5	—	
		t _{THL}	—	7.0	15	—	7.0	—	
Wideband Input Noise (5.0 Hz — 10 MHz, R _S = 50 ohms)	10,20	e _n	—	25	—	—	25	—	μV(rms)
DC Power Consumption	11,20	P _C	—	70	110	—	70	150	mW

Note 1. V_{IL(G)} is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.

Note 2. V_{IH(G)} is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

FIGURE 1 - SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

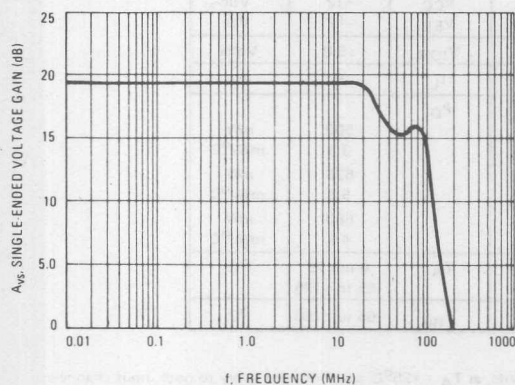


FIGURE 2 - SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

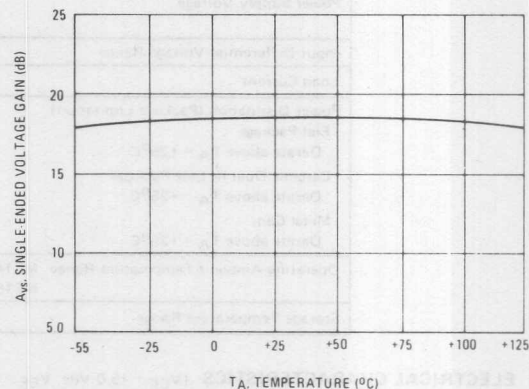


FIGURE 3 - VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

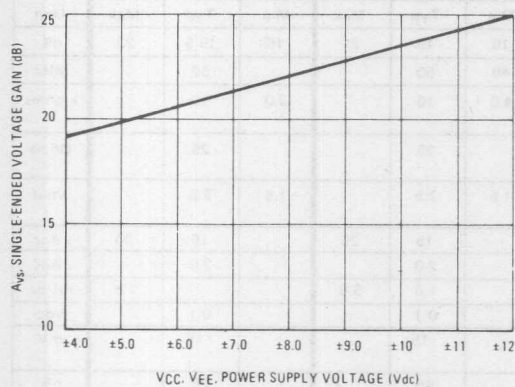


FIGURE 4 - OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

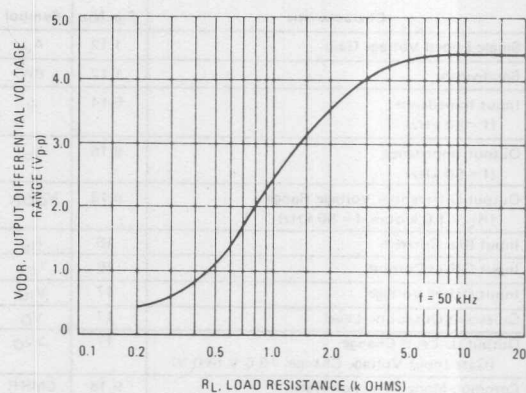


FIGURE 5 - INPUT C_p AND R_p versus FREQUENCY (BOTH CHANNELS)

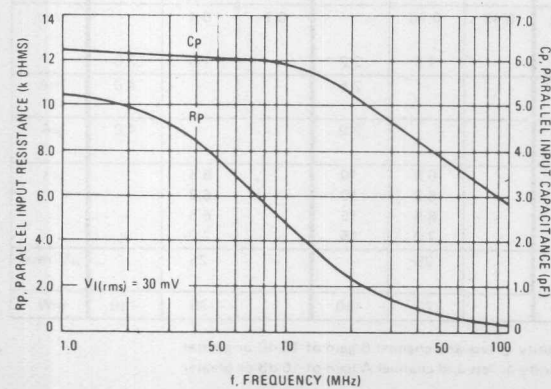


FIGURE 6 - OUTPUT IMPEDANCE versus FREQUENCY

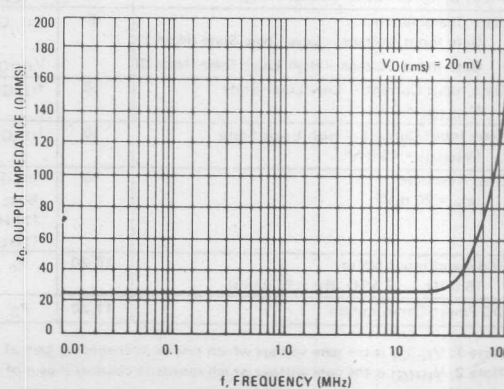


FIGURE 7 - CHANNEL SEPARATION versus FREQUENCY

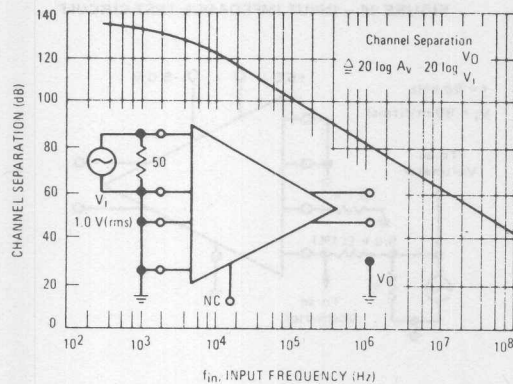


FIGURE 9 - COMMON MODE REJECTION RATIO versus FREQUENCY

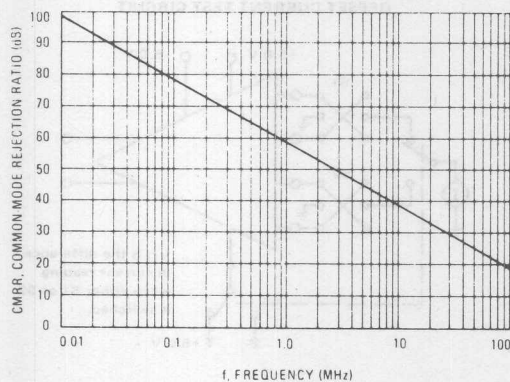


FIGURE 11 - CIRCUIT SCHEMATIC

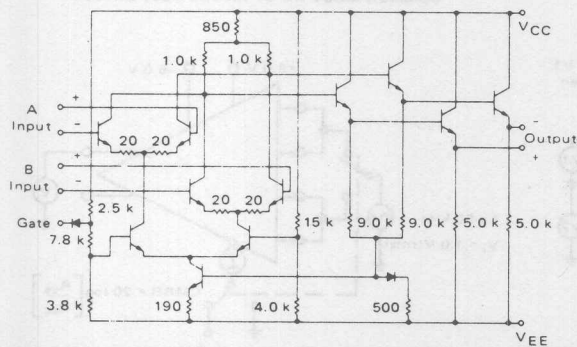


FIGURE 8 - GATE CHARACTERISTICS

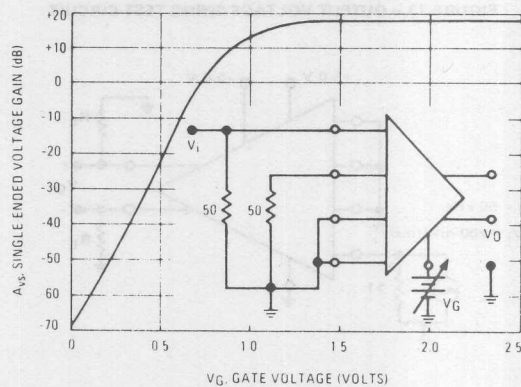


FIGURE 10 - INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

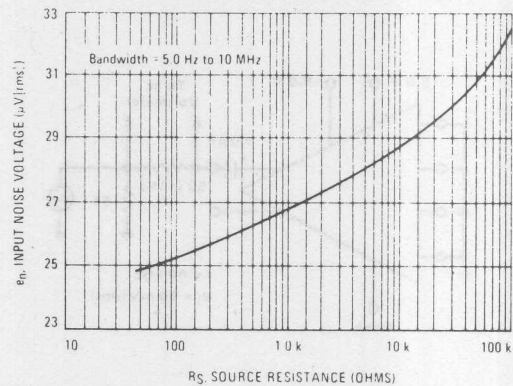


FIGURE 12 - SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT

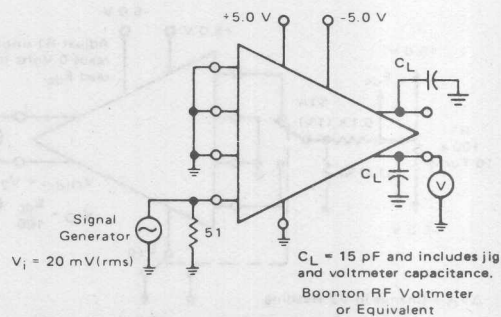


FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

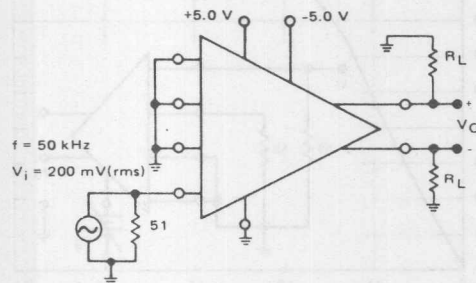


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

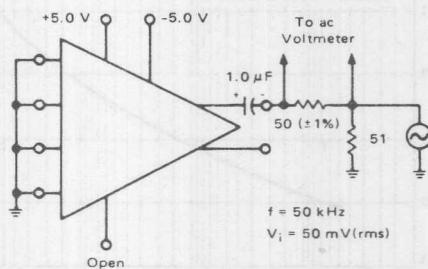


FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

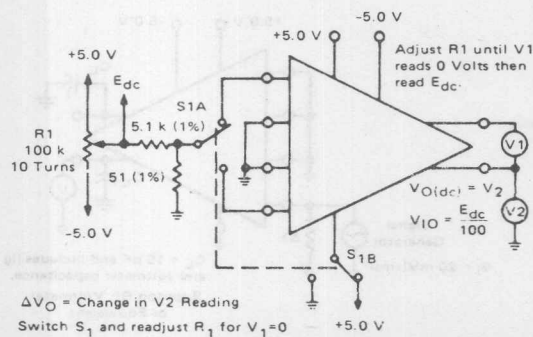


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

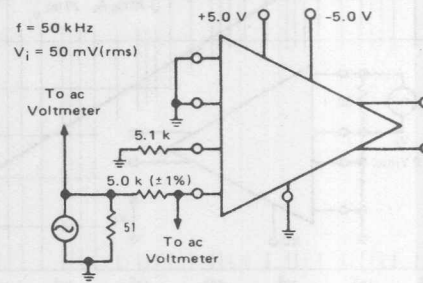


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

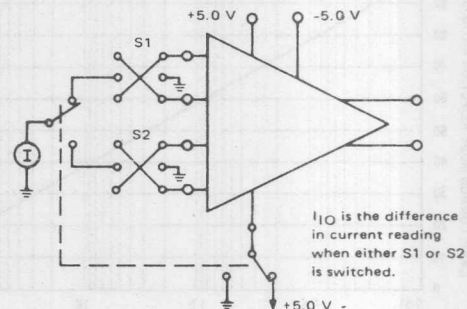
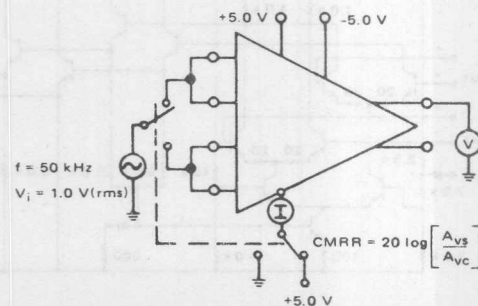


FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT



MC1445, MC1545

FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT

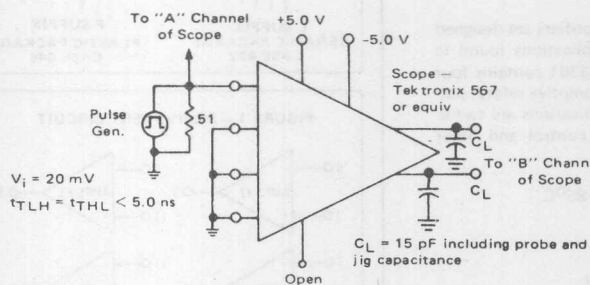


FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

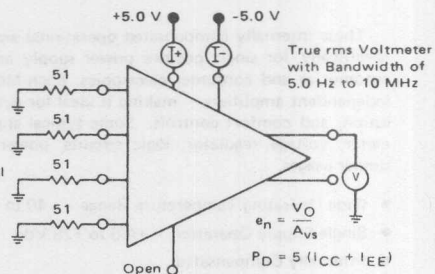
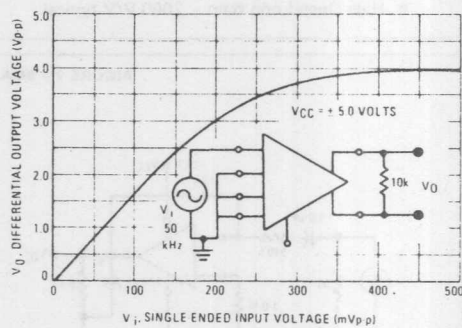


FIGURE 21 – LIMITING CHARACTERISTIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC3301L	-40°C to +85°C	Ceramic DIP
MC3301P	-40°C to +85°C	Plastic DIP

QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER FOR AUTOMOTIVE APPLICATIONS

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in automotive and consumer electronics. Each MC3301 contains four independent amplifiers -- making it ideal for automotive safety, pollution, and comfort controls. Some typical applications are tachometer, voltage regulator, logic circuits, power control and other similar usages.

- Wide Operating Temperature Range -- -40 to +85°C
- Single-Supply Operation -- +4.0 to +28 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth -- 4.0 MHz typical
- Low Input Bias Current -- 50 nA typical
- High Open-Loop Gain -- 2000 V/V typical

MC3301

QUAD OPERATIONAL AMPLIFIER SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

FIGURE 1 - EQUIVALENT CIRCUIT

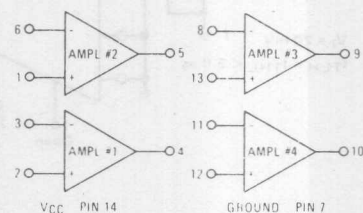


FIGURE 2 - SMALL-SIGNAL TRANSIENT RESPONSE

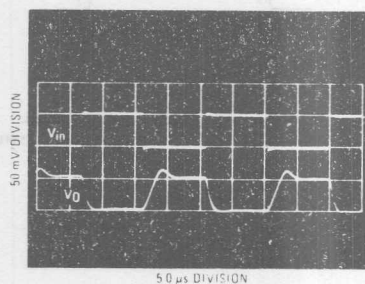
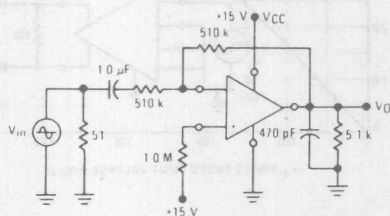


FIGURE 3 - INVERTING AMPLIFIER

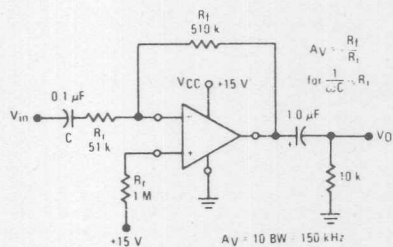
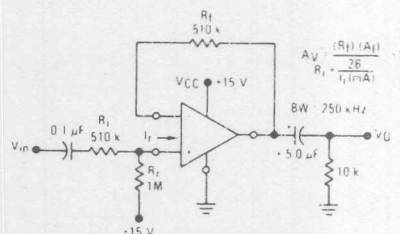


FIGURE 4 - NONINVERTING AMPLIFIER



MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+28	Vdc
Noninverting Input Current	I_r	5.0	mA
Sink Current	I_{sink}	50	mA
Source Current	I_{source}	50	mA
Power Dissipation (Package Limitation) Derate above $T_A = +25^\circ\text{C}$	P_D	625 5.0	mW mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS [$V_{CC} = +15\text{ Vdc}$, $R_L = 5.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ (each amplifier) unless otherwise noted]

Characteristic	Fig.No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain $T_A = +25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	5		A_{vol}	1000 —	2000 1600	— —	V/V
Quiescent Power Supply Current (Total for four amplifiers) Noninverting inputs open Noninverting inputs grounded	6	1	I_{DO} I_{DG}	— —	6.9 7.8	10 14	mAdc
Input Bias Current, $R_L = \infty$ $T_A = +25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	7	2	I_{IB}	— —	50 100	300 —	nAdc
Current Mirror Gain ($I_r = 200\text{ }\mu\text{Adc}$)	7	3	A_I	0.80	0.98	1.16	A/A
Current Mirror Gain Drift $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$					± 2.5	—	%
Output Current Source Capability ($V_{\text{OH}} = 0.4\text{ Vdc}$) ($V_{\text{OH}} = 9.0\text{ Vdc}$) Sink Capability ($V_{\text{OL}} = 0.4\text{ Vdc}$)	8		I_{source} I_{sink}	3.0 0.5	10 0.87	— —	mAdc
Output Voltage High Voltage Low Voltage (Inverting Input Driven) (Noninverting Input Driven)	6		V_{OH} $V_{\text{OL(inv)}}$ $V_{\text{OL(non)}}$	13.5 — —	14.2 0.03 0.6	— 0.1 —	Vdc
Input Resistance (Inverting input only)			R_{in}	0.1	1.0	—	Meg Ω
Slew Rate ($C_L = 100\text{ pF}$, $R_L = 5.0\text{ k}$)			SR	—	0.6	—	V/ μs
Unity Gain Bandwidth		4	BW	—	4.0	—	MHz
Phase Margin		4	ϕ_m	—	70	—	Degrees
Power Supply Rejection ($f = 100\text{ Hz}$)			PSSR	—	55	—	dB
Channel Separation ($f = 1.0\text{ kHz}$)			$e_{\text{O1}}/e_{\text{O2}}$	—	65	—	dB

NOTES:

1. The quiescent current drain will increase approximately 0.3 mA for each inverting or noninverting input that is grounded.
2. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" — as with a conventional IC operational amplifier. As such this

input does not have a requirement for input bias current.

3. Current mirror gain is defined as the current demanded at the inverting input divided by the current into the noninverting input.
4. Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output.

TYPICAL CHARACTERISTICS
 $(V_{CC} = +15 \text{ Vdc}, R_L = 5.0 \text{ k}\Omega, T_A = +25^\circ\text{C})$
 [each amplifier] unless otherwise noted.)

FIGURE 5 — OPEN-LOOP VOLTAGE GAIN

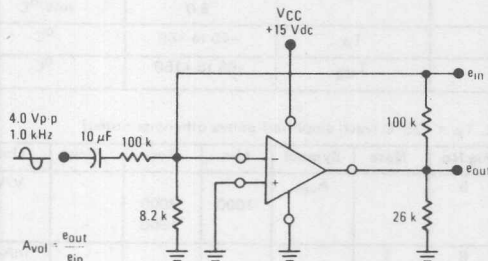


FIGURE 6 — QUIESCENT POWER SUPPLY CURRENT

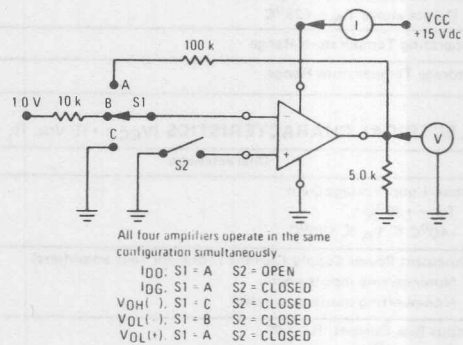


FIGURE 7 — INPUT BIAS CURRENT AND CURRENT MIRROR GAIN

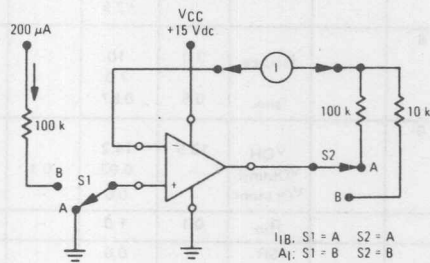
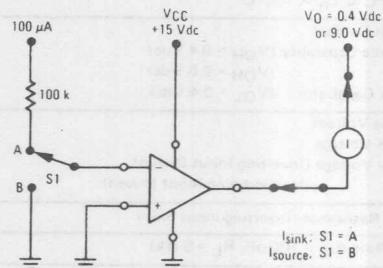


FIGURE 8 — OUTPUT CURRENT



TYPICAL CHARACTERISTICS

($V_{CC} = +15$ Vdc, $R_L = 5.0$ k Ω , $T_A = +25^\circ\text{C}$
[each amplifier] unless otherwise noted.)

FIGURE 9 — OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

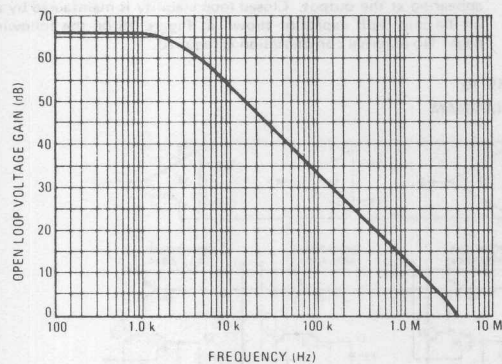


FIGURE 10 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

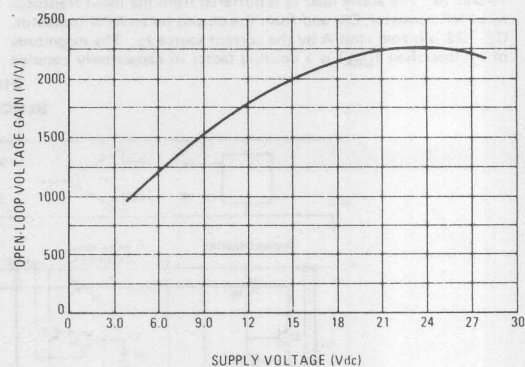


FIGURE 11 — OUTPUT RESISTANCE versus FREQUENCY

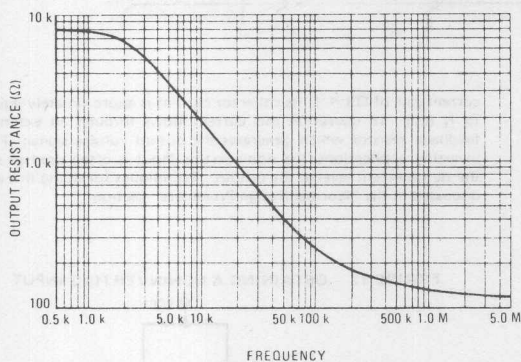


FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE

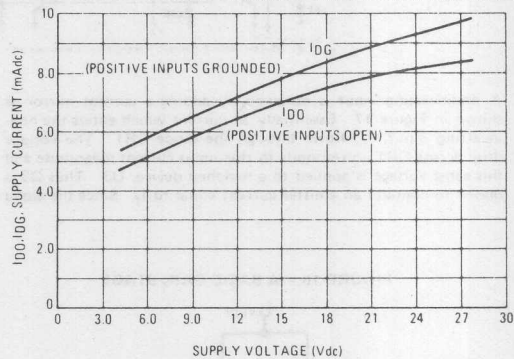


FIGURE 13 — LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

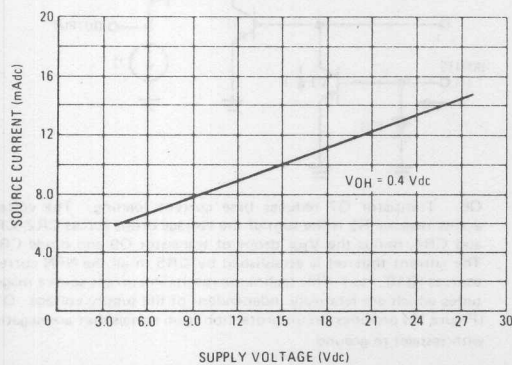
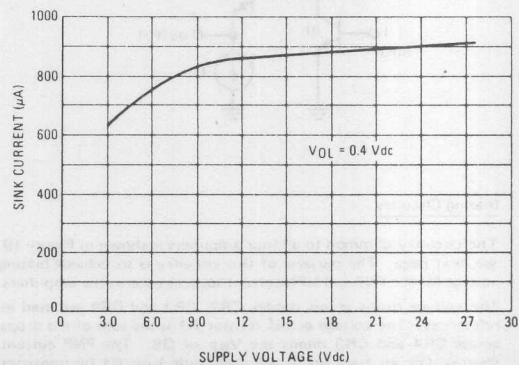


FIGURE 14 — LINEAR SINK CURRENT versus SUPPLY VOLTAGE



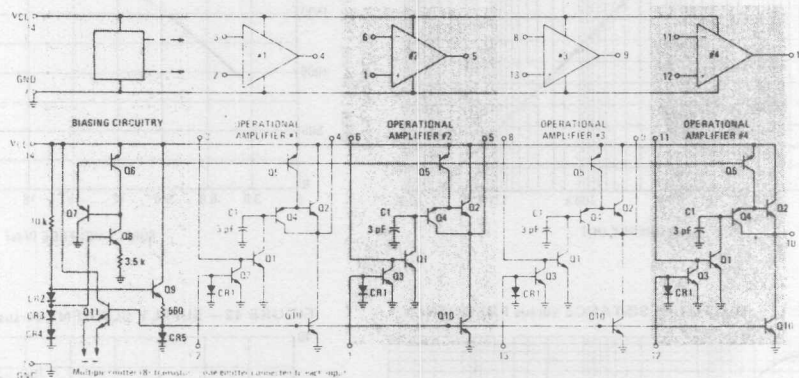
OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2 . The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled

linear operation at the output. The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18 on the following page. No external compensation is required.

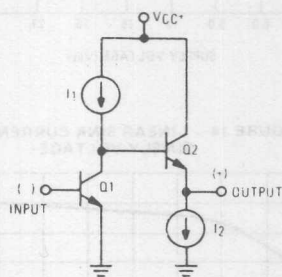
FIGURE 15
BLOCK DIAGRAM



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the non-inverting input, I_r , flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_r . Since the alpha

current gain of Q3 ≈ 1 , its collector current is approximately equal to I_r also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

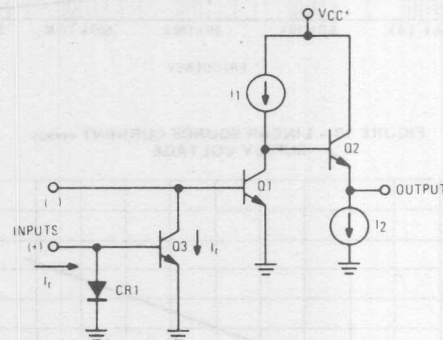
FIGURE 16 - A BASIC GAIN STAGE



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19, see next page. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers. The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor

FIGURE 17 - OBTAINING A NONINVERTING INPUT



Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 15) provides circuit protection from signals that are negative with respect to ground.

FIGURE 18 — A BASIC OPERATIONAL AMPLIFIER

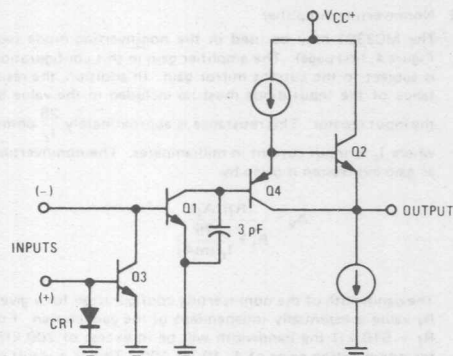
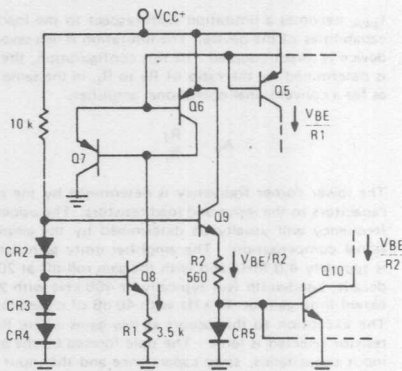


FIGURE 19 — BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μ A to 200 μ A range.

B. V_{CC} Reference Voltage (see Figures 3 and 4)

The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r , allowing the input current, I_r , to be within the range of 10 μ A to 200 μ A. Choosing the feedback resistor, R_f , to be equal to $\frac{1}{2} R_r$ will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

C. Reference Voltage other than V_{CC} (see Figure 20)

The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC} . By setting $R_f = R_r$ (still keeping I_r between 10 μ A and 200 μ A) the output dc level will be equal to V_r . The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_I)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_I\right) \phi$$

where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_I is the current mirror gain.

2. Gain Determination

A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

FIGURE 20 — INVERTING AMPLIFIER WITH ARBITRARY REFERENCE

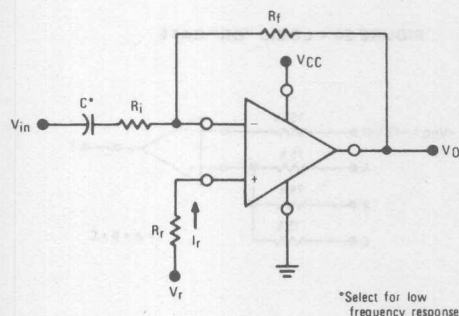
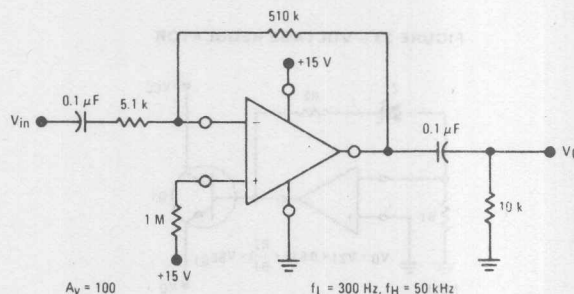


FIGURE 21 — INVERTING AMPLIFIER WITH $A_v = 100$ AND $V_r = V_{CC}$



NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i , in the same manner as for a conventional operational amplifier.

$$A_v = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed loop gain or 40 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

The MC3301 may be used in the noninverting mode (see Figure 4, first page). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting ac gain expression is given by:

$$A_v = \frac{(R_f)(A_1)}{R_i + \frac{26}{I_r (\text{mA})}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For $R_f = 510 \text{ k}\Omega$ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – TACHOMETER CIRCUIT

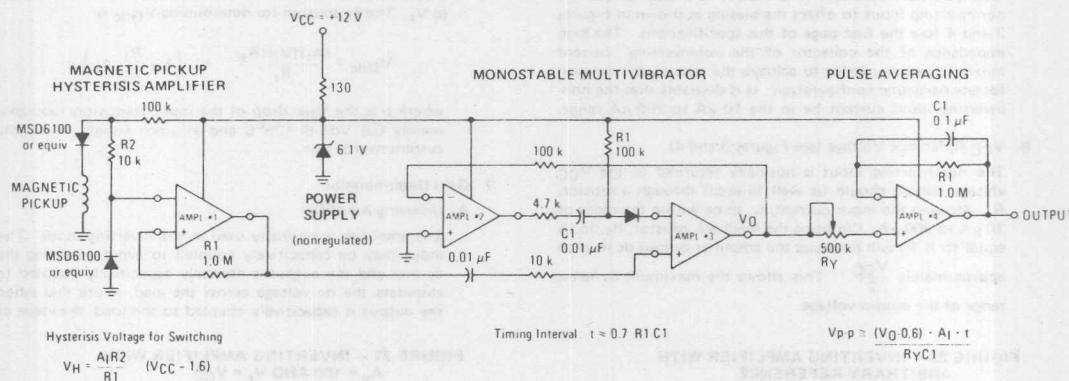


FIGURE 23 – VOLTAGE REGULATOR

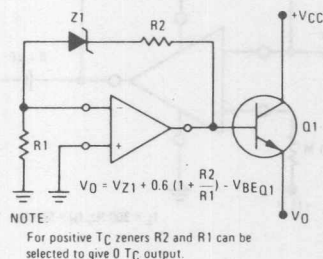
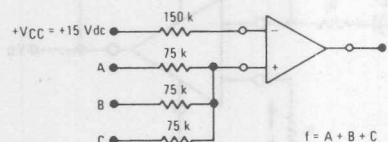


FIGURE 24 – LOGIC "OR" GATE



TYPICAL APPLICATIONS (continued)

FIGURE 25 – LOGIC "NAND" GATE (Large Fan-In)

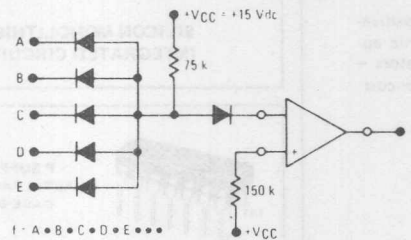


FIGURE 26 – LOGIC "NOR" GATE

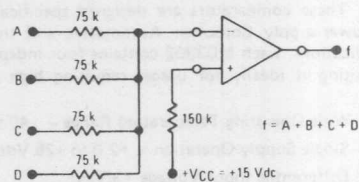


FIGURE 27 – R-S FLIP-FLOP

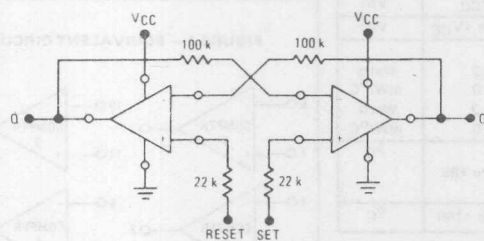


FIGURE 28 – ASTABLE MULTIVIBRATOR

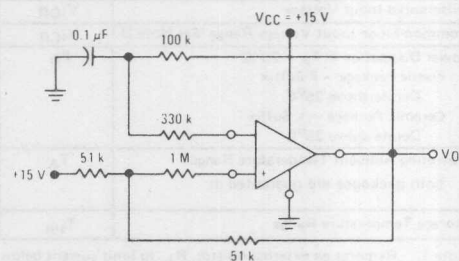


FIGURE 29 – POSITIVE-EDGE DIFFERENTIATOR

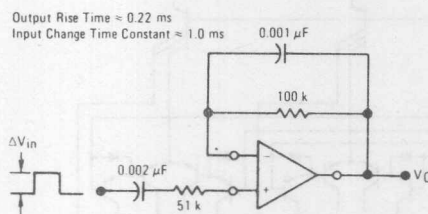
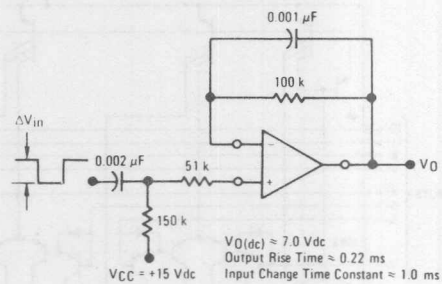


FIGURE 30 – NEGATIVE-EDGE DIFFERENTIATOR



MC3302

QUAD SINGLE-SUPPLY COMPARATOR

These comparators are designed specifically for single positive-power-supply Consumer Automotive and Industrial electronic applications. Each MC3302 contains four independent comparators – suiting it ideally for usages requiring high density and low-cost.

- Wide Operating Temperature Range – -40 to $+85^{\circ}\text{C}$
- Single-Supply Operation – $+2.0$ to $+28$ Vdc
- Differential Input Voltage $= \pm V_{CC}$
- Compare Voltages at Ground Potential
- MTTL Compatible
- Low Current Drain – $700\mu\text{A}$ typical @ $V_{CC} +5.0$ to $+28$ Vdc
- Outputs can be Connected to Give the Implied AND Function

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

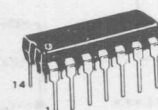
Rating	Symbol	Value	Unit
Power Supply Range	V_{CC}	$+2.0$ to $+28$	Vdc
Output Sink Current (See Note 1)	I_O	20	mA
Differential Input Voltage	V_{IDR}	$\pm V_{CC}$	Vdc
Common-Mode Input Voltage Range (See Note 2)	V_{ICR}	-0.3 to $+V_{CC}$	Vdc
Power Dissipation @ $T_A = 25^{\circ}\text{C}$	P_D		
Plastic Package – P Suffix		1.2	Watts
Derate above 25°C		10	mW/ $^{\circ}\text{C}$
Ceramic Package – L Suffix		1.2	Watts
Derate above 25°C		10	mW/ $^{\circ}\text{C}$
Operating Ambient Temperature Range both packages are guaranteed at	T_A	-40 to $+85$	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$	$^{\circ}\text{C}$

Note 1. Requires an external resistor, R_L , to limit current below maximum rating.

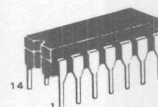
Note 2. If either (+) or (–) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns “on” causing high input current and possible faulty outputs.

QUAD COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – EQUIVALENT CIRCUIT

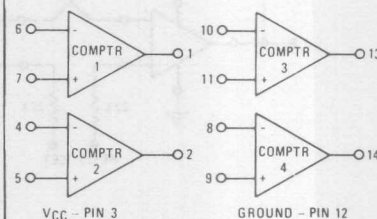
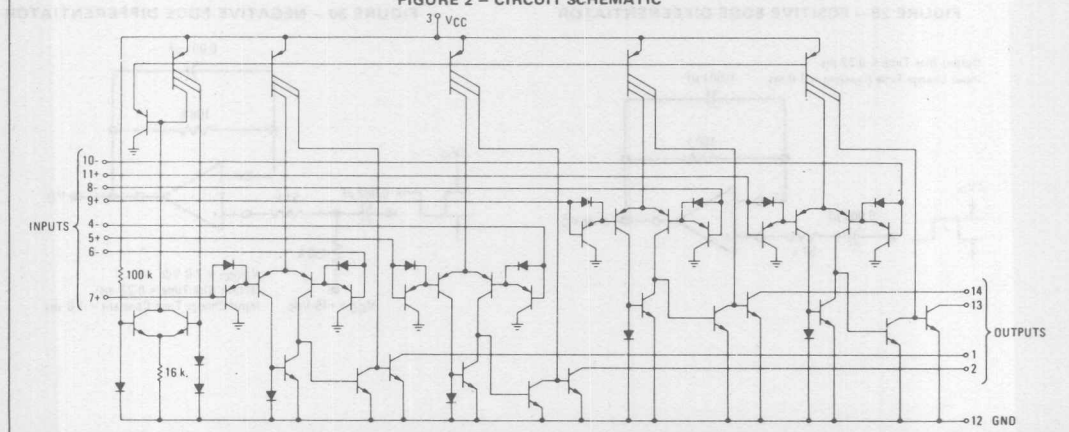
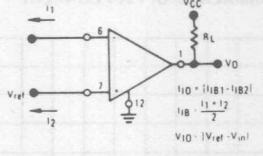
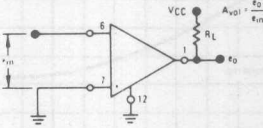
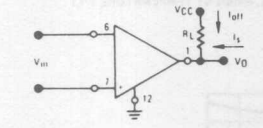
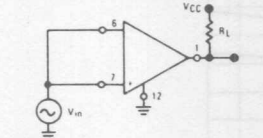
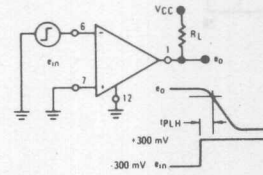
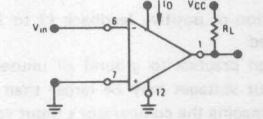


FIGURE 2 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ Vdc, $T_A = +25^\circ\text{C}$ (each comparator) unless otherwise noted.)

Characteristic Definitions (1/4 Circuit Shown)	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage ($V_{ref} = 1.2$ Vdc) ($T_A = +25^\circ\text{C}$) ($T_A = -40$ to $+85^\circ\text{C}$)	V_{IO}	—	3.0	20	mVdc
	Input Offset Current	I_{IO}	—	3.0	—	nAdc
	Input Bias Current ($T_A = +25^\circ\text{C}$) ($T_A = -40$ to $+85^\circ\text{C}$)	I_{IB}	—	30	500	nAdc
	Voltage Gain ($T_A = +25^\circ\text{C}$, $R_L = 15$ k Ω)	A_{Vol}	2,000	30,000	—	V/V
	Transconductance	g_m	—	2.0	—	mhos
	Input Differential Voltage Range	V_{IDR}	$\pm V_{CC}$	—	—	Vdc
	Output Leakage Current (Output Voltage High)	I_{OL}	—	—	1.0	μAdc
	Output Voltage - Low Logic State ($I_s = 2.0$ mA, $V_{CC} = +5.0$ to $+28$ Vdc)	V_{OL}	—	150	400	mVdc
	Output Sink Current ($V_{CC} = +5.0$ Vdc) ($T_A = +25^\circ\text{C}$, $V_{OL} = 400$ mV) ($T_A = -40$ to $+85^\circ\text{C}$, $V_{OL} = 800$ mV)	I_{sink}	— 2.0	6.0 —	— —	mAdc
	Input Common-Mode Voltage Range ($V_{CC} = +28$ Vdc)	V_{ICR}	0-26	—	—	Volts
	Common-Mode Rejection Ratio	CMRR	—	60	—	dB
	Propagation Delay Time For Positive and Negative-Going Input Pulse ($R_L = 15$ k Ω)	$t_{PHL/LH}$	—	2.0	—	μs
	Transition Time ($R_L = 15$ k Ω)	t_{THL} t_{TLH}	— —	0.15 0.8	— —	μs
	Power Supply Current (Total of four comparators) ($R_L = \infty$, $V_{CC} = +5.0$ to $+28$ Vdc)	I_{CC} I_{EE}	—	0.7	1.8	mAdc

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A +25°C (each comparator) unless otherwise noted.)

FIGURE 3 – NORMALIZED INPUT OFFSET VOLTAGE

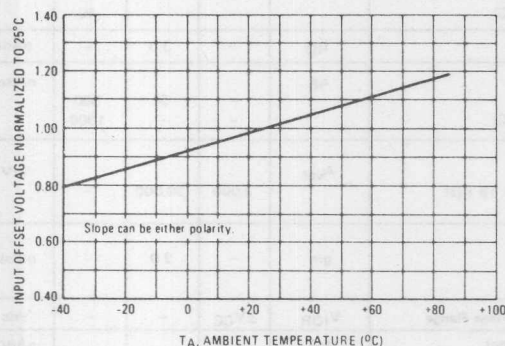


FIGURE 4 – NORMALIZED OFFSET CURRENT

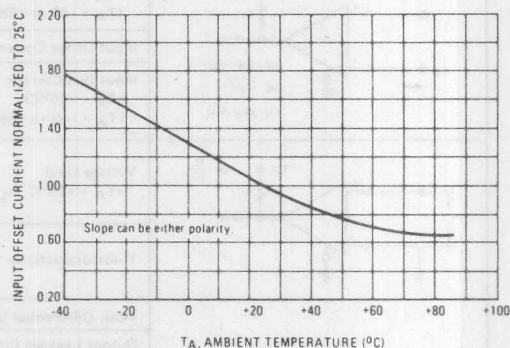
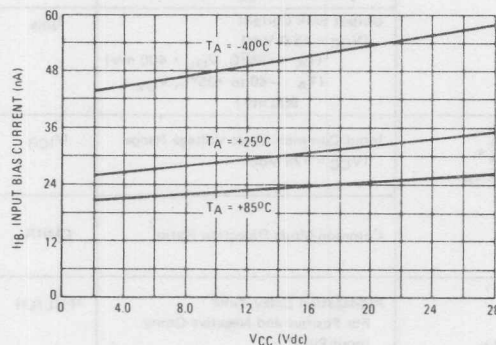


FIGURE 5 – INPUT BIAS CURRENT



TYPICAL APPLICATIONS

The MC3302 is a quad comparator having high gain, wide bandwidth characteristics. This gives the device oscillator tendencies if the outputs capacitively couple to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should

be used. The addition of positive feedback (1 to 10 mV) is also recommended.

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than -300 mV should not be used.

TYPICAL APPLICATIONS (continued)

FIGURE 6 - FREE-RUNNING SQUARE-WAVE OSCILLATOR

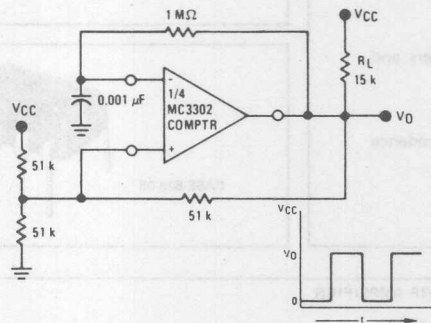


FIGURE 7 - TIME DELAY GENERATOR

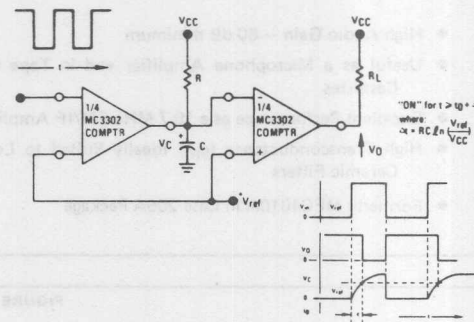
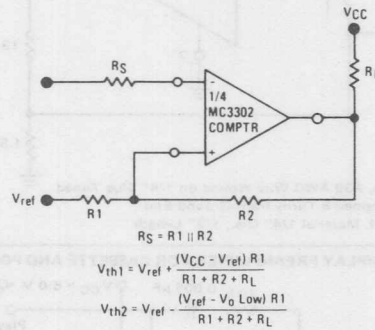


FIGURE 8 - COMPARATOR WITH HYSTERESIS



MC3310P

WIDE-BAND AMPLIFIER

... designed for FM/IF and low-level audio applications.

- High Audio Gain – 60 dB minimum
- Useful as a Microphone Amplifier and in Tape Recorders and Cassettes
- Excellent Performance as a 10.7 MHz FM/IF Amplifier
- High Transconductance (g_m) Ideally Suited to Low Impedance Ceramic Filters
- Formerly MFC4010A in Case 206A Package

WIDE-BAND AMPLIFIER

SILICON MONOLITHIC
FUNCTIONAL CIRCUIT

CASE 626-03



FIGURE 1 – FM/IF AMPLIFIER

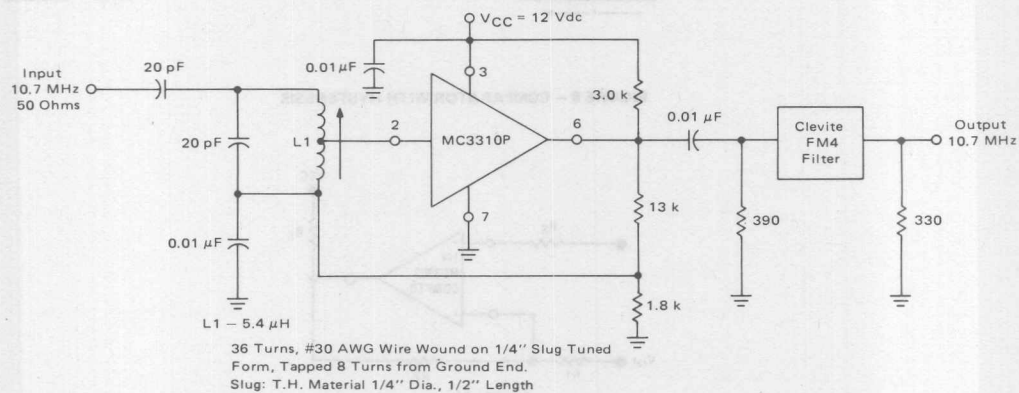
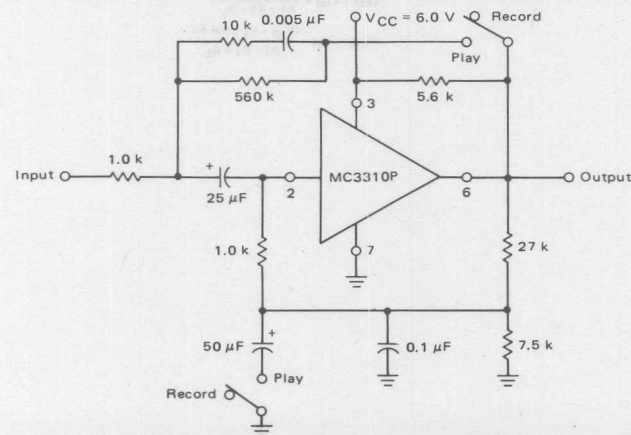


FIGURE 2 – RECORD/PLAY PREAMPLIFIER FOR CASSETTE AND PORTABLE TAPE RECORDERS



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted).

Rating	Value	Unit
Power Supply Voltage	21	Vdc
Power Dissipation @ $T_A = 25^\circ\text{C}$ (Package Limitation) Derate above 25°C	1.2	Watts
Operating Ambient Temperature Range	0 to +75	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 6.0\text{ Vdc}$, $T_A = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Min	Typ	Max	Unit
Open Loop Voltage Gain (Figure 3) ($f = 1.0\text{ kHz}$)	60	68	—	dB
h Parameters(1) ($f = 1.0\text{ kHz}$)	h_{11}	1.0	—	k ohms
	h_{12}	10^{-6}	—	—
	h_{21}	1000	—	—
	h_{22}	10^{-5}	—	mhos
Output Noise Voltage (Figure 3) (BW = 20 Hz to 20 kHz, $R_S = 1.0\text{ k ohms}$)	—	3.0	—	mV(RMS)
	—	3.0	—	—
Current Drain	—	3.0	—	mA

HIGH FREQUENCY CHARACTERISTICS ($V_{CC} = 12\text{ Vdc}$, $f = 10.7\text{ MHz}$, $T_A = 25^\circ\text{C}$ unless otherwise noted).

Power Gain (Figure 1) $e_{in} = 0.1\text{ mVRMS}$	—	42	—	dB
Noise Figure (Figure 1) ($R_S \approx 740\text{ Ohms}$)	—	6.0	—	dB
y Parameters(1) ($f = 10.7\text{ MHz}$, $I_2 = 2.0\text{ mA}$)	Y_{11}	$1.3 + j1.5$	—	mmhos
	Y_{12}	$-3.4 + j8.1$	—	μmhos
	Y_{21}	$-0.33 + j0.68$	—	mho
	Y_{22}	$120 + j0$	—	μmhos

(1) Device only, without external passive components.

FIGURE 3 — AUDIO TEST CIRCUIT

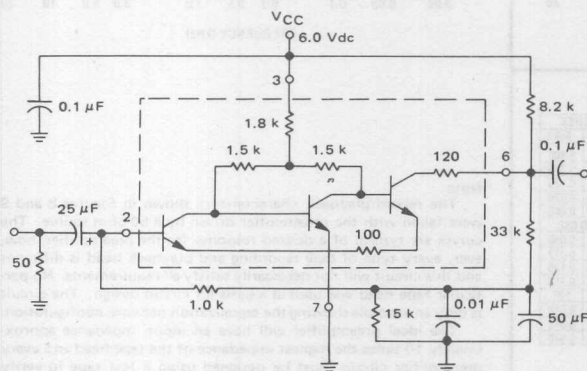
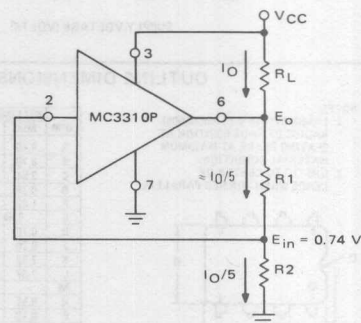


FIGURE 4 — BIASING RECOMMENDATIONS



Select: V_{CC} , E_o , and I_O
 Solve for: $R_L = (V_{CC} - E_o)/I_O$
 Let: $R_2 = 5(0.74)/I_O$
 Then: $R_1 = R_2 (E_o - 0.74)/0.74$



MOTOROLA Semiconductor Products Inc.

TYPICAL CHARACTERISTICS

AUDIO PERFORMANCE CHARACTERISTICS
(for Test Circuit Figure 3)

FIGURE 5 - VOLTAGE GAIN versus FREQUENCY

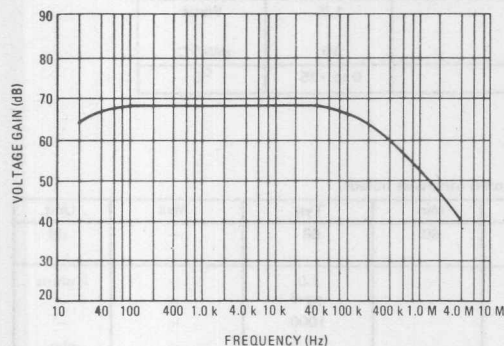


FIGURE 6 - VOLTAGE GAIN versus POWER SUPPLY

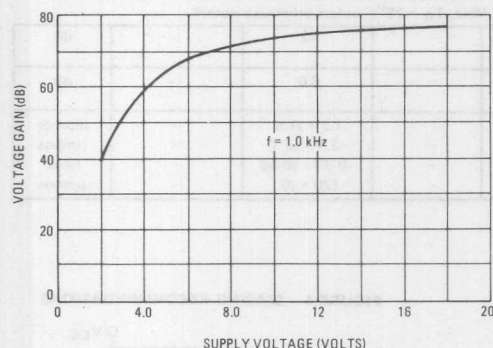
*TAPE PREAMPLIFIER PERFORMANCE
(for Circuit Figure 2)

FIGURE 7 - RECORD VOLTAGE GAIN versus FREQUENCY

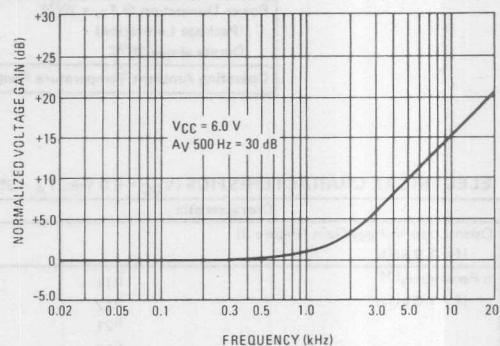
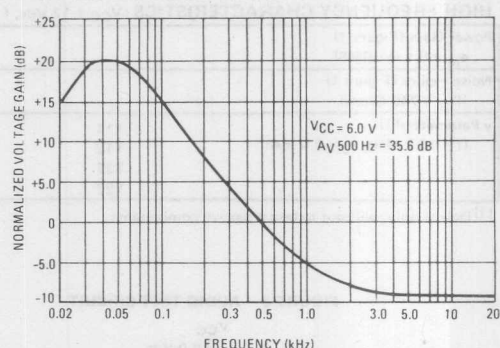
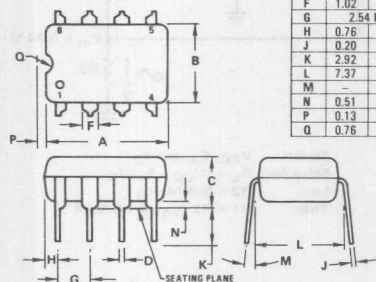


FIGURE 8 - PLAYBACK VOLTAGE GAIN versus FREQUENCY



OUTLINE DIMENSIONS

- NOTES:
1. LEADS WITHIN 0.13 mm (0.005)
RADIUS OF TRUE POSITION AT
SEATING PLANE AT MAXIMUM
MATERIAL CONDITION.
2. DIM "L" TO CENTER OF
LEADS WHEN FORMED PARALLEL.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	10°		10°	
N	0.51	0.76	0.020	0.030
P	0.13	0.38	0.005	0.015
Q	0.76	1.02	0.030	0.040

CASE 626-03

Note:

The record/playback characteristics shown in Figures 8 and 9 were taken with the preamplifier driven by a 50 ohm source. The curves are typical of a desired response for the preamplifier; however, every type of tape recording and playback head is different and this circuit will not necessarily satisfy all requirements. No particular tape head was used as a basis for circuit design. The circuit is only an example showing the equalization network configuration.

The ideal preamplifier will have an input impedance approximately 10 times the highest impedance of the tape head and every preamplifier circuit must be designed using a test tape to verify the response of the design.

10.7 MHz y PARAMETERS

FIGURE 9 – INPUT ADMITTANCE

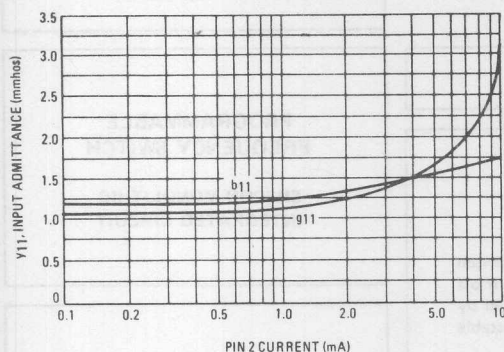


FIGURE 10 – REVERSE TRANSFER ADMITTANCE

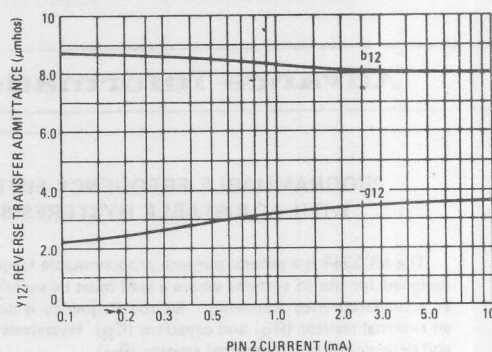


FIGURE 11 – FORWARD TRANSFER ADMITTANCE

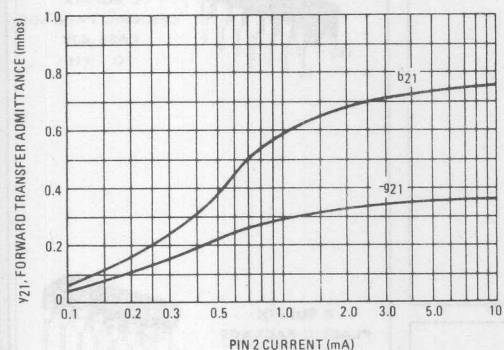


FIGURE 12 – OUTPUT ADMITTANCE

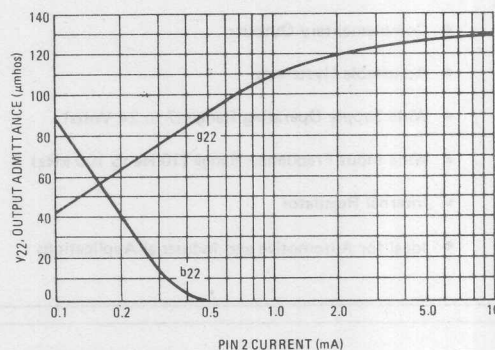
10.7 MHz PERFORMANCE
(Circuit of Figure 1)

FIGURE 13 – POWER GAIN versus SUPPLY VOLTAGE

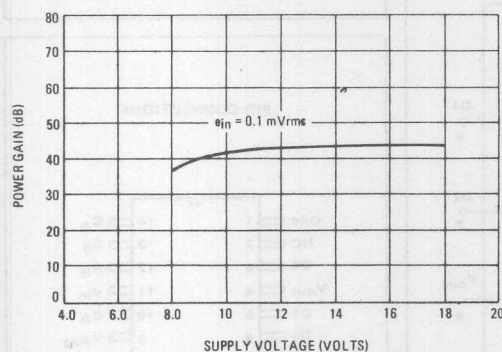
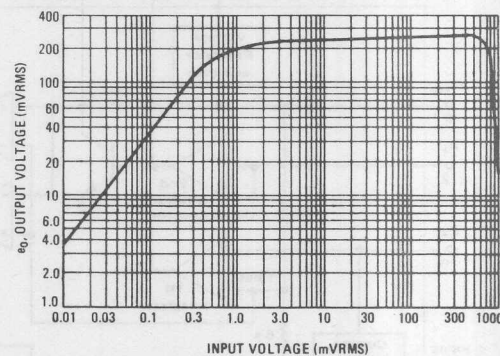


FIGURE 14 – VOLTAGE TRANSFER CHARACTERISTIC



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3344L	-40°C to +85°C	Ceramic DIP
MC3344P	-40°C to +85°C	Plastic DIP

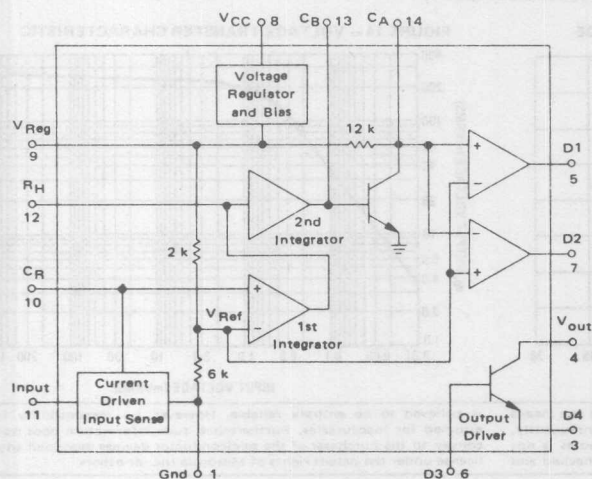
Advance Information

PROGRAMMABLE FREQUENCY SWITCH WITH ADJUSTABLE HYSTERESIS

The MC3344 is a general purpose programmable frequency switch designed for use in systems where a load must be switched on or off at a predetermined frequency. Switch frequency is determined by an external resistor (R_P) and capacitor (C_P). Hysteresis is adjustable and determined by an external resistor (R_H).

- Isolated Driver Transistor
- Complementary Outputs
- Adjustable Hysteresis
- Wide Supply Operating Range (7 to 24 Volts)
- Wide Input Frequency Range (10 Hz to 100 kHz)
- Internal Regulator
- Ideal for Automotive and Industrial Applications

FIGURE 1 -- CIRCUIT BLOCK DIAGRAM

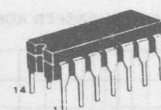


This is advance information and specifications are subject to change without notice.

MC3344

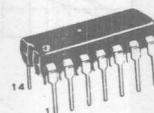
PROGRAMMABLE FREQUENCY SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

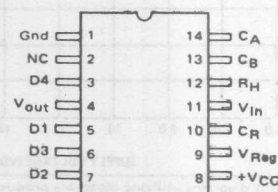


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO : 116

P SUFFIX
PLASTIC PACKAGE
CASE 646



PIN CONNECTIONS



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	24	Vdc
Peak Input Current	I_I	10	mA
Junction Temperature	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = +15\text{ Vdc}$ unless otherwise specified)

Characteristic	Test Ckts	Symbol	Min	Typ	Max	Unit
Supply Current	2	I_D	—	2.5	4.0	mA
Trigger Reset Voltage $I_{in} = 200\ \mu\text{A}$ $I_{in} = 500\ \mu\text{A}$	3	V_{CR1} V_{CR2}	0.25 —	— —	— 0.25	Vdc
Regulator Output Voltage	4	V_{Reg}	4.0	4.5	5.0	Vdc
Threshold Output Voltage $V_{TCR} = V_{CR}/V_{Reg}$	5	V_{TCR}	0.739	0.750	0.761	V/V
Hysteresis Sink Current	6	I_H	100	400	—	μA
Second Comparator Output D1 Leakage D2 Source D1 Source D2 Leakage	7	I_{D1L} I_{D2S} I_{D1S} I_{D2L}	— 100 100 —	— 250 200 —	100 — — 100	nA μA μA nA
Output Driver Gain $I_C = 5.0\text{ mA}$	8	h_{FE1}	50	100	—	—
Output Driver Voltage Standoff $I_D = 5.0\text{ mA}$	9	BV_{CEO}	25	30	—	Vdc
Integrator Transistor Gain $h_{FE2} = \Delta I_C / \Delta I_B$ $I_{C1} = 0.4\text{ mA}$, $I_{C2} = 0.6\text{ mA}$	10	h_{FE2}	50	200	300	—

TEST CIRCUITS

FIGURE 2 – SUPPLY CURRENT

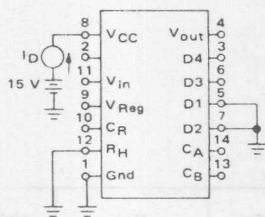
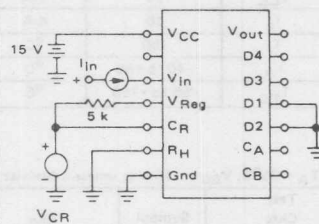


FIGURE 3 – TRIGGER RESET VOLTAGE



$$I_{in} = 200 \mu A, V_{CR} \geq 0.25 V$$

$$I_{in} = 600 \mu A, V_{CR} \leq 0.25 V$$

FIGURE 4 – REGULATOR OUTPUT VOLTAGE

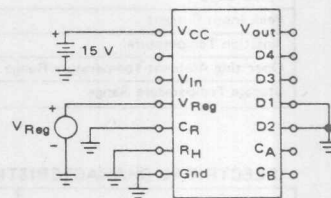


FIGURE 5 – THRESHOLD VOLTAGE RATIO

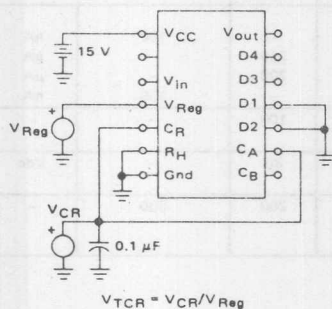
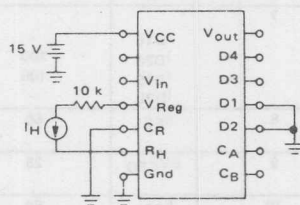
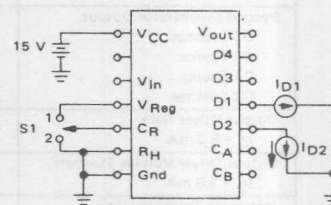


FIGURE 6 – HYSTERESIS SINK CURRENT

FIGURE 7 – I_{D1L}/I_{D2S} , I_{D2L}/I_{D1S} 

$$I_{D1L}/I_{D2S} - S1 \text{ in position 1}$$

$$I_{D2L}/I_{D1S} - S1 \text{ in position 2}$$

FIGURE 8 – OUTPUT DRIVER GAIN

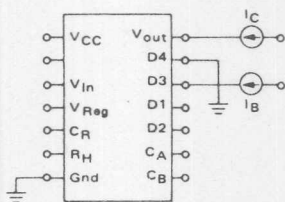
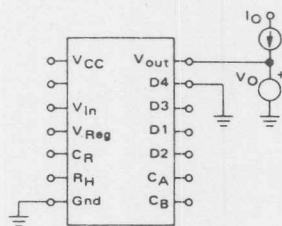
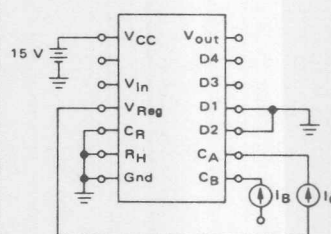
FIGURE 9 – BV_{CEO} OF OUTPUT TRANSISTOR

FIGURE 10 – INTEGRATOR TRANSISTOR GAIN



APPLICATIONS INFORMATION

The voltage regulator and bias section provides the proper biasing and regulated supply voltage to the integrated circuit.

A square wave, when applied to the RC differentiator, provides input current pulses to the IC. The input circuit discharges and clamps, for a predetermined time, the voltage across capacitor C_R . This establishes the initial ramp voltage (V_{sat}) and allows initiation of a new voltage ramp after each positive transition of the input waveform.

The voltage, V_{CR} , ramps from V_{sat} to the final value, V_{Reg} , charging through R_R .

If V_{CR} is never allowed to reach V_{Ref} due to quick reset pulses, the second integrator amplifier will not be activated, and capacitor C_{AB} is allowed to charge through the 12 k Ω resistor until V_{CA} is greater than V_{Ref} . At this point, D1 will switch ON and D2 will switch OFF. By connecting either D1 or D2 to the D3 drive pin, the output drive transistor may be either switched ON or OFF at the switch point.

If V_{CR} is allowed to ramp above V_{Ref} before being reset, the second integrator amplifier is driven ON which discharges and resets capacitor C_{AB} keeping V_{CA} low with respect to V_{Ref} .

V_{CA} will always be low with respect to V_{Ref} if the time from reset C_R to $V_{CR} = V_{Ref}$ is less than the time

from reset C_{AB} to $V_{CA} = V_{Ref}$.

Resistor R_H provides hysteresis around the switch point (i.e., frequency to switch the output driver ON, when connected to the D1 terminal, is higher than the frequency required to switch the output driver OFF). If no hysteresis is desired then the R_H resistor should be omitted and pin 12 grounded.

Circuit Equations:

The first integrator time constant is

$$T1 = R_H \parallel R_R C_R. \text{ If } R_H \text{ is omitted then } T1 = R_R C_R.$$

The second integrator time constant is

$$T2 = (12 \text{ k}) (h_{FE2}) (C_{AB}).$$

$$f1 = \text{Switch Point frequency} \approx \frac{1}{1.39 R_R C_R}$$

$$f2 = \text{Hysteresis Switch Point frequency} \approx$$

$$\frac{1}{R_R \parallel R_H C_R \ln \left[\frac{R_H}{0.25 R_H - 0.75 R_R} \right]}$$

2

FIGURE 11 – TYPICAL APPLICATION

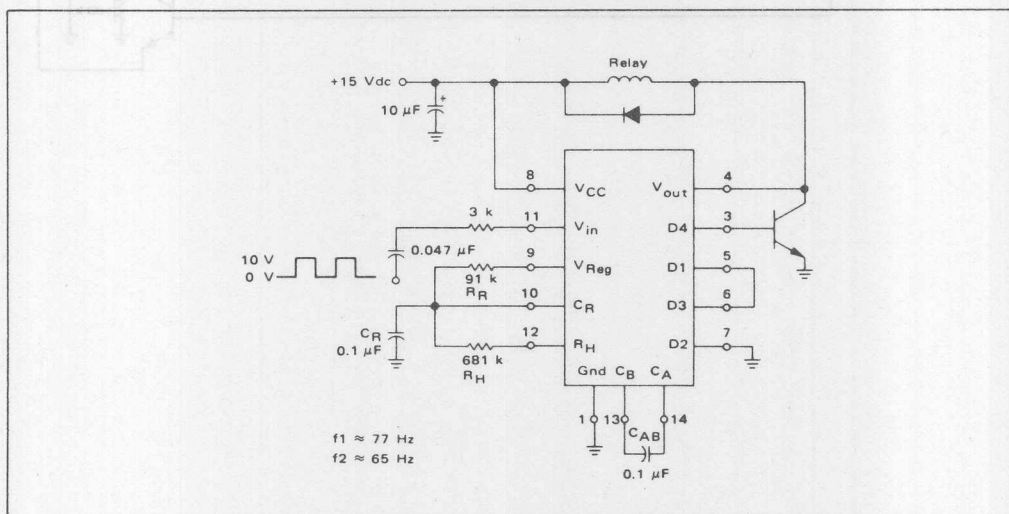
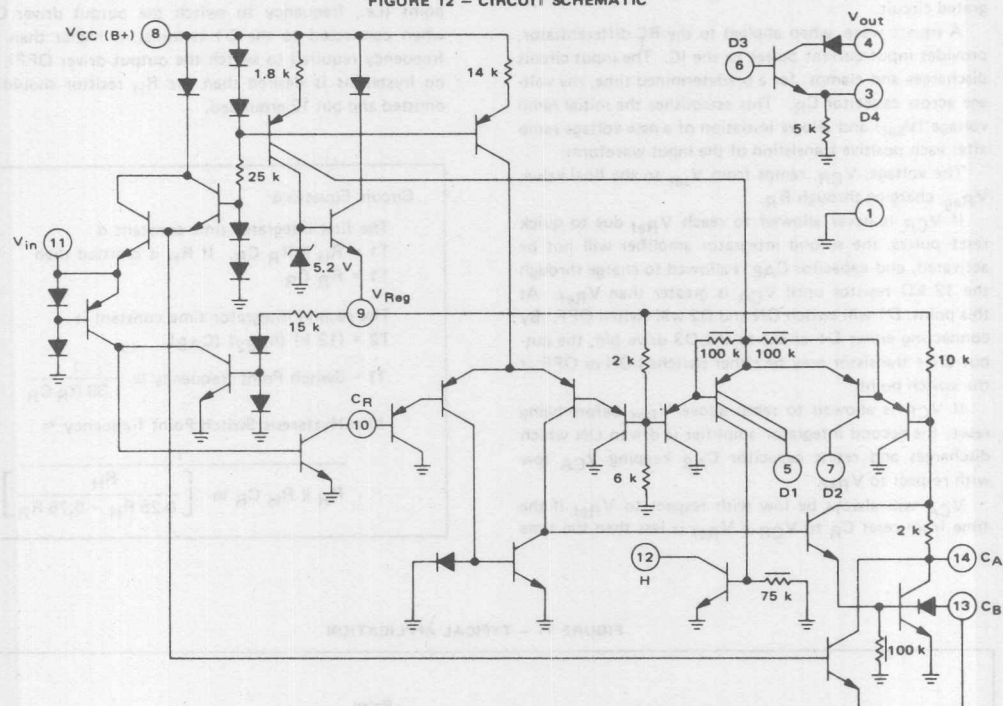


FIGURE 12 - CIRCUIT SCHEMATIC



Device	Temperature Range	Package
MC3346P	-40°C to +85°C	Plastic DIP
MC3386P	-40°C to +85°C	Plastic DIP

MC3346
MC3386

ONE DIFFERENTIALLY-CONNECTED PAIR AND THREE ISOLATED TRANSISTOR ARRAY

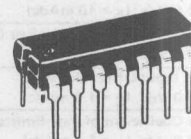
The MC3346 and MC3386 are designed for general-purpose, low power applications for consumer and industrial designs.

- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified - 10 μ A to 10 mA
- Five General-Purpose Transistors in One Package

GENERAL-PURPOSE TRANSISTOR ARRAY SILICON MONOLITHIC INTEGRATED CIRCUIT.

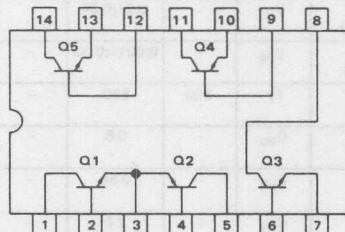
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current - Continuous	I_C	50	mA dc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C Derate Each Transistor @ 25°C	P_D	1.2 10 300	Watts mW/ $^\circ\text{C}$ mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$



P SUFFIX
PLASTIC PACKAGE
CASE 646

2



MC3346, MC3386

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MC3346P			MC3386P			Unit
		Min	Typ	Max	Min	Typ	Max	
STATIC CHARACTERISTICS								
Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{Adc}$)	BV_{CBO}	20	60	—	20	60	—	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 1.0 \text{ mAdc}$)	BV_{CEO}	15	—	—	15	—	—	Vdc
Collector-Substrate Breakdown Voltage ($I_C = 10 \mu\text{A}$)	BV_{CIO}	20	60	—	20	60	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{Adc}$)	BV_{EBO}	5.0	7.0	—	5.0	7.0	—	Vdc
Collector-Base Cutoff Current ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	—	40	—	—	100	nAdc
DC Current Gain ($I_C = 10 \text{ mAdc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 1.0 \text{ mAdc}$, $V_{CE} = 3.0 \text{ Vdc}$) ($I_C = 10 \mu\text{Adc}$, $V_{CE} = 3.0 \text{ Vdc}$)	h_{FE}	— 40 —	140 130 60	— — —	— 40 —	— 130 —	— — —	—
Base-Emitter Voltage ($V_{CE} = 3.0 \text{ Vdc}$, $I_E = 1.0 \text{ mAdc}$) ($V_{CE} = 3.0 \text{ Vdc}$, $I_E = 10 \text{ mAdc}$)	V_{BE}	— —	0.72 0.80	— —	— —	0.72 0.80	— —	Vdc
Input Offset Current for Matched Pair Q1 and Q2 ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	$ I_{IO1} $ $ I_{IO2} $	—	0.3	2.0	—	0.3	—	μAdc
Magnitude of Input Offset Voltage ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	—	—	0.5	5.0	—	0.5	—	mVdc
Temperature Coefficient of Base-Emitter Voltage ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	$\frac{\Delta V_{BE}}{\Delta T}$	—	-1.9	—	—	-1.9	—	mV/ $^{\circ}\text{C}$
Temperature Coefficient	$\frac{ \Delta V_{IO} }{\Delta T}$	—	1.0	—	—	1.0	—	$\mu\text{V}/^{\circ}\text{C}$
Collector-Emitter Cutoff Current ($V_{CE} = 10 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	—	0.5	—	—	5.0	μAdc
DYNAMIC CHARACTERISTICS								
Low Frequency Noise Figure ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 100 \mu\text{Adc}$, $R_S = 1.0 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	NF	—	3.25	—	—	3.25	—	dB
Forward Current Transfer Ratio ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$, $f = 1.0 \text{ kHz}$)	h_{FE}	—	110	—	—	110	—	—
Short-Circuit Input Impedance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	h_{ie}	—	3.5	—	—	3.5	—	$\text{k}\Omega$
Open-Circuit Output Impedance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	h_{oe}	—	15.6	—	—	15.6	—	μmhos
Reverse Voltage Transfer Ratio ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$)	h_{re}	—	1.8	—	—	1.8	—	$\times 10^{-4}$
Forward Transfer Admittance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$, $f = 1.0 \text{ MHz}$)	y_{fe}	—	31-j1.5	—	—	31-j1.5	—	—
Input Admittance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$, $f = 1.0 \text{ MHz}$)	y_{ie}	—	0.3+j0.04	—	—	0.3+j0.04	—	—
Output Admittance ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 1.0 \text{ mAdc}$, $f = 1.0 \text{ MHz}$)	y_{oe}	—	0.001+j0.03	—	—	0.001+j0.03	—	—
Current-Gain – Bandwidth Product ($V_{CE} = 3.0 \text{ Vdc}$, $I_C = 3.0 \text{ mAdc}$)	f_T	300	550	—	—	550	—	MHz
Emitter-Base Capacitance ($V_{EB} = 3.0 \text{ Vdc}$, $I_E = 0$)	C_{eb}	—	0.6	—	—	0.6	—	pF
Collector-Base Capacitance ($V_{CB} = 3.0 \text{ Vdc}$, $I_C = 0$)	C_{cb}	—	0.58	—	—	0.58	—	pF
Collector-Substrate Capacitance ($V_{CS} = 3.0 \text{ Vdc}$, $I_C = 0$)	C_{CI}	—	2.8	—	—	2.8	—	pF

TYPICAL CHARACTERISTICS

FIGURE 1 – COLLECTOR CUTOFF CURRENT
versus TEMPERATURE (Each Transistor)

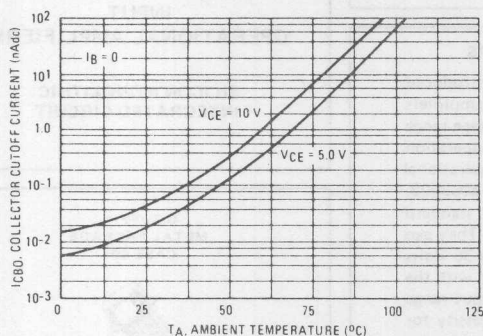


FIGURE 2 – COLLECTOR CUTOFF CURRENT
versus TEMPERATURE (Each Transistor)

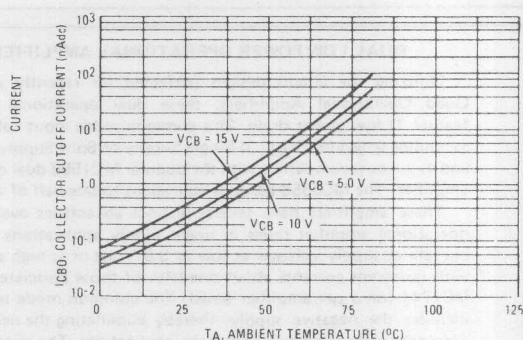


FIGURE 3 – INPUT OFFSET CHARACTERISTICS FOR
Q1 and Q2

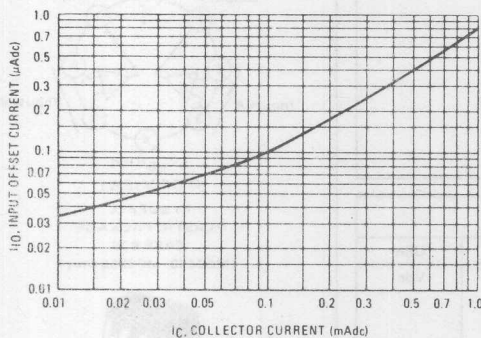


FIGURE 4 – BASE-EMITTER AND INPUT OFFSET
VOLTAGE CHARACTERISTICS

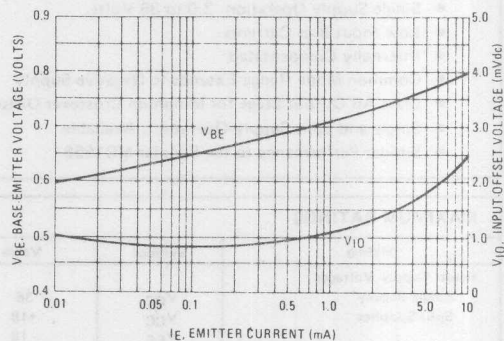
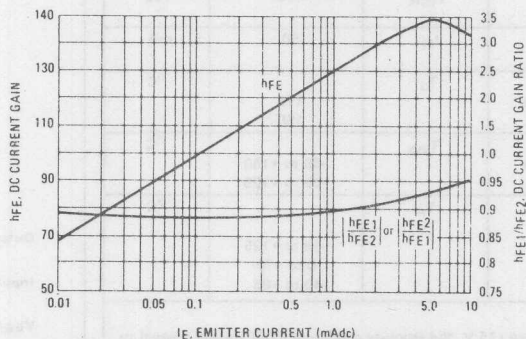


FIGURE 5 – DC CURRENT GAIN



ORDERING INFORMATION

Device	Temperature Range	Package
MC3358P1	-40°C to +85°C	Plastic DIP
MC3458G	0°C to +70°C	Metal Can
MC3458P1	0°C to +70°C	Plastic DIP
MC3458U	0°C to +70°C	Ceramic DIP
MC3558G	-55°C to +125°C	Metal Can
MC3558U	-55°C to +125°C	Ceramic DIP

Specifications and Applications Information

DUAL LOW POWER OPERATIONAL AMPLIFIERS

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/ V_{EE} , 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The MC3558 Series is equivalent to one-half of a MC3503.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1558

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	36	
Split Supplies	V_{CC} V_{EE}	+18 -18	
Input Differential Voltage Range (1)	V_{IDR}	± 30	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	± 15	Vdc
Input Forward Current ($V_I < -0.3$ V)	I_{IF}	50	mA
Junction Temperature	T_J		°C
Ceramic and Metal Packages		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150 -55 to +125	°C
Operating Ambient Temperature Range	T_A		°C
MC3558		-55 to +125	
MC3458		0 to +70	
MC3358		-40 to +85	

(1) Split Power Supplies.

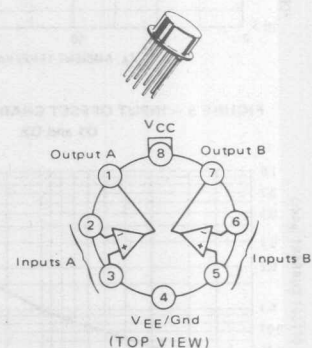
(2) For Supply Voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

MC3458
MC3558
MC3358

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

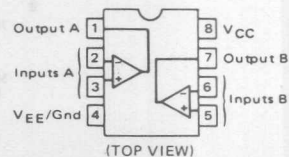
G SUFFIX
METAL PACKAGE
CASE 601



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3458, MC3358 only)



U SUFFIX
CERAMIC PACKAGE
CASE 693



(For MC3558, MC3458, $V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.) (For MC3358, $V_{CC} = +14\text{ V}$, $V_{EE} = \text{Gnd}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = T_{\text{high}} \text{ to } T_{\text{low}} (1)$	V_{IO}	—	2.0	5.0 6.0	—	2.0	10 12	—	2.0	8.0 10	mV
Input Offset Current $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	I_{IO}	—	30	50 200	—	30	50 200	—	30	75 250	nA
Large Signal Open Loop Voltage Gain $V_O = +10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	A_{VOL}	50 25	200 300	—	20 15	200	—	20 15	200	—	V/mV
Input Bias Current $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	I_{IB}	—	-200 -300	-500 -1500	—	-200 -500	-800	—	-200 -500	-500 -1000	nA
Output Impedance $f = 20\text{ Hz}$	Z_o	—	75	—	—	75	—	—	75	—	Ω
Input Impedance $f = 20\text{ Hz}$	Z_i	0.3	1.0	—	0.3	1.0	—	0.3	1.0	—	M Ω
Output Voltage Range $R_L = 10\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$, $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	V_{OR}	-12 -10 -10	-13.5 -13	—	-12 -10 -10	-13.5 -13	—	12 10 10	12.5 12	—	V
Input Common Mode Voltage Range	V_{ICR}	+13 V - V_{EE}	+13.5 V - V_{EE}	—	+13 V - V_{EE}	+13.5 V - V_{EE}	—	+12 V - V_{EE}	+12.5 V - V_{EE}	—	V
Common Mode Rejection Ratio $R_{IS} = 10\text{ k}\Omega$	CMRR	70	90	—	70	90	—	70	90	—	dB
Power Supply Current ($V_O = 0$) $R_L = \infty$	I_{CC} / I_{EE}	—	1.6	2.2	—	1.6	3.7	—	1.6	3.7	mA
Individual Output Short Circuit Current (2)	I_{OS}	-10	-30	-45	-10	-20	-45	-10	-30	-45	mA
Positive Power Supply Rejection Ratio	PSRR+	—	30	150	—	30	150	—	30	150	$\mu\text{V/V}$
Negative Power Supply Rejection Ratio	PSRR-	—	30	150	—	30	150	—	—	—	$\mu\text{V/V}$
Average Temperature Coefficient of Input Offset Current $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	I_{IO}/T	—	50	—	—	50	—	—	50	—	pA/ $^\circ\text{C}$
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{\text{high}} \text{ to } T_{\text{low}}$	V_{IO}/T	—	10	—	—	10	—	—	10	—	$\mu\text{V}/^\circ\text{C}$
Power Bandwidth $A_V = 1$, $R_L = 2.0\text{ k}\Omega$, $V_O = 20\text{ Vip-p}$, THD = 5%	BWp	—	9.0	—	—	9.0	—	—	9.0	—	kHz
Small Signal Bandwidth $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	BW	—	1.0	—	—	1.0	—	—	1.0	—	MHz
Slew Rate $A_V = 1$, $V_i = -10\text{ V to } +10\text{ V}$	SR	—	0.6	—	—	0.6	—	—	0.6	—	V/ μs
Rise Time $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	t_{RLH}	—	0.35	—	—	0.35	—	—	0.35	—	μs
Fall Time $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	t_{THL}	—	0.35	—	—	0.35	—	—	0.35	—	μs
Overshoot $A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$	OS	—	20	—	—	20	—	—	20	—	%
Phase Margin $A_V = 1$, $R_L = 2.0\text{ k}\Omega$, $C_L = 200\text{ pF}$	ϕ_m	—	60	—	—	60	—	—	60	—	Degrees
Crossover Distortion ($V_{in} = 30\text{ mVp-p}$, $V_{out} = 2.0\text{ Vp-p}$, $f = 10\text{ kHz}$)	—	—	1.0	—	—	1.0	—	—	1.0	—	%

(1) $T_{\text{high}} = 125^\circ\text{C}$ for MC3558, 70°C for MC3458, 85°C for MC3358

$T_{\text{low}} = -55^\circ\text{C}$ for MC3558, 0°C for MC3458, -40°C for MC3358

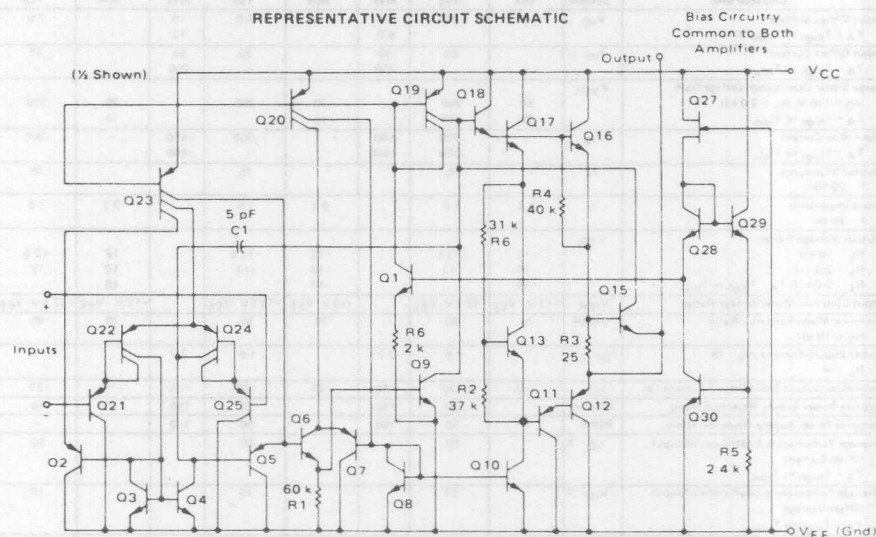
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $V_{EE} = \text{Gnd}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	2.0	5.0	—	2.0	10	—	2.0	10	mV
Input Offset Current	I_{IO}	—	30	50	—	30	50	—	—	75	nA
Input Bias Current	I_{IB}	—	-200	-500	—	-200	-500	—	—	-500	nA
Large Signal Open-Loop Voltage Gain $R_L = 2.0\text{ k}\Omega$	A_{VOL}	20	200	—	20	200	—	20	200	—	V/mV
Power Supply Rejection Ratio	PSRR	—	—	150	—	—	150	—	—	150	$\mu\text{V/V}$
Output Voltage Range (3) $R_L = 10\text{ k}\Omega$, $V_{CC} = 5.0\text{ V}$ $R_L = 10\text{ k}\Omega$, $5.0\text{ V} < V_{CC} < 30\text{ V}$	V_{OR}	3.3 —	3.5 $V_{CC} - 1.7\text{ V}$	—	3.3 —	3.5 $V_{CC} - 1.7\text{ V}$	—	3.3 —	3.5 $V_{CC} - 1.7\text{ V}$	—	Vp-p
Power Supply Current	I_{CC}	—	2.5	4.0	—	2.5	7.0	—	2.5	4.0	mA
Channel Separation ($f = 1.0\text{ kHz to } 20\text{ kHz}$ (Input Referenced))	—	—	-120	—	—	-120	—	—	-120	—	dB

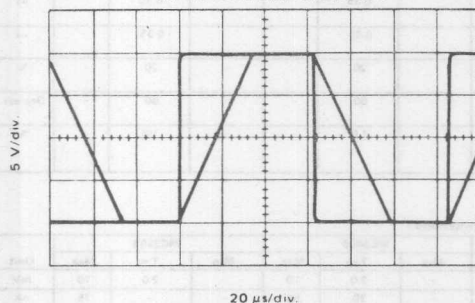
(2) Not to exceed maximum package power dissipation.

(3) Output will swing to ground.

REPRESENTATIVE CIRCUIT SCHEMATIC



INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

The MC3558 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

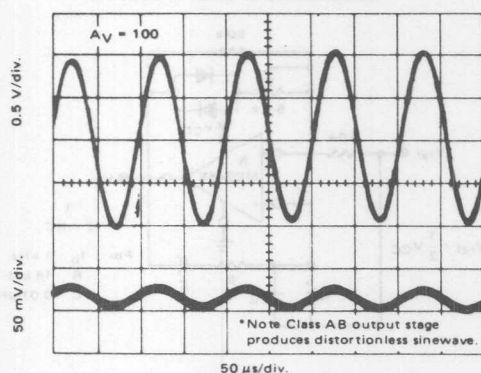


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

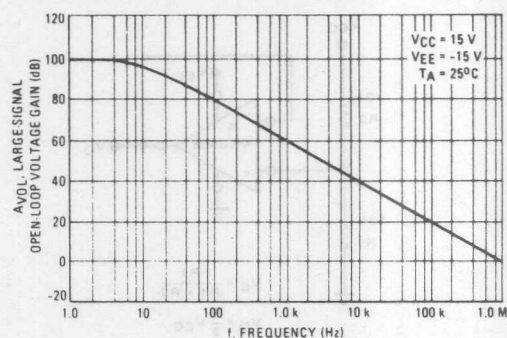


FIGURE 3 – POWER BANDWIDTH

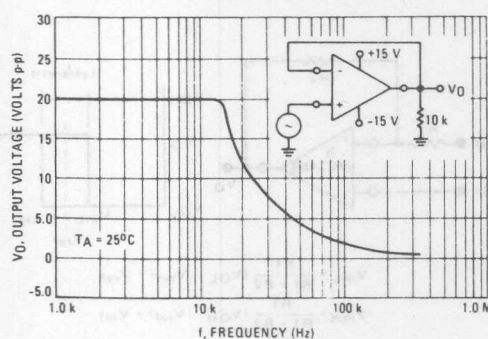


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

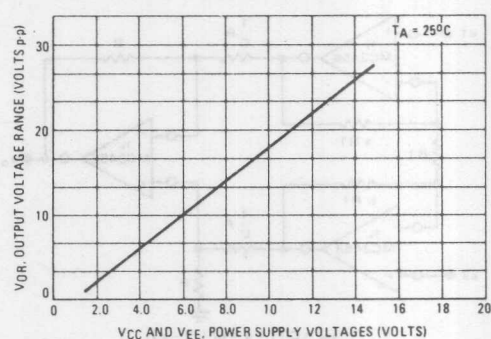


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

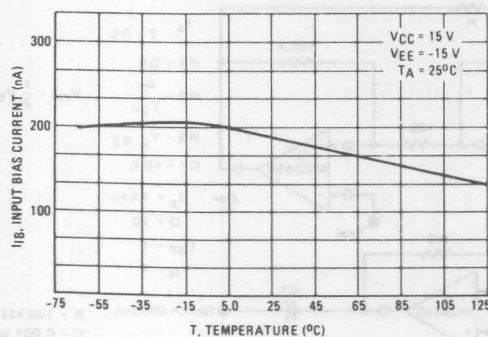
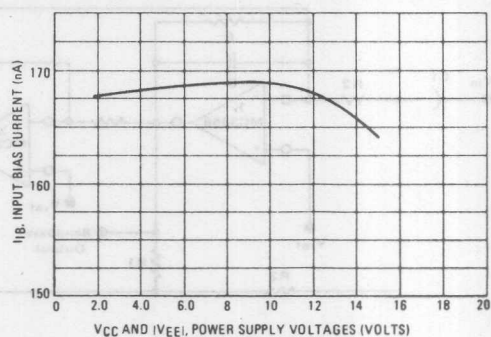


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 7 - VOLTAGE REFERENCE

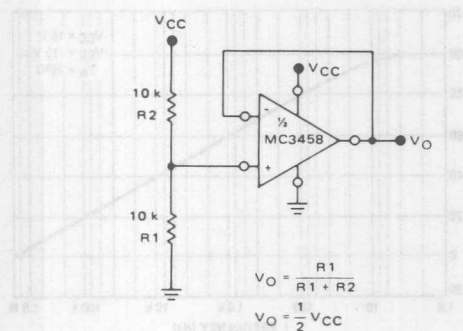


FIGURE 8 - WIEN BRIDGE OSCILLATOR

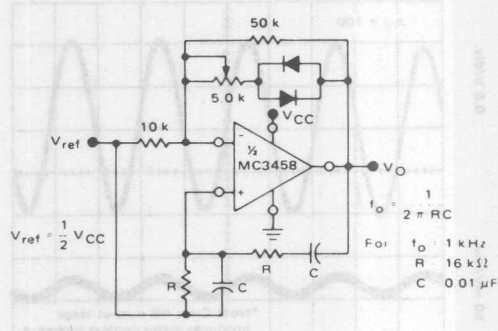


FIGURE 9 - HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER

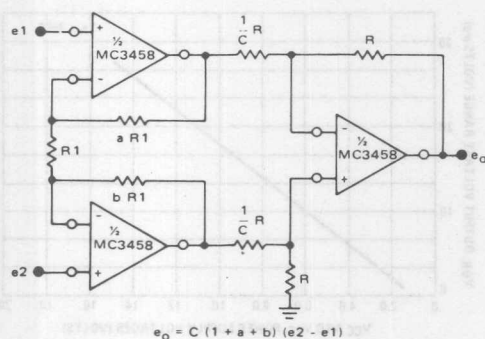


FIGURE 10 - COMPARATOR WITH HYSTERESIS

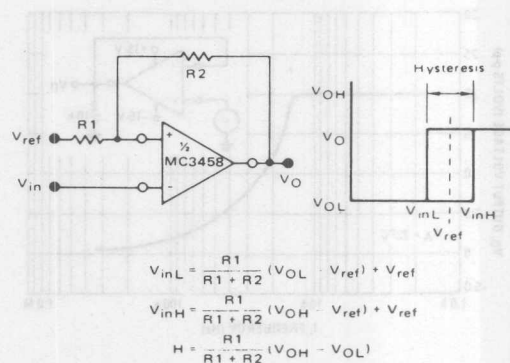
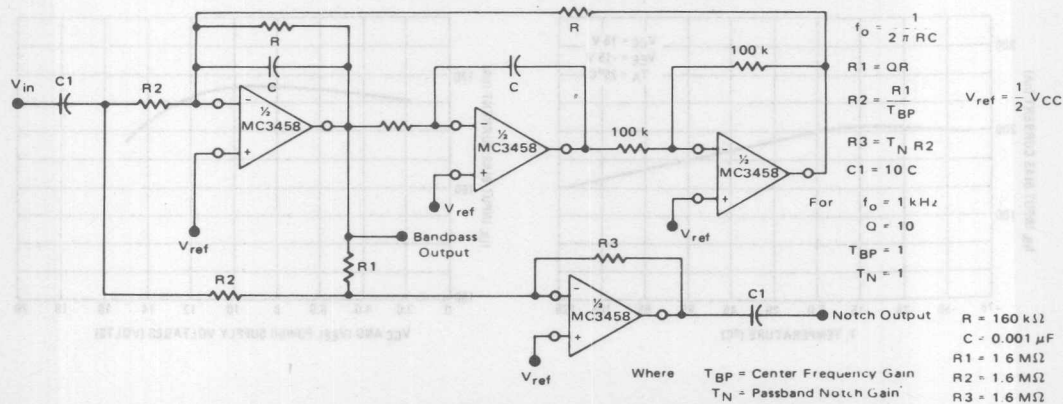


FIGURE 11 - BI-QUAD FILTER



MC3458, MC3558, MC3358

APPLICATIONS INFORMATION (continued)

FIGURE 12 - FUNCTION GENERATOR

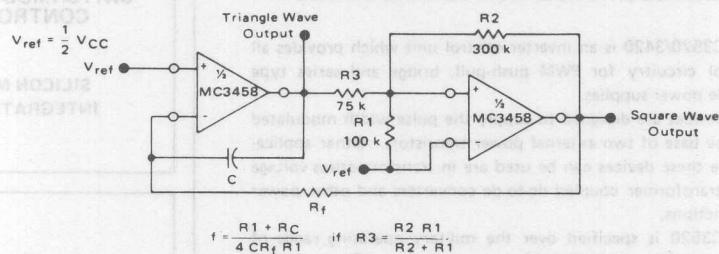
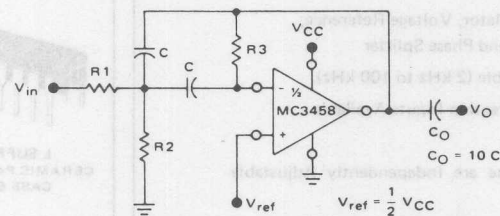


FIGURE 13 - MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
 $A(f_o)$ = Gain at Center Frequency

Choose Value f_o , C

Then

$$R3 = \frac{Q}{\pi f_o C}$$

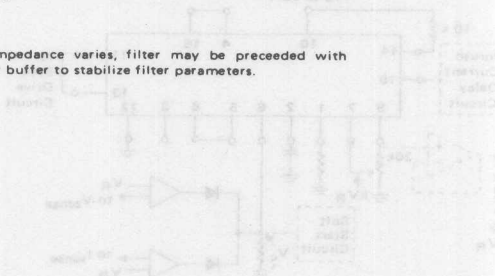
$$R1 = \frac{R3}{2 A(f_o)}$$

$$R2 = \frac{R1 R3}{4 Q^2 R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1 \quad \text{Where } f_o \text{ and } BW \text{ are expressed in Hz.}$$

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.



MC3420 MC3520

SWITCHMODE REGULATOR CONTROL CIRCUIT

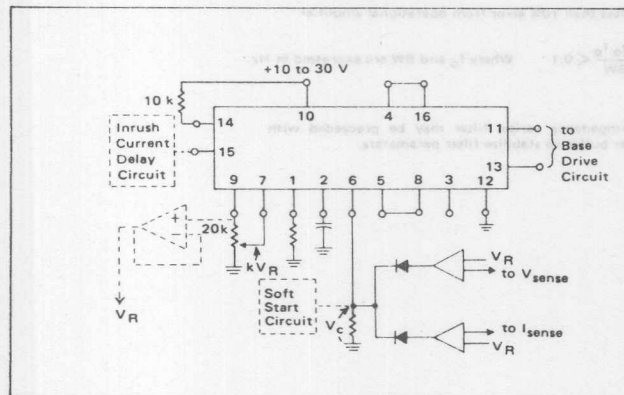
The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

These devices are designed to supply the pulse width modulated drive to the base of two external power transistors. Other applications where these devices can be used are in transformerless voltage doublers, transformer coupled dc-to-dc converters and other power control functions.

The MC3520 is specified over the military operating range of -55°C to $+125^{\circ}\text{C}$. The MC3420 is specified from 0°C to $+70^{\circ}\text{C}$.

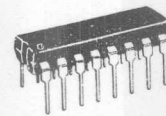
- Includes Symmetrical Oscillator
- On Chip Pulse Width Modulator, Voltage Reference, Dead Time Comparator, and Phase Splitter
- Output Frequency Adjustable (2 kHz to 100 kHz)
- Inhibit and Symmetry Correction Inputs Available
- Controlled Start-Up
- Frequency and Dead Time are Independently Adjustable (0% to 100%)
- Can be Slaved to Other MC3420s
- Open Collector Outputs
- Output Capability 50 mA (Max.)
- On Chip Protection Against Double Pulsing of Same Output During Load Transient Condition

FIGURE 1—TYPICAL APPLICATION

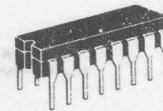


SWITCHMODE REGULATOR CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUITS

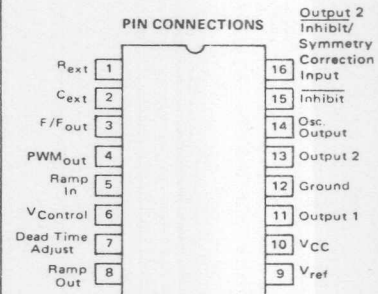


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3420P	0 to $+70^{\circ}\text{C}$	Plastic DIP
MC3420L	0 to $+70^{\circ}\text{C}$	Ceramic DIP
MC3520L	-55 to $+125^{\circ}\text{C}$	Ceramic DIP

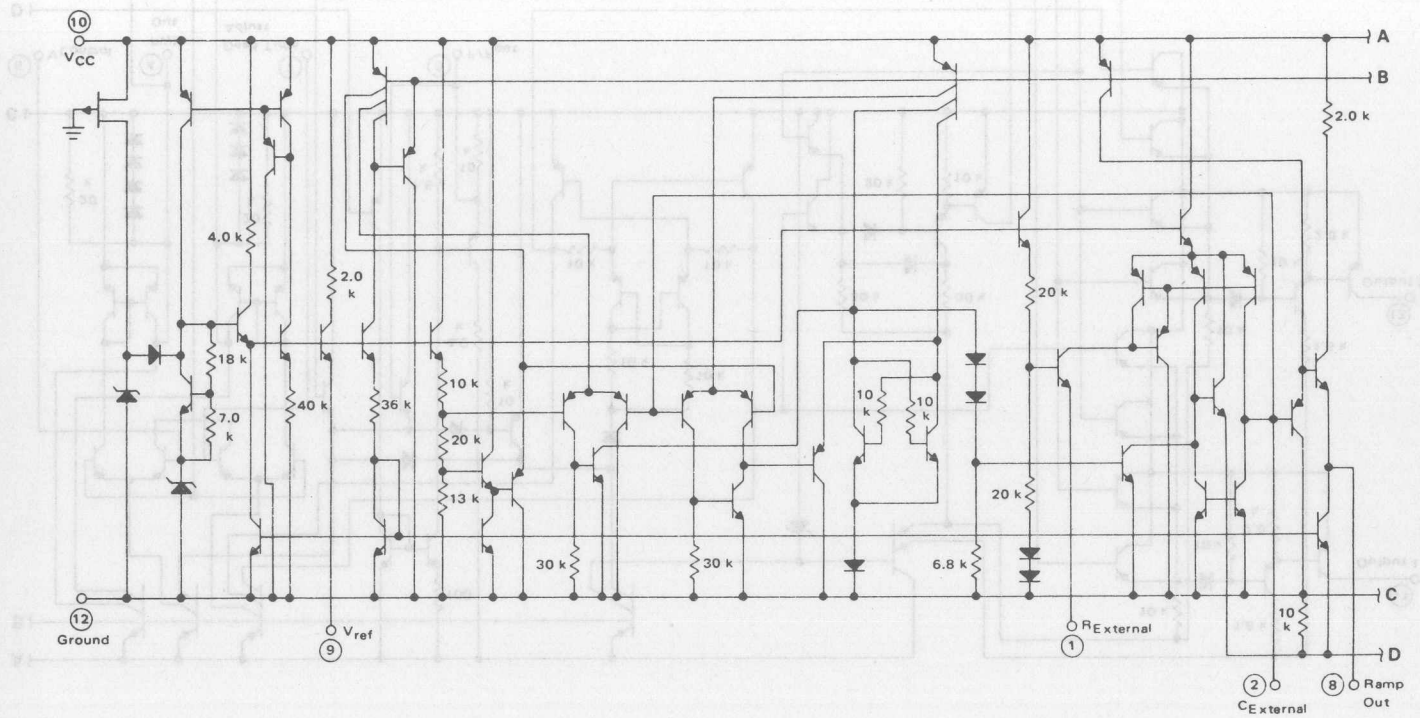
MAXIMUM RATINGS

Rating	Symbol	MC3520	MC3420	Unit
Power Supply Voltage	V_{CC}	30		V
Output Voltage (pins 11 and 13)	V_{out}	40		V
Oscillator Output Voltage (pin 14)	V_{14}	30		V
Voltage at pin 4	V_4	2.0		V
Voltage at pins 3 and 8	V_3, V_8	5.0		V
Voltage at pin 5	V_5	7.0		V
Power Dissipation	P_D	See Thermal Information		
Operating Junction Temperature	T_J			$^{\circ}\text{C}$
Plastic Package		—	125	
Ceramic Package		150	150	
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	$^{\circ}\text{C}$

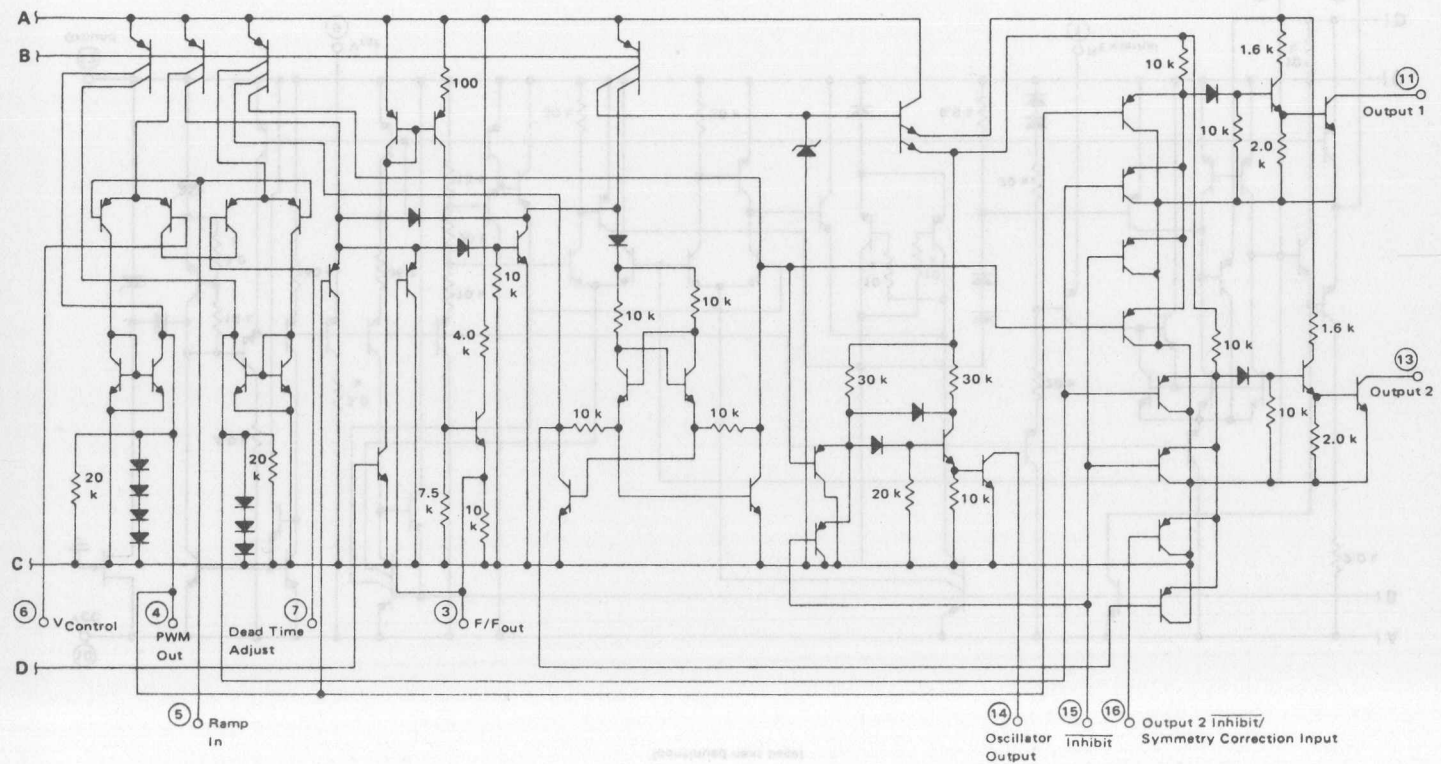
ELECTRICAL CHARACTERISTICS ($V_{CC} = 10$ to 30 V, $T_A = 25^{\circ}\text{C}$ unless otherwise noted.)

Characteristic	Figure	Symbol	MC3520			MC3420			Unit
			Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION									
Reference Voltage ($I_{ref} = 400 \mu A$)	5	V_{ref}	7.6	7.8	8.0	7.4	7.8	8.2	V
Temperature Coefficient of Reference Voltage ($V_{CC} = 15 \text{ V}$, $I_{ref} = 400 \mu A$)	5	TCV_{ref}	—	0.008	0.03	—	0.008	0.03	%/ $^{\circ}C$
Input Regulation of Reference Voltage ($I_{ref} = 400 \mu A$) ($I_{ref} = 1.0 \text{ mA}$)	5	$Reg_{(in)}$	— —	3.0 5.0	7.5 —	— —	4.0 5.0	7.5 —	mV/V
DC SUPPLY SECTION									
Supply Voltage	5	V_{in}	10	—	30	10	—	30	V
Supply Current ($R_{ext} = 10 \text{ k}\Omega$, excluding load and current and reference current)	5	I_D	—	—	16	—	—	22	mA
OSCILLATOR SECTION									
Line Frequency Stability ($f = 20 \text{ kHz}$) ($f = 20 \text{ kHz}$, $V_{CC} = 15 \text{ V}$, T_{low} to T_{high})	5	Δf Δf	— —	— 0.03	3.0 —	— —	— 0.04	5.0 —	% %/ $^{\circ}C$
Maximum Output Frequency ($V_{CC} = 15 \text{ V}$)	6	f_{max}	100	200	—	100	200	—	kHz
Minimum Output Frequency ($V_{CC} = 15 \text{ V}$)	6	f_{min}	—	2.0	5.0	—	2.0	5.0	kHz
Oscillator Output Saturation Voltage ($I_{14 \text{ sink}} = 5.0 \text{ mA}$)	11	$V_{osc(sat)}$	—	0.2	0.5	—	0.2	0.5	V
OUTPUT SECTION									
Output Saturation Voltage ($I_L = 40 \text{ mA}$, T_{high} to T_{low}) ($I_L = 25 \text{ mA}$, T_{high} to T_{low})	7	$V_{CE(sat)}$	— —	0.33 0.22	0.5 —	— —	0.33 0.22	0.5 —	V
Output Leakage Current ($V_{CE} = 40 \text{ V}$, pins 11 and 13)	8	I_{CE}	—	—	50	—	—	50	μA
COMPARATOR SECTION									
Pulse Width Adjustment Range	9	ΔPW	0	—	100	0	—	100	%
Dead Time Adjustment Range	9	ΔDDT	0	—	100	0	—	100	%
Temperature Coefficient of Dead Time	—	$TCDDT$	—	0.1	—	—	0.1	—	%/ $^{\circ}C$
Comparator Bias Currents	12, 13 14	I_{IB} I_{IB}	— —	5.0 10	15 30	— —	5.0 10	15 30	μA

FIGURE 3 - CIRCUIT SCHEMATIC
(continued next page)



(continued) FIGURE 3 - CIRCUIT SCHEMATIC



GENERAL INFORMATION

The internal block diagram of the MC3420 is shown in Figure 2, and consists of the following sections:

Voltage Reference

A stable reference voltage is generated by the MC3420 primarily for internal use. However, it is also available externally at Pin 9 (V_{ref}) for use in setting the dead time (Pin 7) and for use as a reference for the external control loop error amplifiers.

Ramp Generator

The ramp generator section produces a symmetrical triangular waveform ramping between 2.4 V and 6.0 V, with frequency determined by an external resistor (R_{ext}) and capacitor (C_{ext}) tied from Pins 1 and 2, respectively, to ground.

PWM Comparator

The output of the ramp generator at pin 8 is normally connected to Pin 5, RAMP IN. The PWM (pulse width modulation) comparator compares the voltage at Pin 6 ($V_{control}$) to the ramp generator output. The level of $V_{control}$ determines the outputs' pulse width or duty cycle. The duty cycle of each output can vary, exclusive of dead time, from 50% (when $V_{control}$ is at approximately 2.4 V) to 0% ($V_{control}$ approximately 6.0 V).

Dead Time Comparator

An additional comparator has been included in MC3420 to allow independent adjustment of system dead time or maximum duty cycle. By dividing down V_{ref} at Pin 9 with a resistive divider or potentiometer, and applying this voltage to Pin 7, a stable dead time is obtained for prevention of inverter switching transistor cross conduction at high duty cycles due to storage time delays.

Phase Splitter

A phase splitter is included to obtain two 180° out of phase outputs for use in multiple transistor inverter systems. It consists of a toggle flip-flop whose clock signal is derived by "ANDing" the output of the PWM comparator and a signal from the ramp generator section. This "AND" gate ensures that the outputs truly alternate under control loop transient conditions. Better understanding of this feature and MC3420 operation may be gained by studying the circuit waveforms, shown in Figure 4.

FIGURE 4 - INTERNAL WAVEFORMS

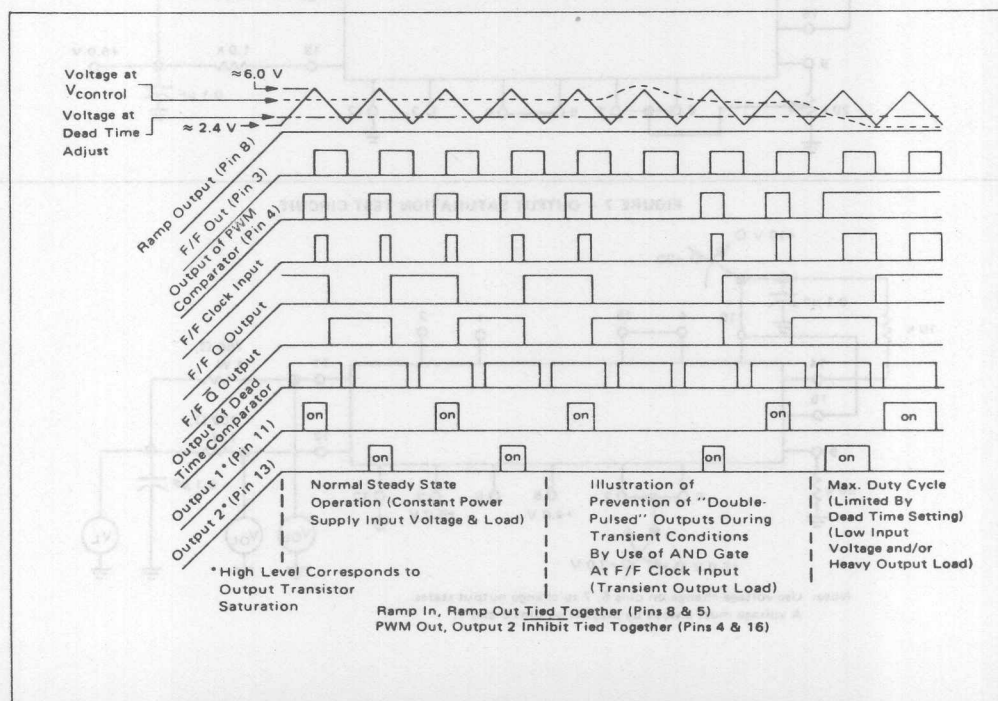


FIGURE 8 - OUTPUT LEAKAGE TEST CIRCUIT

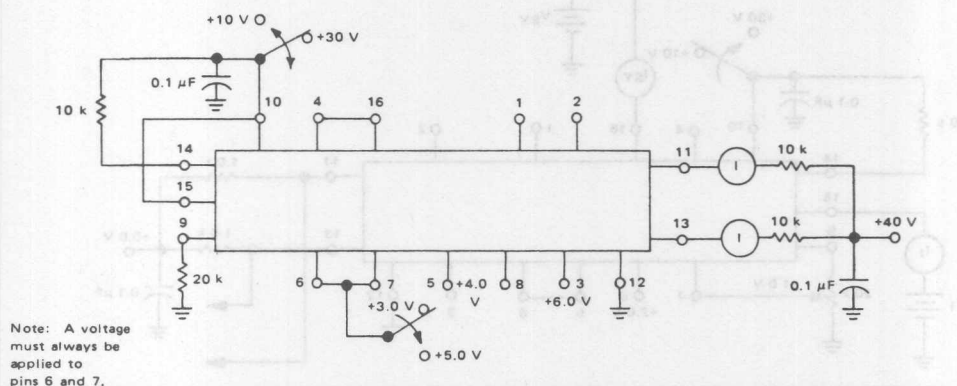
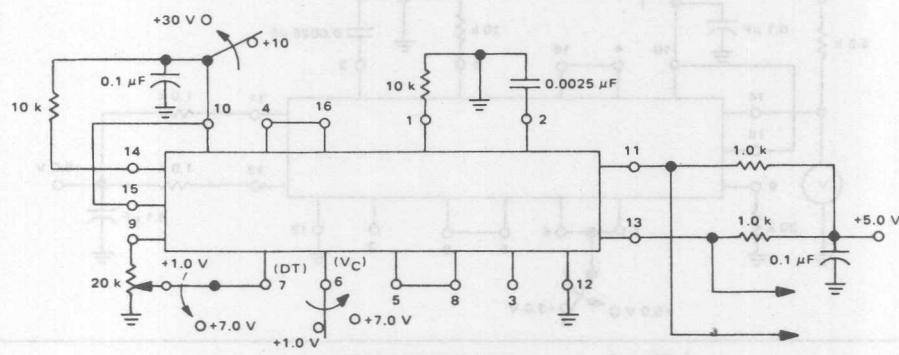


FIGURE 9 - OUTPUT DUTY CYCLE TEST CIRCUIT



TYPICAL DUTY CYCLE versus DEAD TIME VOLTAGE		TYPICAL DUTY CYCLE versus PWM VOLTAGE (V_{control})	
PIN 7. DEAD TIME VOLTAGE (V) ($V_{\text{control}} = 2.0 \text{ V}$)	% DUTY CYCLE (FOR EACH OUTPUT)	PIN 6. V_{control} (V) (DEAD TIME VOLTAGE = 1.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)
2.0	50	2.0	50
2.5	46	2.5	46
3.0	40	3.0	40
3.5	33	3.5	33
4.0	26	4.0	26
4.5	18	4.5	18
5.0	11	5.0	11
5.5	4.0	5.5	4.0
6.0	0	6.0	0

	V_6	V_7	
	Volts		
100% Adjust			
Dead Time	1.0	1.0	(Pin 11 + Pin 13 = Logic "1")
Pulse Width	1.0	1.0	
0% Adjust			
Dead Time	7.0	1.0	(Pin 11)(Pin 13) = Logic "1"
Pulse Width	1.0	7.0	

NOTE: Logic "1" is TTL-Compatible V_{OH} .

FIGURE 10 – INHIBIT/SYMMETRY TEST CIRCUIT

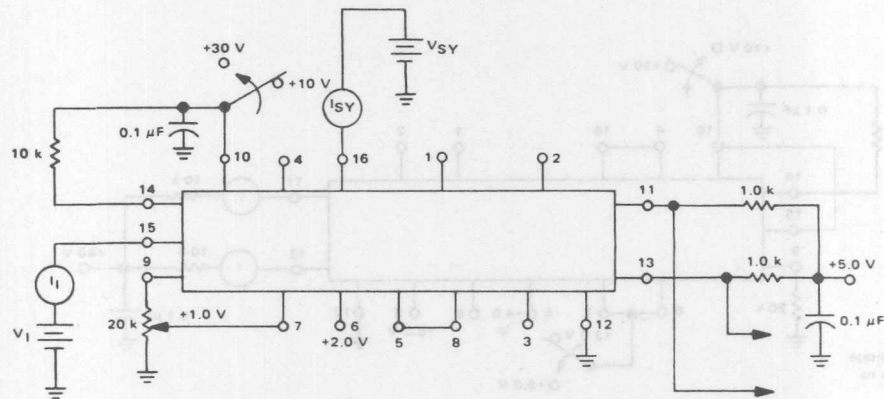


FIGURE 11 – OSCILLATOR OUTPUT (pin 14) TEST CIRCUIT

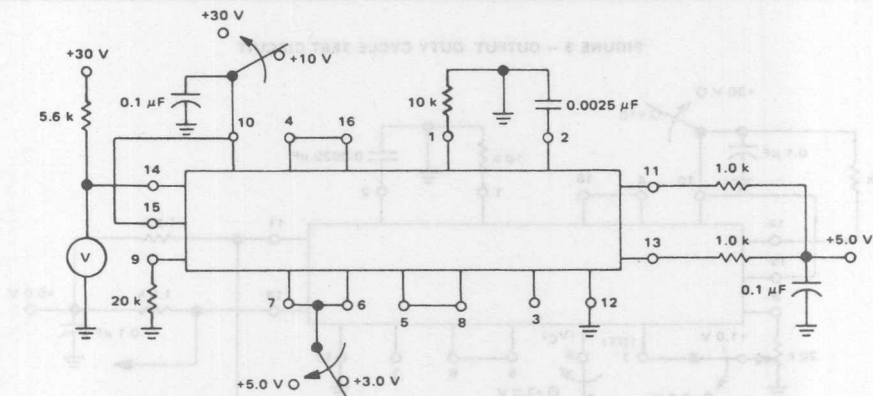


FIGURE 12 – $V_{Control}$ BIAS CURRENT TEST CIRCUIT

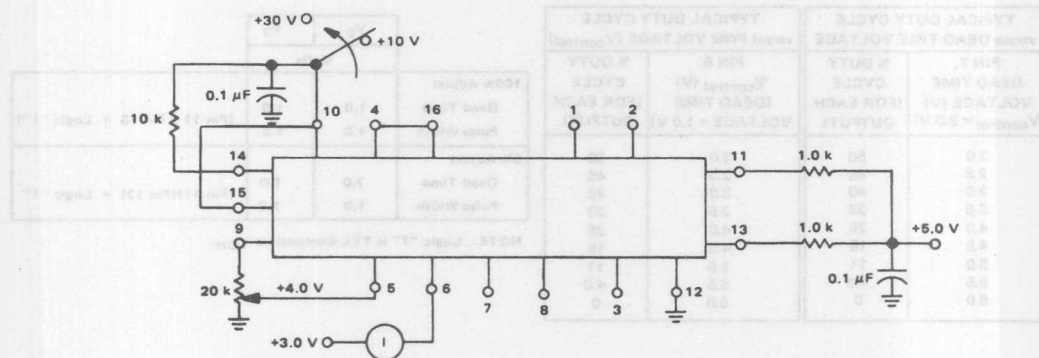


FIGURE 13 – DEAD TIME BIAS CURRENT TEST CIRCUIT

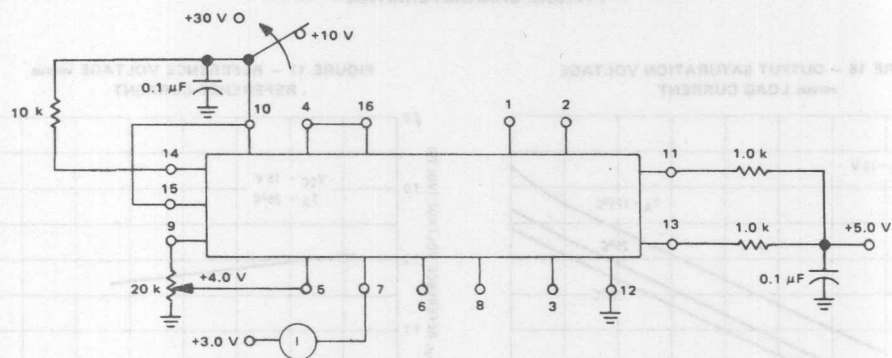


FIGURE 14 – RAMP IN BIAS CURRENT TEST CIRCUIT

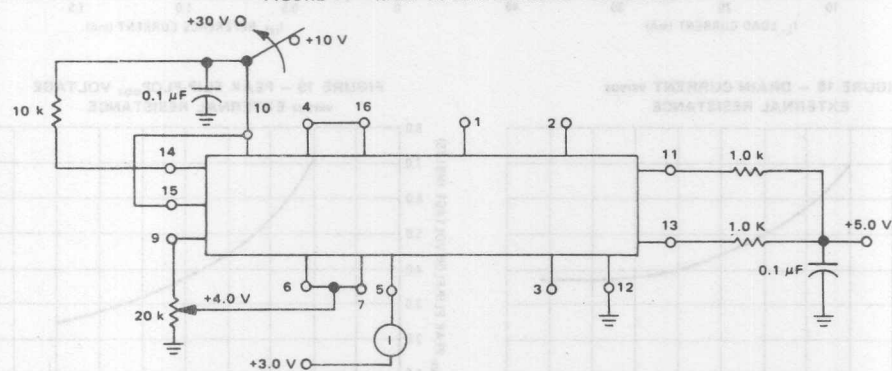
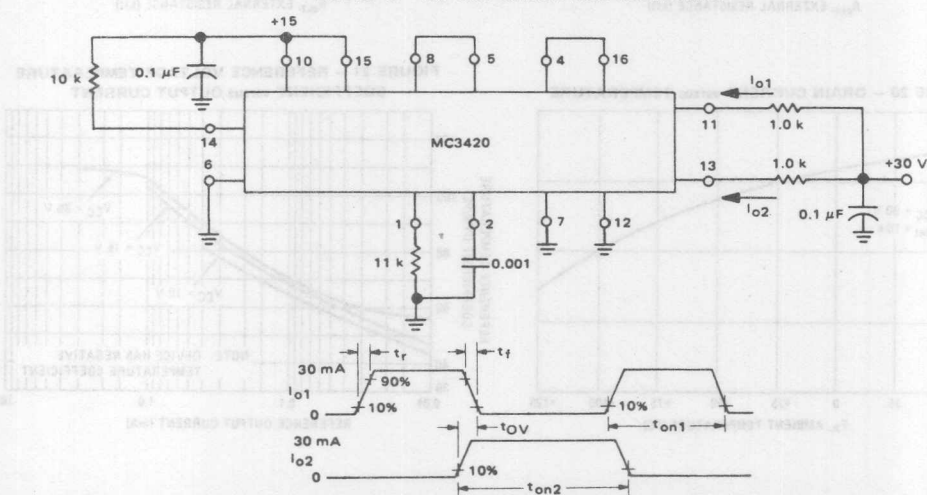


FIGURE 15 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL CHARACTERISTICS

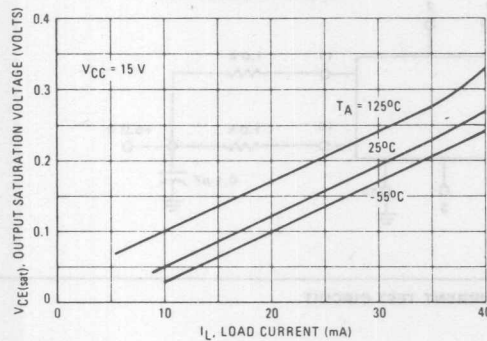
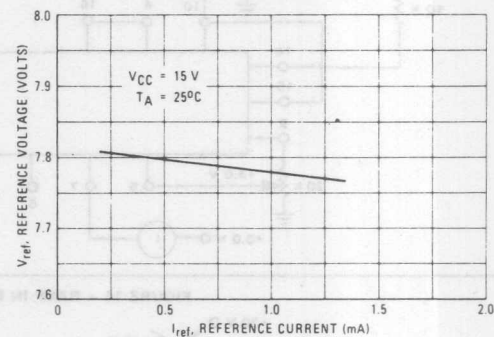
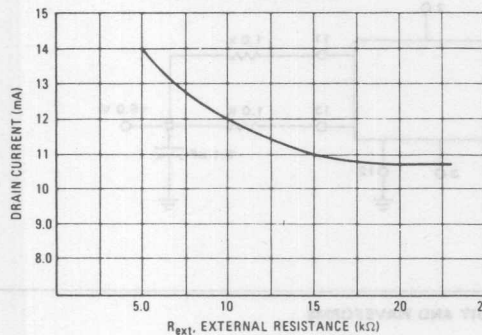
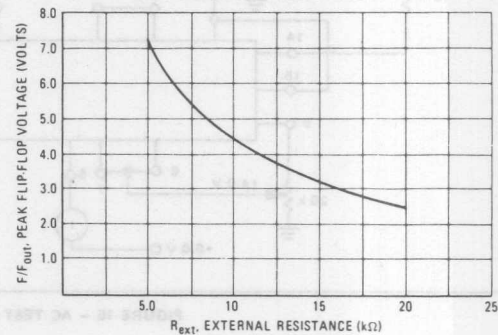
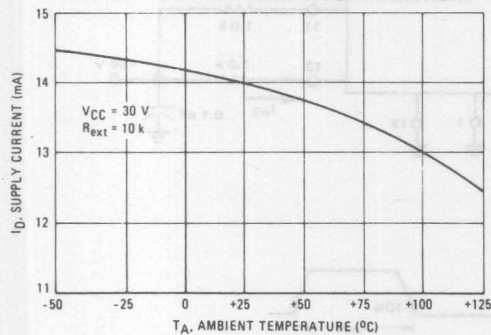
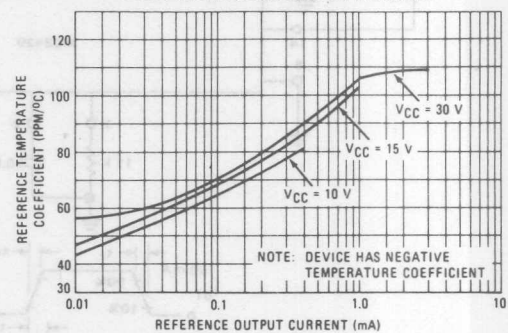
FIGURE 16 – OUTPUT SATURATION VOLTAGE
versus LOAD CURRENTFIGURE 17 – REFERENCE VOLTAGE versus
REFERENCE CURRENTFIGURE 18 – DRAIN CURRENT versus
EXTERNAL RESISTANCEFIGURE 19 – PEAK FLIP-FLOP_{out} VOLTAGE
versus EXTERNAL RESISTANCE

FIGURE 20 – DRAIN CURRENT versus TEMPERATURE

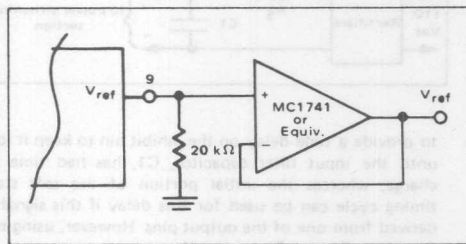
FIGURE 21 – REFERENCE VOLTAGE TEMPERATURE
COEFFICIENT versus OUTPUT CURRENT

OPERATION AND APPLICATIONS INFORMATION

The Voltage Reference

The temperature coefficient of V_{ref} has been optimized for a $400\ \mu A$ ($\approx 20\ k\Omega$) load. If increased current capability is required, an op amp buffer may be used, as shown in Figure 22.

FIGURE 22



Output Frequency

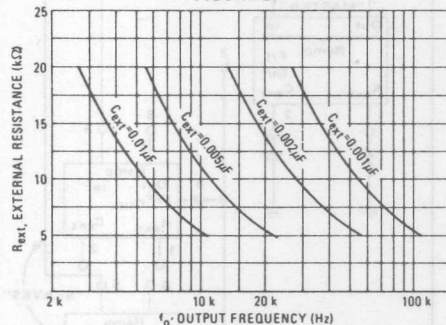
The values of R_{ext} and C_{ext} for a given output frequency, f_o , can be found from:

$$f_o \approx \frac{0.55}{R_{ext} C_{ext}}; 5.0\ k\Omega \leq R_{ext} \leq 20\ k\Omega \text{ (Eq. 1)}$$

or from the graph shown in Figure 23.

Note that f_o refers to the frequency of Output 1 (Pin 11) or Output 2 (Pin 13). The frequency of the ramp generator output waveform at Pin 8 will be twice f_o .

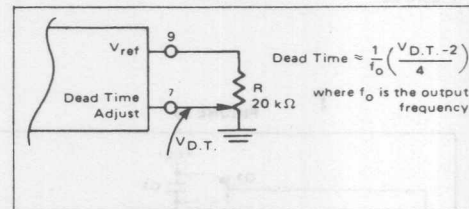
FIGURE 23



Dead Time

Figure 24 illustrates how to set or adjust the MC3420 outputs' dead time or maximum duty cycle. For minimum dead time drift with temperature or supply voltage, $V_{D.T.}$ should be derived from V_{ref} as shown.

FIGURE 24

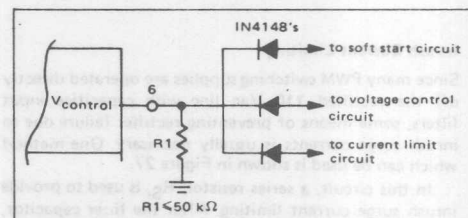
Connections to the $V_{control}$ Pin

In many systems, it is necessary to make multiple connections to the $V_{control}$ Pin in order to implement features in addition to voltage regulation such as current limiting, soft start, etc. These can be made by the use of a simple "diode-OR" connection, as shown in Figure 25. This allows whichever control element is seeking the lowest PWM duty cycle to dominate. Note that a resistor, $R1$, whose value is $\leq 50\ k\Omega$ is placed from the $V_{control}$ Pin to ground. This is necessary to provide a dc path for the PWM comparator input bias current under all conditions.

The system duty cycle is given by:

$$\text{D.C. (\%)} \approx \frac{V_{control} - 2}{4} \times 100 \text{ (Eq. 2)}$$

FIGURE 25



15 V, 2 A DC-to-DC Converter

Figure 29 illustrates the use of the MC3520 in a PWM switching power supply utilizing a single series switching element (see Appendix for description of PWM switching supply configurations). The series switching transistor, Q1, chops the dc input voltage, V_{in} , at a frequency of ≈ 25 kHz, and the resulting waveform is filtered by L1 and C1 to provide the dc output voltage. The frequency is set by R4 and C3, and since the outputs of the MC3520 are wire-ORed together, f_o is twice that given by Equation 1 and Figure 23. V_o is regulated by comparing its value to the MC3520's reference voltage and amplifying the error voltage with U1. The output of U1 is fed into the MC3520 to provide PWM to Q1, thereby controlling its duty cycle and thus the value of V_o .

C2 provides a soft-start feature during power up to prevent output voltage overshoots and excessive start up currents through Q1.

Short circuit protection is provided by R_{SC} , Q3 and Q4. When an overcurrent condition occurs, Q3 is turned on by the voltage across R_{SC} ; Q3 drives Q4 on, which raises the voltage at pin 6 ($V_{control}$) of the MC3520, reducing Q1's duty cycle and maintaining a constant output current of ≈ 2.5 A.

5 V, 50 A Line-Operated Supply

A 5 V, 50 A line-operated 20 kHz switching power supply using the MC3520 is shown in Figures 30a and b. An explanation of the operation of each section of the supply follows.

Input Section

The 120 Vac line is full wave voltage doubled by CR1, CR2, C1 and C2 to provide 310 Vdc to the power section of the supply. Inrush surge current limiting is provided by R1, which is shorted out of the circuit by Q1 after C1 and C2 are initially charged.

Power Section

The supply utilizes two switching transistors, Q2 and Q3, in a half-bridge configuration (see Appendix) to drive the high frequency power transformer, T2.

The bases of Q2 and Q3 are driven by T3 and T4, respectively, to provide isolation from the control and base drive sections of the supply. CR3, CR5, CR6, and CR8 constitute anti-saturation (Baker) clamps which provide increased and more uniform switching speeds for

Q2 and Q3. CR4 and CR7 allow reverse base currents during turn off.

Output Section

The output of T2 is rectified by Schottky diodes, CR9 and CR10. VR1 is a transient suppressor to protect CR9 and CR10 from transients that might cause reverse breakdown. L1 and C4 constitute the output filter. C4 should have very low ESR (equivalent series resistance) at 20 kHz to provide the most effective filtering. L2 and C5 make up a high-frequency filter to reduce commutation spikes which pass L1 due to its interwinding capacitance. R_{SC} provides output overcurrent sensing to the control section.

Control Section

The MC3520 provides the PWM control for the supply. R2 is adjusted to obtain a 20 kHz operating frequency. R3 adjusts the dead time (≈ 5 μ s each half-cycle). U1A and U1B are the output current and output voltage error amplifiers, respectively. R5 sets the output voltage while R4 determines the output current limit. C7 and C8 are the current and voltage loop compensation capacitors.

C6 provides the soft-start feature while Q4 ensures a soft-start after each system inhibit (pin 15 low).

Base Drive Section

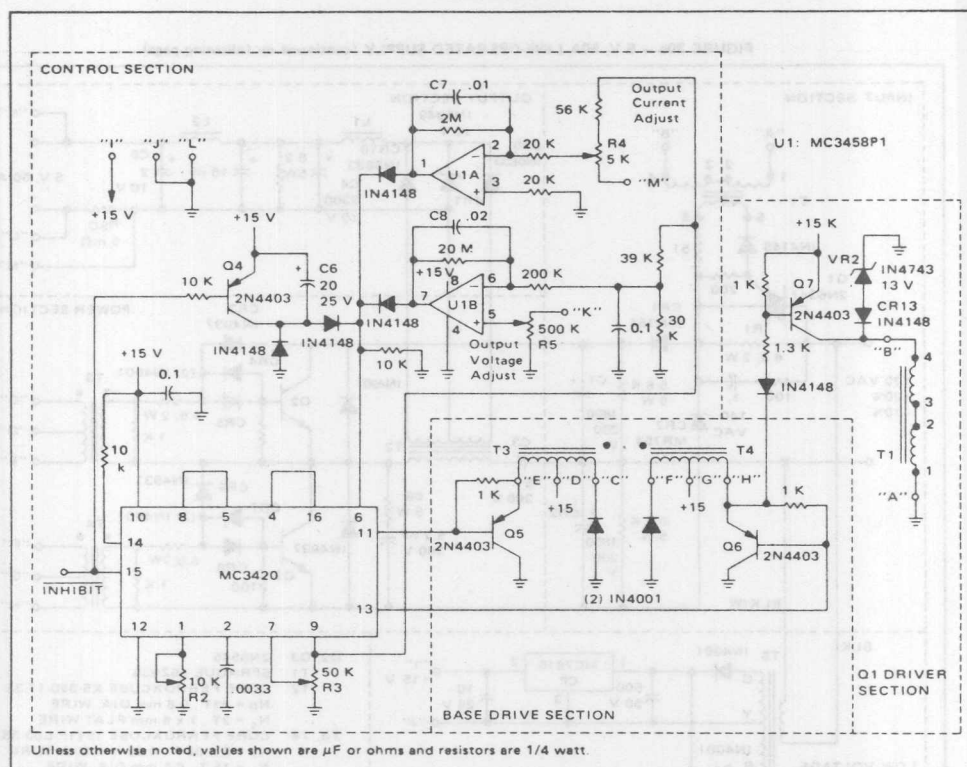
Turn on drive to the power section switching transistors occurs when each of the outputs of the MC3520 saturate. Q5 or Q6 are therefore turned on, and 15 V applied to the primaries of T3 or T4, supplying forward base drive to Q2 or Q3.

Turn off drive occurs when Q5 or Q6 turn off, and the magnetizing energy stored in T3 or T4's core is transformed into a negative "flyback" voltage at their secondaries, providing reverse base drive to Q2 or Q3. CR11 and CR12 act as clamps, to prevent this flyback voltage from exceeding -5 V at T3 or T4's secondary (30 V on Q5 or Q6's collector).

Q1 Driver Section

Q7 and T1 provide the gate drive to Q1. Q7 starts operating after an initial delay of 100 ms created by the soft-start circuit, thereby allowing C1 and C2 to charge up before firing Q1.

FIGURE 30b



APPENDIX: BASIC PWM SWITCHING SUPPLY POWER CIRCUIT CONFIGURATIONS

The material given in this section is intended to acquaint the designer with the basic switching transistor configurations used in PWM power supplies. Circuit configurations, collector voltage and current waveforms of the switching transistors, and required transistor specifications for the most commonly utilized configurations are shown in Figures 1A through 4A. It should be noted that the waveforms and specifications are idealized, in that the effects of leakage inductance voltage spikes, stray circuit capacitance, snubber networks, clamp diode overshoots, diode reverse recovery and saturation voltages have been neglected. For more information on these effects, the configurations, or switching supplies in general, consult the references listed in the References section.

Series Configuration

The single transistor series configuration is shown in Figure 1A. This configuration is usually limited to applications in which $0.2 V_{CC} < V_o < 0.8 V_{CC}$ and where input-output isolation is not required.

Push-Pull Configuration

Figure 2A shows the two-transistor push-pull configuration. Unlike the series configuration, it can be used to either step-up or step-down the input voltage, V_{CC} , and also provides input-output isolation. It does, however, have the disadvantage that additional circuitry must be used to provide symmetry correction for the prevention of transformer saturation.

Half-Bridge Configuration

The half-bridge configuration, shown in Figure 3A, does not suffer from the symmetry problems of the push-pull configuration since the transformer primary is capacitively coupled. This prevents transformer core saturation since no net dc current is allowed to flow in its primary.

Note that for the same input power, bus voltage, and duty cycle, the half-bridge requires switching transistors

which have twice the current and half the voltage requirements as those of the push-pull configuration.

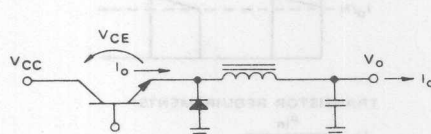
Full-Bridge Configuration

By replacing the bridge capacitors, C , of the half-bridge configuration of Figure 4A results. With this configuration, double the power of the half-bridge configuration can be obtained at the expense of two additional switching transistors and their associated circuitry.

ABBREVIATIONS USED IN FIGURES 1A THROUGH 4A

I_C :	Switching transistor collector current
V_{CE} :	Switching transistor collector-to-emitter-voltage
P_{in} :	Average input power
D.C.:	Inverter duty cycle
V_{CC} :	DC bus voltage
$V_{CEO(sus)}$:	V_{CE} that transistor must withstand during turn-on
V_{CEX} :	V_{CE} that transistor must block during non-conduction period.

FIGURE 1A — SERIES CONFIGURATION



TRANSISTOR REQUIREMENTS*

$$I_C > I_o$$

$$V_{CEO(sus)} \geq V_{CC}$$

$$V_{CEX} \geq V_{CC}$$

*See explanation of abbreviations in text.

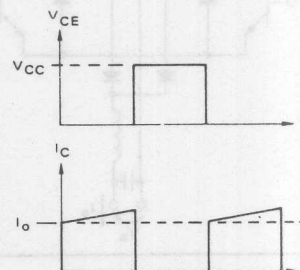
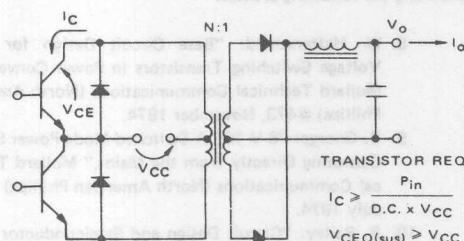


FIGURE 2A — PUSH-PULL CONFIGURATION



TRANSISTOR REQUIREMENTS*

$$I_C > \frac{P_{in}}{D.C. \times V_{CC}}$$

$$V_{CEO(sus)} \geq V_{CC}$$

$$V_{CEX} \geq 2 V_{CC}$$

*See explanation of abbreviations in text.

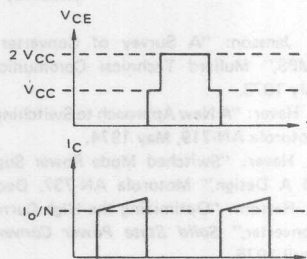
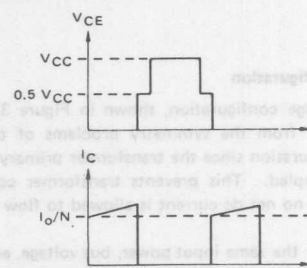
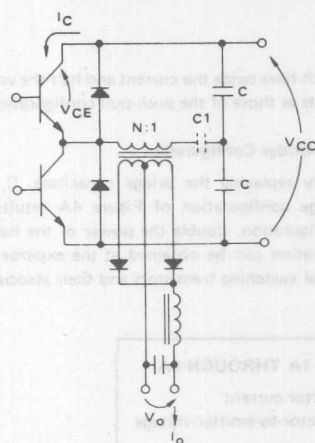


FIGURE 3A — HALF-BRIDGE CONFIGURATION



TRANSISTOR REQUIREMENTS*

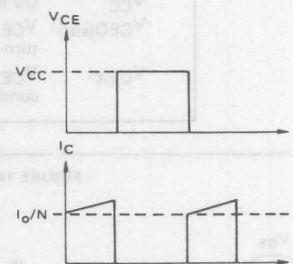
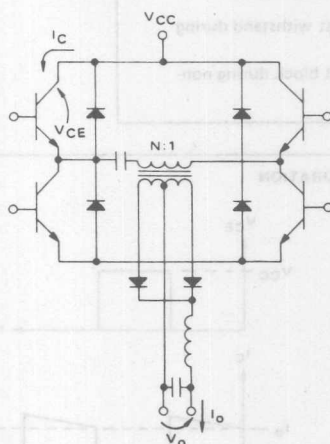
$$I_C \geq \frac{2 \times P_{in}}{D.C. \times V_{CC}}$$

$$V_{CEO(sus)} \geq V_{CC}/2$$

$$V_{CEX} \geq V_{CC}$$

*See explanation of abbreviations in text.

FIGURE 4A — FULL-BRIDGE CONFIGURATION



TRANSISTOR REQUIREMENTS*

$$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$$

$$V_{CEO(sus)} \geq V_{CC}$$

$$V_{CEX} \geq V_{CC}$$

*See explanation of abbreviations in text.

REFERENCES

More detailed information on switching power supplies may be obtained by consulting the following articles:

1. L. Jansson: "A Survey of Converter Circuits for SMPS," Mullard Technical Communications #119, July 1973.
2. R. Haver: "A New Approach to Switching Regulators," Motorola AN-719, May 1974.
3. R. Haver: "Switched Mode Power Supplies, a 5 V, 40 A Design," Motorola AN-737, December 1974.
4. W. Hersom: "Optimizing the High Current Transistor Converter," *Solid State Power Conversion*, March/April 1975.
5. W. Hirshberg: "Simplify Converter Designs with Flyback," *Solid State Power Conversion*, March/April 1975.
6. P. Wood: "Design of a 5 V, 100 Watt Power Supply, TRW AN #122, February 1975.
7. J. Turnbull: "Radio Frequency Interference Suppression in SMPS," Ferroxcube AN-F601.
8. W. Hettterscheid: "Base Circuit Design for High-Voltage Switching Transistors in Power Converters," Mullard Technical Communications (North American Phillips) #473, November 1974.
9. B. George: "6 V 100 A Switched-Mode Power Supply Operating Directly from the Mains," Mullard Technical Communications (North American Phillips) #123, July 1974.
10. B. Bailey: "Circuit Design and Semiconductor Selection for Square-Wave and Sine-Wave Inverters," *Proc. of Powercon 2*, October 1975.
11. B. Bailey: "Safe Reverse Bias Operation—A New Approach," *Proc. of Powercon 3*, June 1976.
12. Gutmann and Suva: "A Line-Operated, Regulated 5 V/50 A Switching Power Supply," Motorola AN-767, September 1976.

MC3423 MC3523

Specifications and Applications Information

OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

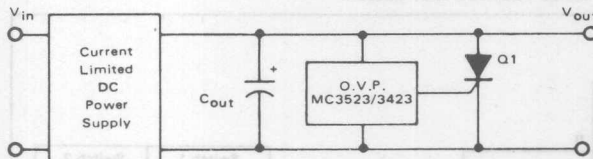
The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423/3523 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Differential Power Supply Voltage	$V_{CC}-V_{EE}$	40	Vdc
Sense Voltage (1)	$V_{Sense 1}$	6.5	Vdc
Sense Voltage (2)	$V_{Sense 2}$	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range MC3423 MC3523	T_A	0 to +70 -55 to +125	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	125 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TYPICAL APPLICATION

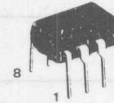


NOTE: A 2N6504 or equivalent is suggested for Q1.

OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

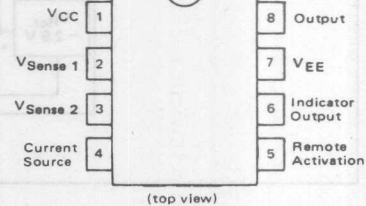
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3423 only)



U SUFFIX
CERAMIC PACKAGE
CASE 693



PIN CONNECTIONS



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3423P1	0 to +70°C	Plastic DIP
MC3423U	0 to +70°C	Ceramic DIP
MC3523U	-55 to +125°C	Ceramic DIP

MC3423, MC3523

ELECTRICAL CHARACTERISTICS (5 V < V_{CC} - V_{EE} ≤ 36 V, T_{low} < T_A < T_{high} unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V _{CC} -V _{EE}	4.5	—	40	Vdc
Output Voltage (I _O = 100 mA)	V _O	V _{CC} -2.2	V _{CC} -1.8	—	Vdc
Indicator Output Voltage (I _O (Ind) = 1.6 mA)	V _{OL} (Ind)	—	0.1	0.4	Vdc
Sense Voltage (T _A = 25°C)	V _{Sense 1} , V _{Sense 2}	2.45	2.6	2.75	Vdc
Temperature Coefficient of V _{Sense 1} (Figure 2)	TCV _{S1}	—	0.06	—	%/°C
Remote Activation Input Current (V _{IH} = 2.0 V, V _{CC} -V _{EE} = 5.0 V) (V _{IL} = 0.8 V, V _{CC} -V _{EE} = 5.0 V)	I _{IH} I _{IL}	— —	5.0 -120	40 -180	μA
Source Current	I _{source}	0.1	0.2	0.3	mA
Output Current Rise Time (T _A = 25°C)	t _r	—	400	—	mA/μs
Propagation Delay (T _A = 25°C)	t _{pd}	—	0.5	—	μs
Supply Current MC3423 MC3523	I _D	— —	6.0 5.0	10 7.0	mA

T_{low} = -55°C for MC3523
= 0°C for MC3423

T_{high} = +125°C for MC3523
= +70°C for MC3423

FIGURE 1 — BLOCK DIAGRAM

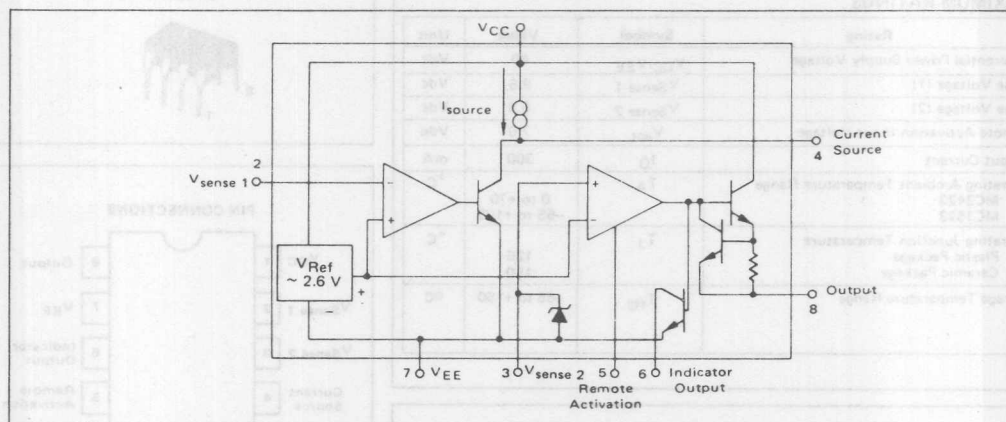


FIGURE 2 — SENSE VOLTAGE TEST CIRCUIT

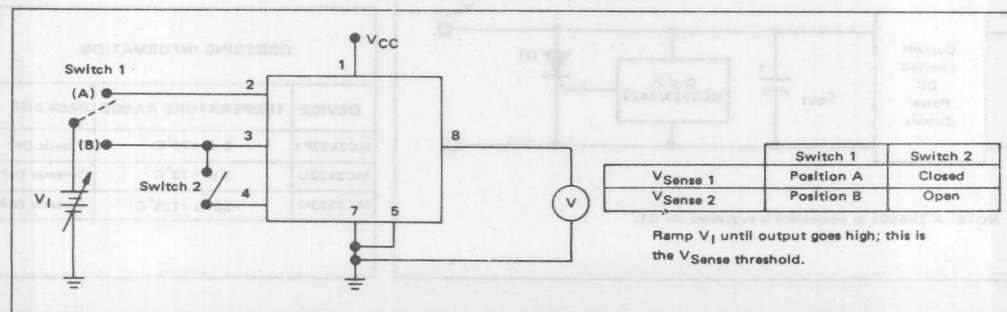


FIGURE 3 – BASIC CIRCUIT CONFIGURATION

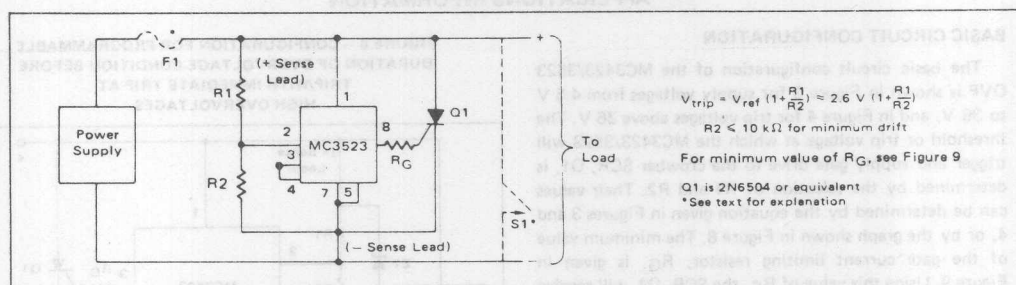


FIGURE 4 – CIRCUIT CONFIGURATION FOR SUPPLY VOLTAGE ABOVE 36 V

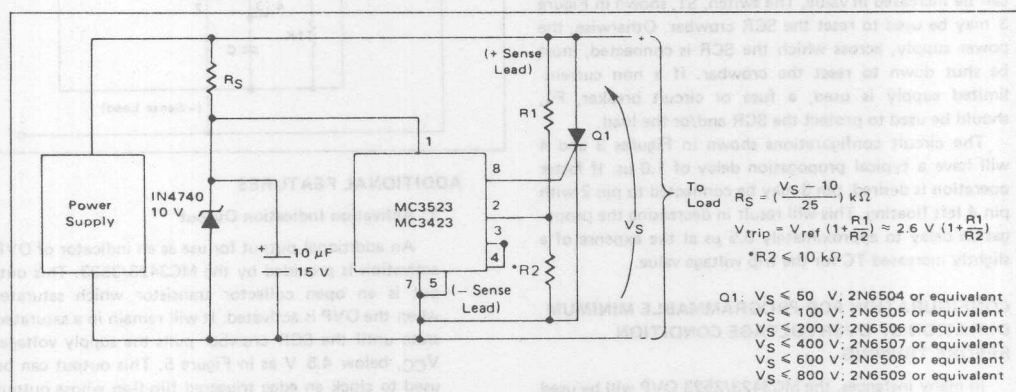
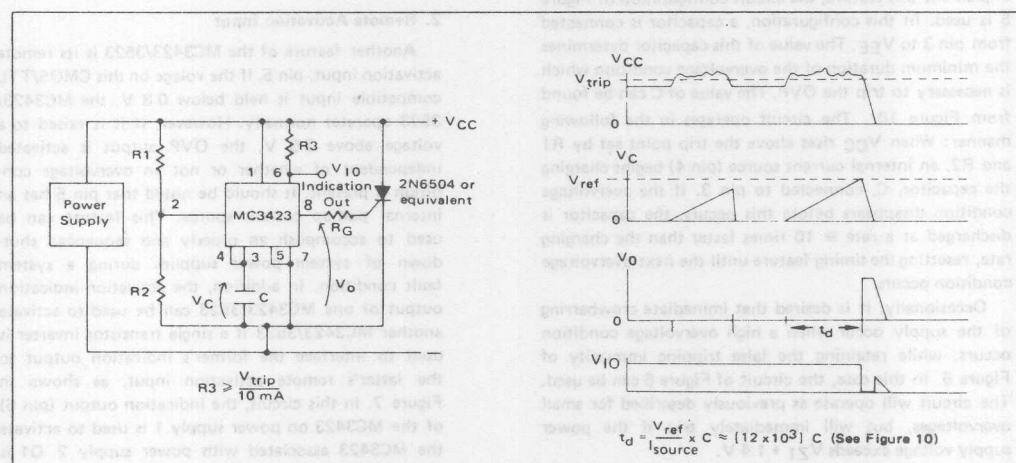


FIGURE 5 – BASIC CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP



APPLICATIONS INFORMATION

BASIC CIRCUIT CONFIGURATION

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G , is given in Figure 9. Using this value of R_G , the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

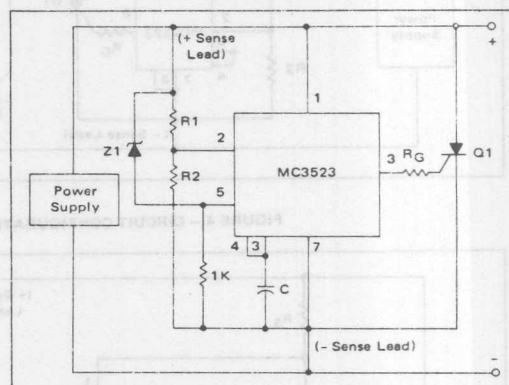
The circuit configurations shown in Figures 3 and 4 will have a typical propagation delay of 1.0 μ s. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propagation delay to approximately 0.5 μ s at the expense of a slightly increased TC for the trip voltage value.

CONFIGURATION FOR PROGRAMMABLE MINIMUM DURATION OF OVERVOLTAGE CONDITION BEFORE TRIPPING

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from pin 3 to V_{EE} . The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≈ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds $V_{Z1} + 1.4$ V.

FIGURE 6 - CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP/WITH IMMEDIATE TRIP AT HIGH OVERVOLTAGES



ADDITIONAL FEATURES

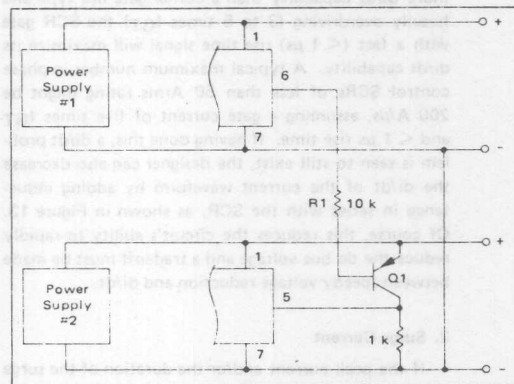
1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC} , below 4.5 V as in Figure 5. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shut-down of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

FIGURE 7 - CIRCUIT CONFIGURATION FOR ACTIVATING ONE MC3523 FROM ANOTHER



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}^1 . This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt , absolute peak surge, or I^2t . The interrelationship of these failure methods and the breadth of the application make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

C_{out}^1 consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps.

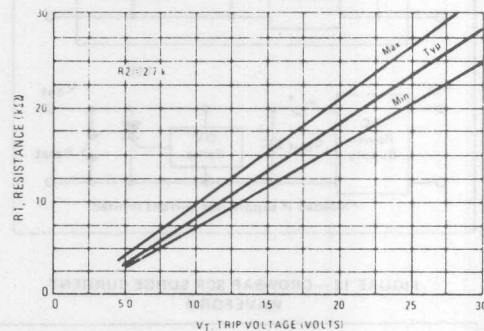
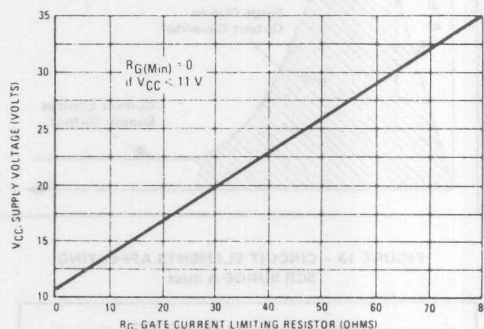
FIGURE 8 - R_1 versus TRIP VOLTAGEFIGURE 9 - MINIMUM R_G versus SUPPLY VOLTAGE

FIGURE 10 - CAPACITANCE versus MINIMUM OVERVOLTAGE DURATION

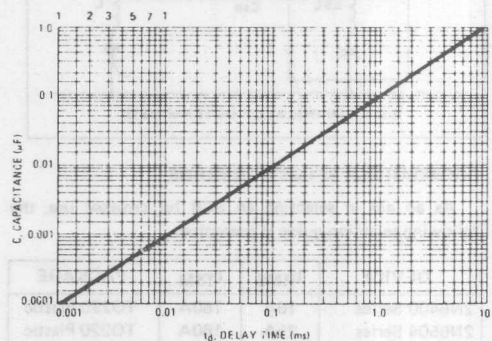


FIGURE 11 – TYPICAL CROWBAR OVP CIRCUIT CONFIGURATIONS

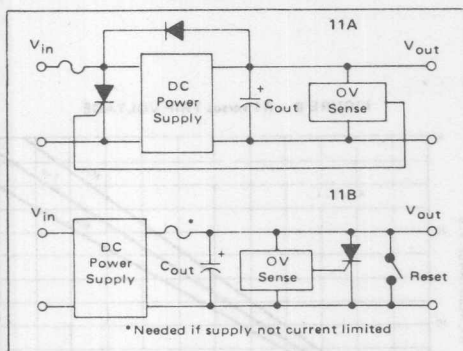
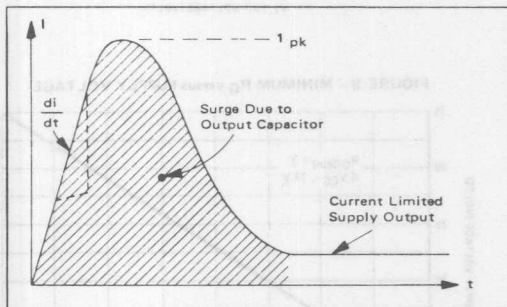
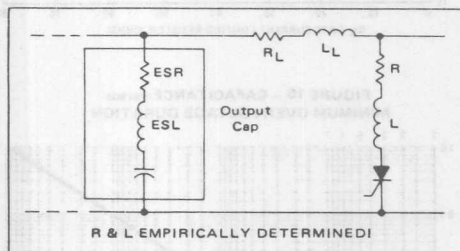


FIGURE 12 – CROWBAR SCR SURGE CURRENT WAVEFORM

FIGURE 13 – CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt 

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{TSM}	PACKAGE
2N6400 Series	16A	160A	TO220 Plastic
2N6504 Series	25A	160A	TO220 Plastic
2N1842 Series	16A	125A	Metal Stud
2N2573 Series	25A	260A	Metal TO-3 Type
2N681 Series	25A	200A	Metal Stud
MCR3935-1 Series	35A	350A	Metal Stud
MCR81-5 Series	80A	1000A	Metal Stud

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast ($< 1 \mu s$) rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 Arms rating might be 200 A/ μs , assuming a gate current of five times I_{GT} and $< 1 \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt .

2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 13) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

MC3490 MC3494

ANODE (DIGIT) DRIVERS FOR GAS-DISCHARGE DISPLAYS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

SEVEN-DIGIT GAS-DISCHARGE DISPLAY DRIVERS

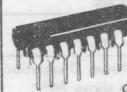
Seven channel digit (anode) drivers, the MC3490 and MC3494 are specifically conceived to be used with high-voltage, gas-discharge numeric displays such as the Burroughs' Panaplex®, Beckman (Sperry) Cherry, or Diacon displays.

The MC3490 version is configured such that a high logic level input causes the driver to turn on while the MC3494 requires a low logic level to turn the drivers on. Both devices are designed to mate with the MC3491 cathode (segment) driver.

With a low input current requirement of only 300 μ A typically, these devices are compatible with popular MOS chips.

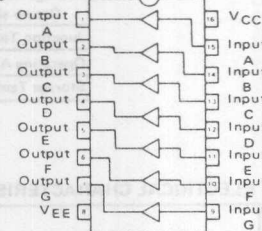
Minimum breakdown voltage is specified at 48 V and output drive current capability is typically 30 mA per channel.

- High Breakdown Voltage — 55 V Typical
- Low Input Current for MOS Compatibility
- Available with Either Active High or Active Low Inputs
- Operable from Either Positive or Negative Supply Voltages
- Input Clamp Diodes on MC3494 Version for DC Restoration
- Internal Pull-down Resistors

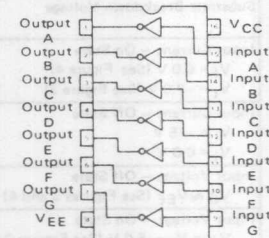


P SUFFIX
PLASTIC
PACKAGE
CASE 648

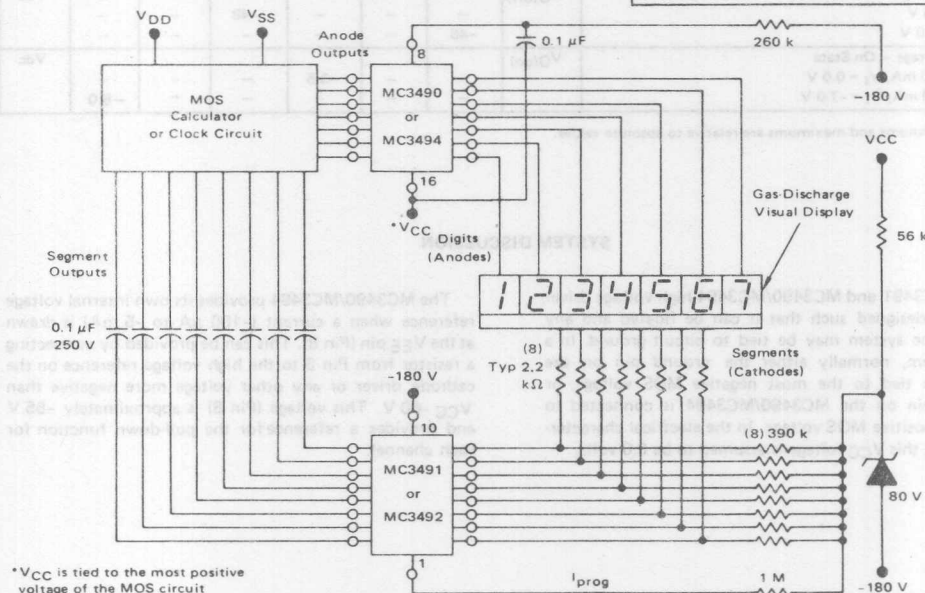
PIN CONNECTIONS MC3490



MC3494



TYPICAL APPLICATION WITH CAPACITIVE LEVEL SHIFT TO CATHODE DRIVER



® Registered Trademark of Burroughs Corporation

MC3490, MC3494

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Negative Supply Voltage (Current Limited to -5 mA)	V_{EE}	-60	Vdc
Negative Supply Current	I_{EE}	-5.0	mAdc
Input Voltage	V_I	$V_{CC}-20, V_{CC}$	Vdc
Output Current ($V_O = -5\text{ V}$)	I_O	-50	mAdc
Package Power Dissipation Derate above 25°C	P_D	830 6.7	mW mW/ $^\circ\text{C}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to $+70$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = \text{Gnd}$, $V_{EE} = -60\text{ V}$ thru $5.0\text{ k}\Omega$, unless otherwise noted.)

Characteristic	Symbol	MC3490			MC3494			Unit
		Min	Typ	Max	Min	Typ	Max	
Substrate Breakdown Voltage	$V_{S(BR)}$	-48	-55	—	-48	-55	—	Vdc
Input Current — On State $V_I = 0.0\text{ V}$ (See Figure 4) $V_I = -7.0\text{ V}$ (See Figure 3)	$I_{I(on)}$	—	250	700	—	—	—	μA
Input Current — Off State $V_I = -15\text{ V}$ $V_I = 0.0\text{ V}$	$I_{I(off)}$	—	< -1.0	-45	—	—	—	μA
Input Voltage — Off State $V_O \approx V_{EE}$ (See Figures 3 and 4)	$V_{I(off)}$	—	—	-5.0	-2.0	—	—	Vdc
Input Voltage — On State $V_O = V_{CC} - 5.0\text{ V}$ (See Figures 3 and 4)	$V_{I(on)}$	-2.0	—	—	—	—	-5.0	Vdc
Output Voltage — Off State $V_I = 0.0\text{ V}$ $V_I = -7.0\text{ V}$	$V_{O(off)}$	—	—	—	-48	—	—	Vdc
Output Voltage — On State $I_O = -20\text{ mA}$, $V_I = 0.0\text{ V}$ $I_O = -20\text{ mA}$, $V_I = -7.0\text{ V}$	$V_{O(on)}$	—	—	-3.5	—	—	—	Vdc

NOTE: Minimums and maximums are relative to absolute values.

SYSTEM DISCUSSION

The MC3491 and MC3490/MC3494 high voltage driver system is designed such that it can be floated and any point in the system may be tied to circuit ground. In a MOS system, normally either the ground pin on the MC3491 is tied to the most negative MOS voltage; or the V_{CC} pin on the MC3490/MC3494 is connected to the most positive MOS voltage. In the electrical characteristics table, this V_{CC} voltage is assumed to be 0.0 volts.

The MC3490/MC3494 provides its own internal voltage reference when a current ($-100\text{ }\mu\text{A}$ to -5 mA) is drawn at the V_{EE} pin (Pin 8). This can be provided by connecting a resistor from Pin 8 to the high voltage reference on the cathode driver or any other voltage more negative than $V_{CC} - 60\text{ V}$. This voltage (Pin 8) is approximately -55 V and provides a reference for the pull-down function for each channel.

TYPICAL PERFORMANCE CHARACTERISTICS

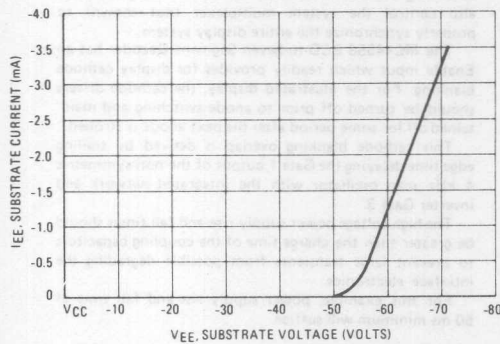
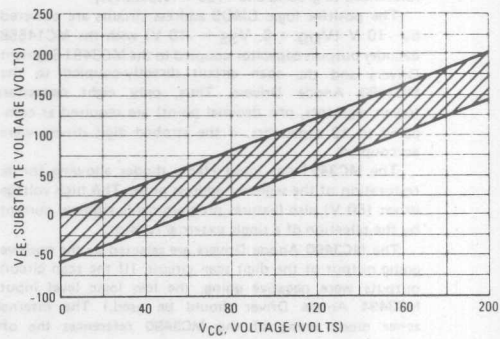
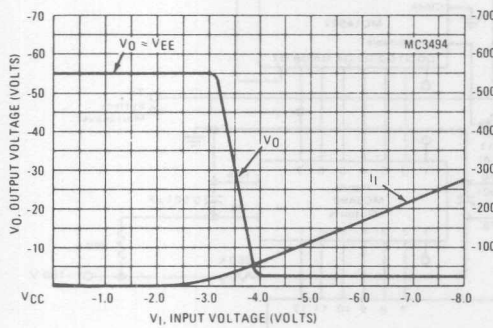
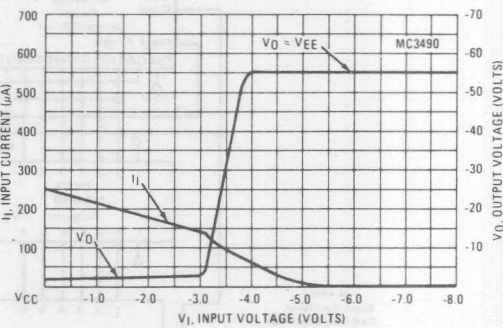
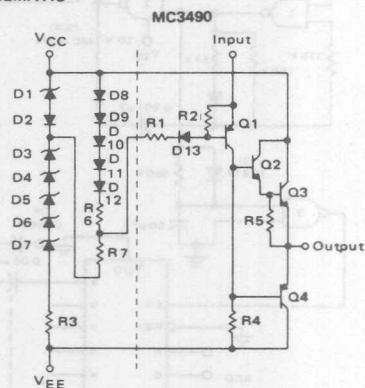
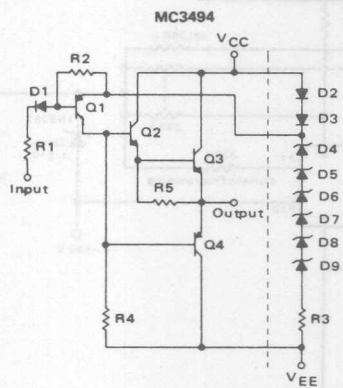
FIGURE 1 - SUBSTRATE CURRENT versus
SUBSTRATE VOLTAGE

FIGURE 2 - PERMISSIBLE OPERATING RANGE

FIGURE 3 - OUTPUT VOLTAGE and INPUT CURRENT
versus INPUT VOLTAGEFIGURE 4 - INPUT CURRENT and OUTPUT VOLTAGE
versus INPUT VOLTAGEREPRESENTATIVE CIRCUIT SCHEMATIC
(1/7 Shown)

12-DIGIT CMOS GAS DISCHARGE DISPLAY

When the number of digits for a gas discharge display system is greater than the number of segment drivers, it is generally more economical to level translate down to the cathode segments than to translate up to the digit anodes. An example of this technique is shown in the 12 digit display system where the display anodes and cathodes are referenced to ground and -180 V respectively.

The positive logic CMOS address circuits are powered by -10 V ($V_{DD} = 0$, $V_{SS} = -10$ V) with the MC14558 decoder outputs capacitor-coupled to the MC3491 Segment Drivers and the scan circuit directly-coupled to the MC3490 Anode Drivers. Thus, only eight capacitors (seven segments, one decimal point) are required as compared to 12 capacitors, if the strobed digit drivers were ac coupled.

The MC3491 has input clamp diodes allowing for dc restoration of the segment address pulse. This high voltage driver (80 V) also features programmable segment current by the selection of a single external resistor.

The MC3490 Anode Drivers are selected by the positive going output of the digit scan circuit. (If the scan circuit outputs were negative going, the low logic level input MC3494 Anode Driver should be used.) The internal zener diode string of the MC3490 references the off

drivers (and display anodes) to -50 V without the need of pull-down resistors.

Digit scanning for this example is derived from two cascaded MC14022 Octal Counter/Drivers. The 12 sequenced output pulses are achieved by resetting the counters with the second counter Q7 output. In addition to driving the two MC3490s, the counter output should also control the system multiplexer (not shown) to properly synchronize the entire display system.

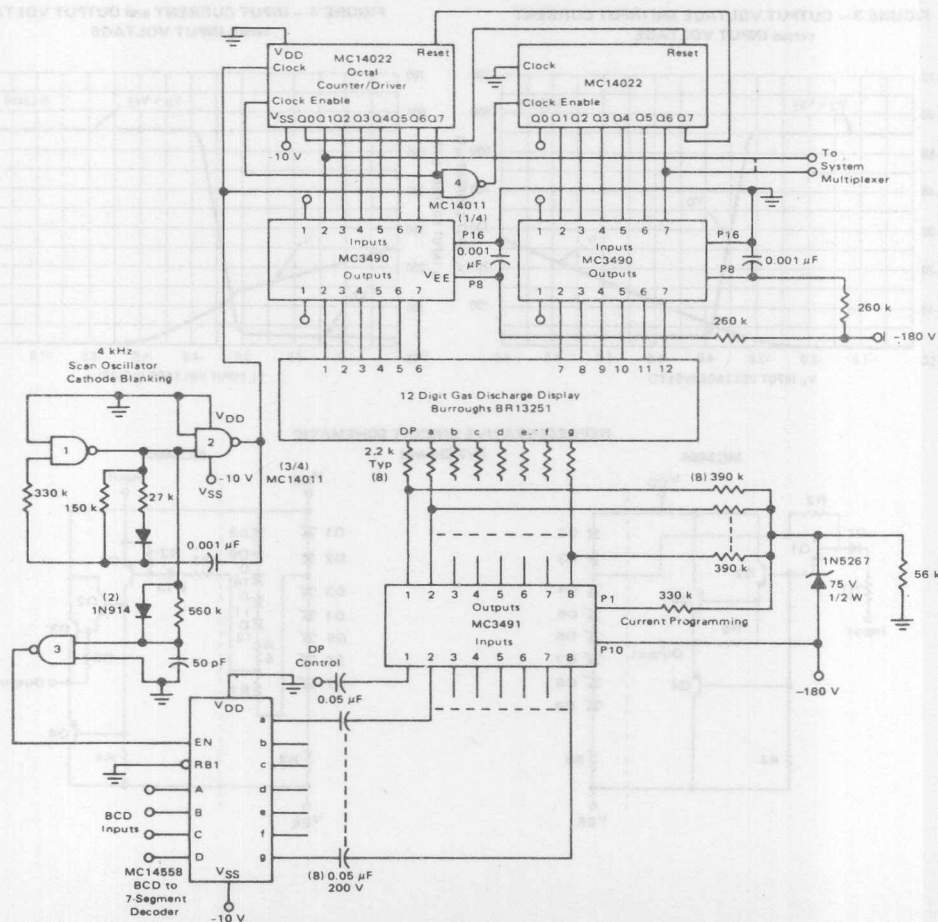
The MC14558 BCD-to-Seven Segment Decoder has an Enable input which readily provides for display cathode blanking. For the illustrated display, the cathode drivers should be turned off prior to anode switching and maintained off for some period after the next anode is strobed.

This cathode blanking overlap is derived by trailing edge time delaying the Gate 1 output of the non-symmetric 4 kHz scan oscillator with the integrated network and inverter Gate 3.

The high voltage power supply rise and fall times should be greater than the charge time of the coupling capacitors to prevent large transients from possible degrading the interface electronics.

For this example, power supply rise and fall time of 50 ms minimum will suffice.

FIGURE 5 — 12-DIGIT CMOS GAS DISCHARGE DISPLAY SYSTEM



3-1/2 DIGIT VOLTMETER

This specific application provides a 3-1/2 digit DVM utilizing the MC1505 dual ramp subsystem and CMOS MC14435 digital subsystem. Interfacing between low voltage logic ICs and the higher voltage gas discharge displays requires level translation or shifting. The method described for the 3-1/2 Digit DVM uses directly coupled high voltage (200 V) transistors to translate upw. d to the MC3494 Anode Drivers. Three of the transistors comprising the MPQ7042 high voltage quad transistor are used for this function. These transistors, connected in a common-base, constant-current configuration, are turned on by the negative going digit select output pulses of the MC14435. The current of approximately 330 μ A is compatible with 200 μ A typical input current of the MC3494 and the sink current capability of the MC14435.

The CMOS MC14558 BCD-to-Seven Segment Decoder has the capability of directly driving the MC3491 Segment Driver. Cathode blanking is accomplished by taking the clock signal from Pin 4 of the MC14435 (approximately 50% duty cycle) and tying it to the Enable input of the MC14558. The display segment current is increased accordingly to 1.1 mA (manufacturers maximum specified current

equals 1.25 mA) for this relatively large cathode blanking period.

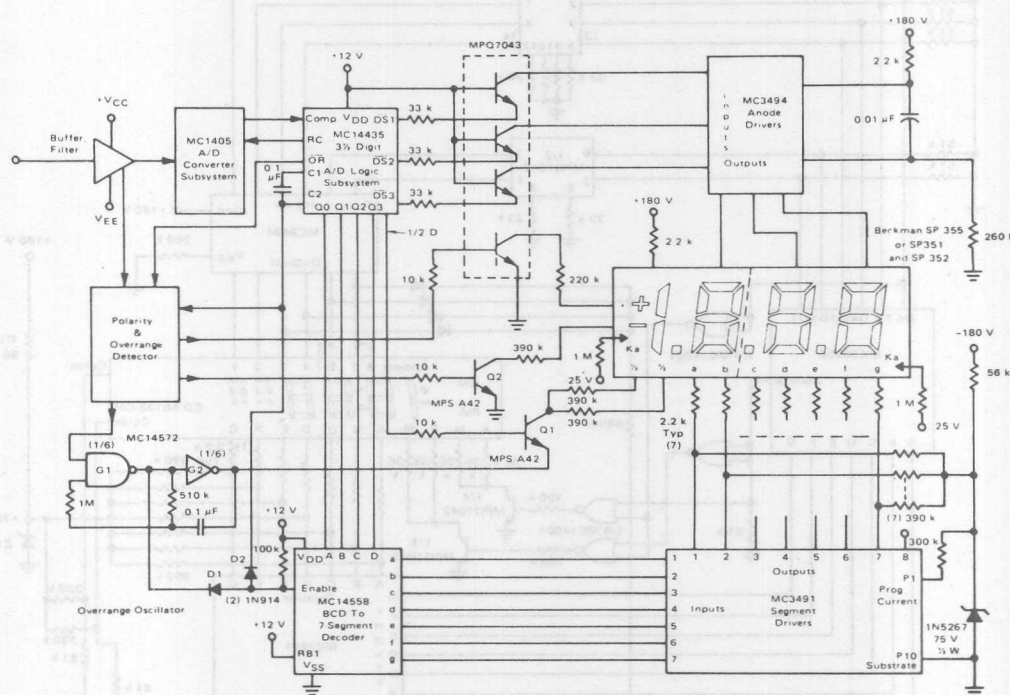
The positive and negative polarity signs are direct driven by the fourth transistor of the MPQ7043 and MPS-A42 transistor, Q2, respectively. Their dc segment currents are scaled to produce the same brightness as the multiplexed digits.

The 1/2 digit segments are driven by transistor Q1. Its emitter is normally referenced to ground through MC14572 Inverter G2, the output inverter of the Overrange Oscillator.

When an overrange situation occurs, the oscillator is enabled, thus causing the display to flash at the oscillator rate (approximately 8 Hz). This is accomplished by blanking the 1/2 digit through Q1 and the multiplexed digits through diode D1 to the decoder enable input.

See the MC1405 and MC14435 data sheets for more details of DVM system.

FIGURE 6 - 3-1/2 DIGIT DIGITAL VOLTMETER



12-HOUR CLOCK WITH GAS DISCHARGE DISPLAYS

The MC3491 cathode driver and MC3494 anode driver, greatly simplify the interfacing of a clock chip (MOSTEK MK50250) to a gas discharge clock display (Burroughs CD60733-CM).

The MK50250 has a 6 digit clock display with multiplexed 7 segment outputs. The MC3491 cathode drivers switch each display cathode between ground (on condition) and +75 Volts (off condition) with current limiting for the display provided via the current programming pin on the MC3491. The +75 Volt reference is obtained from a 75-Volt zener diode, Z1, R1, and a 50-Volt zener diode internal to the MC3494 anode driver.

The programming current is reduced during the time when the "two seconds" indicator digits are ON, to reduce the current through these smaller digits of the display. Four diodes attached to each of the "hours" and "minutes" digits, provide a voltage of +180 Volts across the 680 k Ω resistor. During the "seconds" digits display time, the voltage is reduced to +130 Volts, thus reducing the programming current.

The anodes for each of the six digits are switched between the +180 Volt positive supply and +130 Volts via the MC3494 anode drivers. Inter-digit blanking is

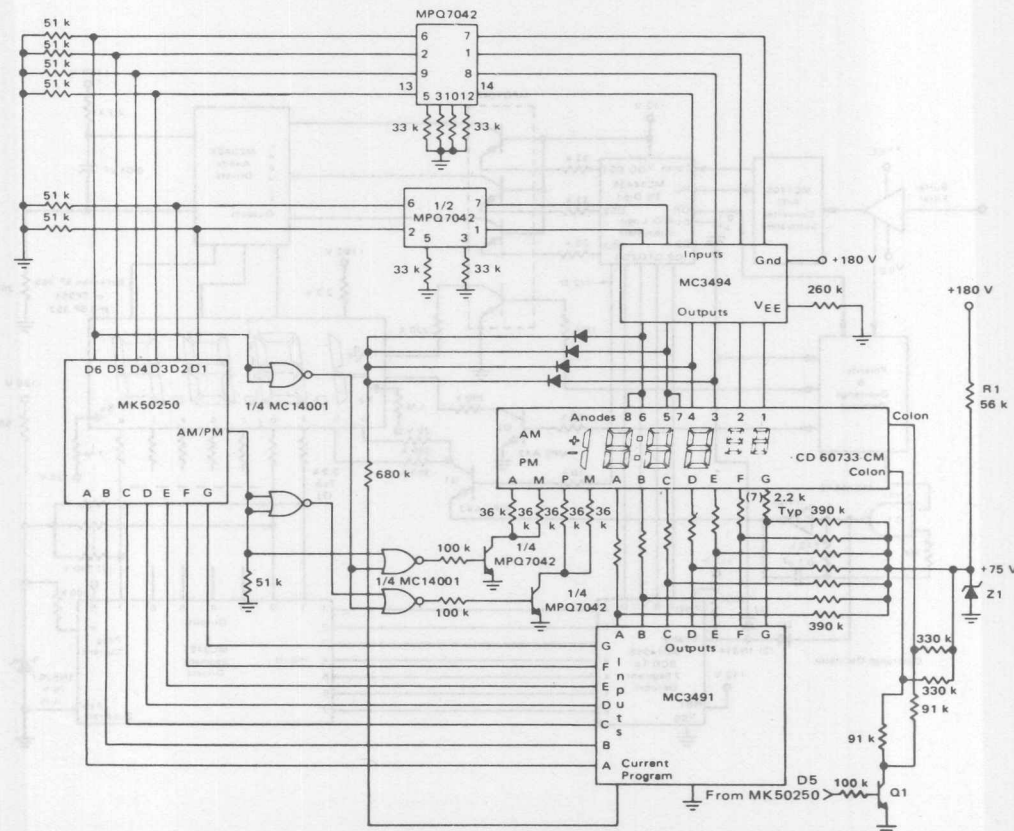
provided in the anode circuits. Level translation from the clock chip output to the input to the MC3494 uses two MPQ7042 quad high voltage transistor packages operating in an emitter follower current source mode. Each current source turns on one of the MC3494 drivers by sinking 300 μ A to ground for the proper "on" digit.

The AM/PM clock output is in the high state when PM is indicated and has a 85% duty cycle corresponding to each anode on time. A MC14001 Quad NOR Gate decodes this output to turn on the appropriate AM or PM indicator during the D6 digit. These Gates control the AM/PM display indicators with the remaining MPQ7042 high voltage transistors which were not used in anode selection.

The colon separating hours and minutes is switched on during the units of hours digit on time. The colon cathodes are switched from +75 Volts to ground via T1 during the D5 digit time while the anodes are switched between +180 and +130 Volts.

Further information concerning operation or technical specifications on the MOSTEK clock chip, MK50250, and the Burroughs clock display, CD60733-CM is obtainable from the manufacturers.

FIGURE 7 - 12 HOUR CLOCK WITH GAS DISCHARGE DISPLAY SYSTEM



MC3491 MC3492

EIGHT-SEGMENT VISUAL DISPLAY DRIVERS

The MC3491 and MC3492 are eight-segment cathode drivers for use with gas-discharge displays, such as the Burroughs' Panaplex®, Beckman, Cherry or Diacon types. Both devices are directly compatible with MOS logic outputs due to their low 300 μ A input current requirement.

All eight driver output currents are simultaneously programmable by selection of a single external resistor. As programmed, all eight currents match to within typically 1% of each other.

Both devices provide dc restoration. The units are specified for a minimum breakdown voltage of 80 V.

The MC3492 device is made for larger and higher intensity displays requiring higher segment current.

- High Breakdown Voltage – 80 V Min
- Drives Seven Cathode Segments plus Decimal Point
- All Currents Simultaneously Programmable with One Resistor
- MC3491 is Pin-for-Pin and Functionally Equivalent to DM8889
- Output Current/Programming Current Ratio –
Typically 4.5:1 for MC3491
9:1 for MC3492
- Companion with MC3490 and MC3494 Anode Drivers
- MC3492 Provides Increased Output Current for High Intensity Displays

*Higher Voltage Selection Available

SEGMENT DRIVERS FOR GAS-DISCHARGE DISPLAYS SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 701

PIN CONNECTIONS

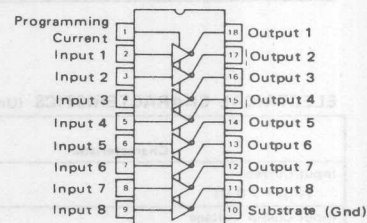
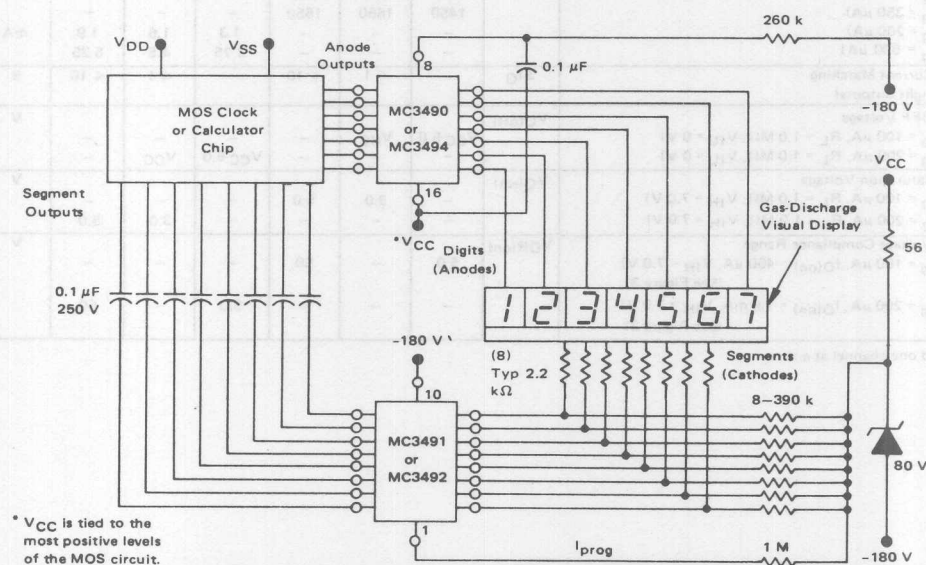


FIGURE 1 – TYPICAL CALCULATOR APPLICATION
WITH CAPACITIVE LEVEL SHIFT AND ANODE DRIVER



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MC3491, MC3492

MAXIMUM RATINGS (Unless otherwise noted, $T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Output OFF Voltage (Current Limited to 0.5 mA)	$V_{O(\text{off})}$	95	V
Output ON Voltage (Current Limited to 2.0 mA)	$V_{O(\text{on})}$	50	V
Input Voltage	V_I	20	V
Programming Current	I_{prog}	400 2500	μA
Junction Temperature	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to 70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $V_{CC} < 80\text{ V}$, $T_A = 25^\circ\text{C}$, Pin 10 = Gnd. All voltages with respect to Gnd.)

Characteristic	Symbol	MC3491			MC3492			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Current ($V_{IH} = 7.0\text{ V}$)	I_{IH}	200	300	400	200	300	400	μA
Input Clamp Voltage ($I_{IK} = -1.0\text{ mA}$)	V_{IK}	—	—	-1.0	—	—	-1.0	V
Input OFF Voltage	V_{IL}	1.0	1.5	—	1.0	1.5	—	V
Input ON Voltage	V_{IH}	—	2.4	3.5	—	2.4	3.5	V
Output OFF Current ($V_{IL} = 0\text{ V}$, $V_O = V_{CC}$)	$I_{O(\text{off})}$	—	—	5.0	—	—	5.0	μA
Output ON Current (at $V_{IH} = 7.0\text{ V}$)* ($I_{\text{prog}} = 100\text{ }\mu\text{A}$) ($I_{\text{prog}} = 350\text{ }\mu\text{A}$) ($I_{\text{prog}} = 200\text{ }\mu\text{A}$) ($I_{\text{prog}} = 500\text{ }\mu\text{A}$)	$I_{O(\text{on})}$	400	450	500	—	—	—	μA
		1450	1650	1850	—	—	—	
		—	—	—	1.3	1.6	1.9	mA
		—	—	—	3.75	4.5	5.25	
Output Current Matching (All eight outputs)	ΔI_O	—	≤ 1	≤ 10	—	≤ 1	≤ 10	%
Output OFF Voltage ($I_{\text{prog}} = 100\text{ }\mu\text{A}$, $R_L = 1.0\text{ M}\Omega$, $V_{IL} = 0\text{ V}$) ($I_{\text{prog}} = 200\text{ }\mu\text{A}$, $R_L = 1.0\text{ M}\Omega$, $V_{IL} = 0\text{ V}$)	$V_{O(\text{off})}$	$V_{CC}-5.0$	V_{CC}	—	$V_{CC}-5.0$	V_{CC}	—	V
Output Saturation Voltage ($I_{\text{prog}} = 100\text{ }\mu\text{A}$, $R_L = 1.0\text{ M}\Omega$, $V_{IH} = 7.0\text{ V}$) ($I_{\text{prog}} = 200\text{ }\mu\text{A}$, $R_L = 1.0\text{ M}\Omega$, $V_{IH} = 7.0\text{ V}$)	$V_{O(\text{sat})}$	—	3.0	5.0	—	3.0	5.0	V
Output Voltage Compliance Range ($I_{\text{prog}} = 100\text{ }\mu\text{A}$, $I_{O(\text{on})} = 450\text{ }\mu\text{A}$, $V_{IH} = 7.0\text{ V}$) (See Figure 3) ($I_{\text{prog}} = 200\text{ }\mu\text{A}$, $I_{O(\text{on})} = 1.6\text{ mA}$, $V_{IH} = 7.0\text{ V}$) (See Figure 3)	$V_{OR(\text{on})}$	5.0	—	50	—	—	—	V
		—	—	—	5.0	—	50	

*Measured one channel at a time.

TYPICAL PERFORMANCE CHARACTERISTICS

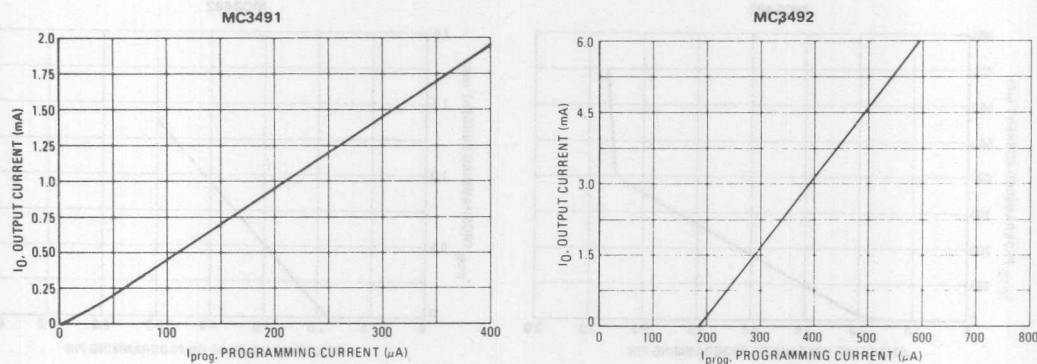
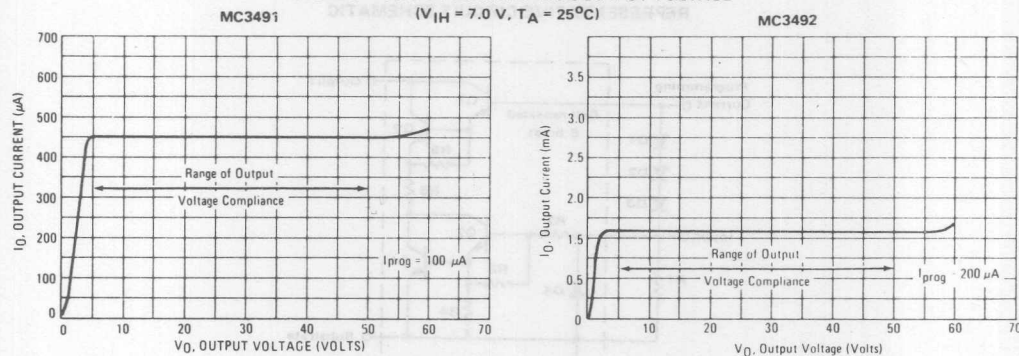
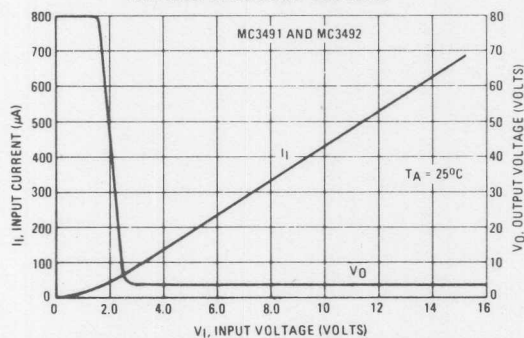
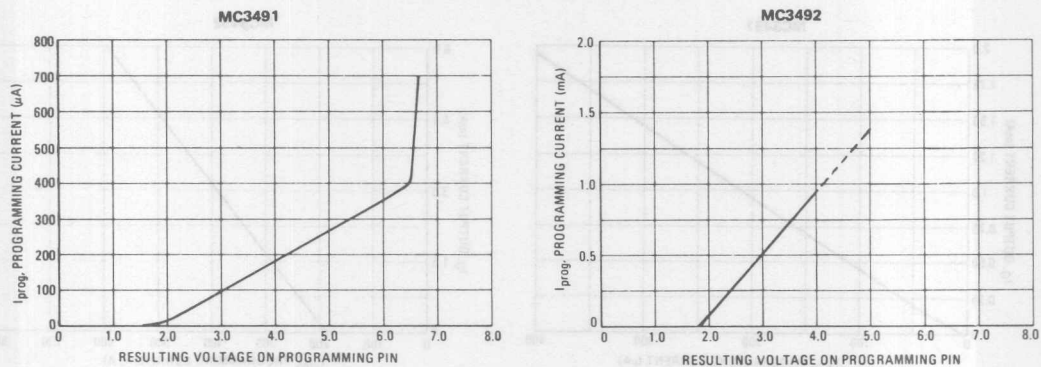
FIGURE 2 – OUTPUT CURRENT versus PROGRAMMING CURRENT ($T_A = 25^\circ\text{C}$)FIGURE 3 – OUTPUT CURRENT versus OUTPUT VOLTAGE
($V_{IH} = 7.0\text{ V}$, $T_A = 25^\circ\text{C}$)

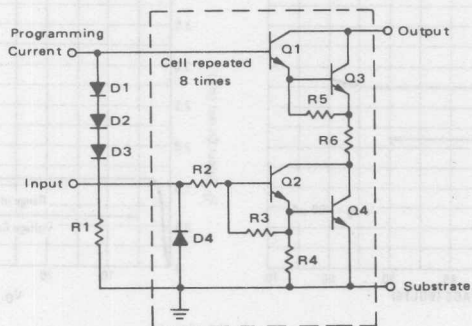
FIGURE 4 – TYPICAL INPUT CURRENT AND OUTPUT VOLTAGE versus INPUT VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 5 – TYPICAL PROGRAMMING CURRENT versus VOLTAGE ON PROGRAMMING PIN
($T_A = 25^\circ\text{C}$)

REPRESENTATIVE CIRCUIT SCHEMATIC



3-1/2-DIGIT VOLTMETER

This specific application provides a 3-1/2-digit DVM utilizing the MC1505 dual ramp subsystem and CMOS MC14435 digital subsystem. Interfacing between low voltage logic ICs and the higher voltage gas discharge displays requires level translation or shifting. The method described for the 3-1/2 digit DVM uses directly coupled high voltage (200 V) transistors to translate upward to the MC3494 Anode Drivers. Three of the transistors comprising the MPQ7042 high voltage quad transistor are used for this function. These transistors connected in a common-base, constant-current configuration are turned on by the negative-going digit select output pulses of the MC14435. The current of approximately 330 μ A is compatible with 200 μ A typical input current of the MC3494 and the sink current capability of the MC14435.

The CMOS MC14558 BCD-to-Seven Segment Decoder has the capability of directly driving the MC3491 or MC3492 Segment Drivers. Cathode blanking is accomplished by taking the clock signal from Pin 4 of the MC14435 (approximately 50% duty cycle) and tying it to the Enable input of the MC14458. The display segment

current is increased accordingly to 1.1 mA (manufacturers maximum specified current equals 1.25 mA) for this relatively large cathode blanking period.

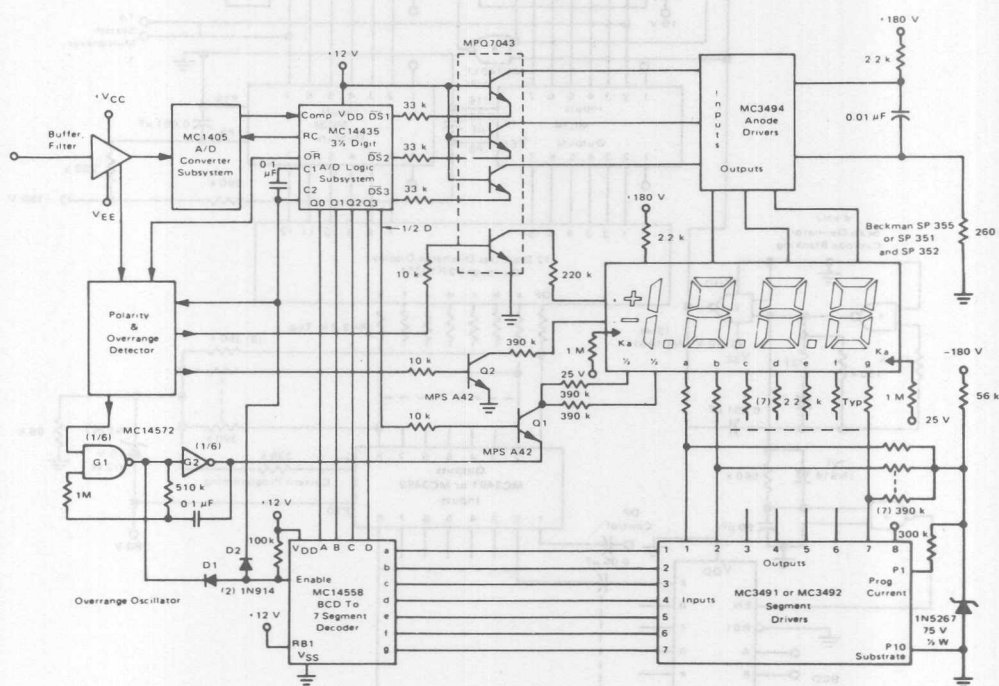
The positive and negative polarity signs are directly driven by the fourth transistor of the MPQ7043 and MPS-A42 transistor, Q2, respectively. Their dc segment currents are scaled to produce the same brightness as the multiplexed digits.

The 1/2-digit segments are driven by transistor Q1. Its emitter is normally referenced to ground through MC14572 Inverter G2, the output inverter of the Over-range Oscillator.

When an overrange situation occurs, the oscillator is enabled, thus causing the display to flash at the oscillator rate (approximately 8 Hz). This is accomplished by blanking the 1/2 digit through Q1 and the multiplexed digits through diode D1 to the decoder enable input.

See the MC1405 and MC14435 data sheets for more details of DVM system.

FIGURE 6 — 3-1/2 DIGIT DIGITAL VOLTMETER



12-DIGIT CMOS GAS DISCHARGE DISPLAY

When the number of digits for a gas discharge display system is greater than the number of segment drivers, it is generally more economical to level translate down to the cathode segments (than to translate up to the digit anodes). An example of this technique is shown in the 12 digit display system where the display anodes and cathodes are referenced to ground and -180 V respectively.

The positive logic CMOS address circuits are powered by -10 V ($V_{DD} = 0$, $V_{SS} = -10$ V) with the MC14558 decoder outputs capacitor-coupled to the MC3491 Segment Drivers and the scan circuit directly-coupled to the MC3490 Anode Drivers. Thus, only eight capacitors (seven segments, one decimal point) are required as compared to 12 capacitors, if the strobed digit drivers were ac coupled.

The MC3491 and MC3492 have input clamp diodes allowing for dc restoration of the segment address pulse. These high voltage drivers (80 V) also feature programmable segment current by the selection of a single external resistor.

The MC3490 Anode Drivers are selected by the positive going output of the digit scan circuit. (If the scan circuit outputs were negative going, the low logic level input MC3494 Anode Driver should be used.) The internal

zener diode string of the MC3490 references the off drivers (and display anodes) to -50 V without the need of pull-down resistors.

Digit scanning for this example is derived from two cascaded MC14022 Octal Counter/Drivers. The 12 sequenced output pulses are achieved by resetting the counters with the second counter Q7 output. In addition to driving the two MC3490's, the counter output should also control the system multiplexer (not shown) to properly synchronize the entire display system.

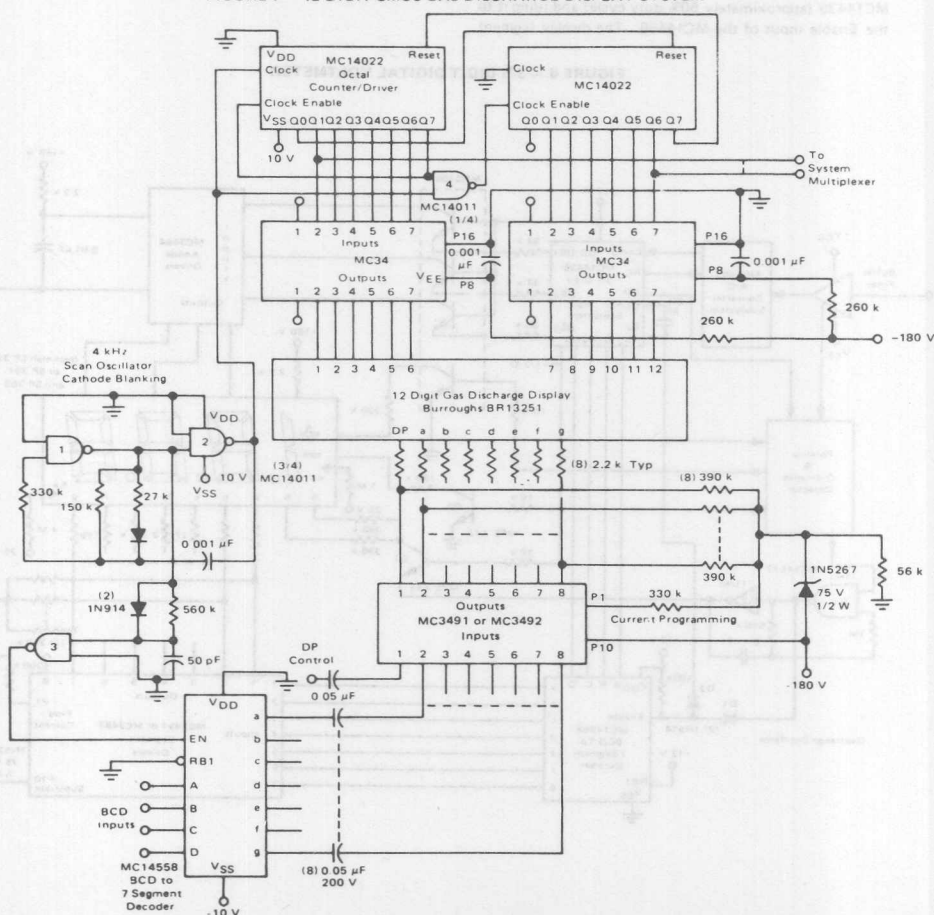
The MC14558 BCD-to-Seven Segment Decoder has an Enable input which readily provides for display cathode blanking. For the illustrated display, the cathode drivers should be turned off prior to anode switching and maintained off for some period after the next anode is strobed.

This cathode blanking overlap is derived by trailing edge time delaying the Gate 1 output of the non-symmetric 4 kHz scan oscillator with the integrated network and inverter Gate 3.

The high voltage power supply rise and fall times should be greater than the charge time of the coupling capacitors to prevent large transients from possible degrading the interface electronics.

For this example, power supply rise and fall time of 50 ms minimum will suffice.

FIGURE 7 - 12-DIGIT CMOS GAS DISCHARGE DISPLAY SYSTEM



MC3491, MC3492

12-HOUR CLOCK WITH GAS DISCHARGE DISPLAYS

The MC3491 or MC3492 cathode drivers and MC3494 anode driver, greatly simplify the interfacing of a clock chip (MOSTEK MK50250) to a gas discharge clock display (Burroughs CD60733-CM).

The MK50250 has a 6-digit clock display with multiplexed 7-segment outputs. The MC3491 cathode drivers switch each display cathode between ground (on condition) and +75 Volts (off condition) with current limiting for the display provided via the current programming pin on the MC3491 or MC3492. The +75 Volt reference is obtained from a 75-Volt zener diode, Z1, R1, and a 50-Volt zener diode internal to the MC3494 anode driver.

The programming current is reduced during the time when the "two seconds" indicator digits are ON, to reduce the current through these smaller digits of the display. Four diodes attached to each of the "hours" and "minutes" digits, provide a voltage of +180 Volts across the 680 k Ω resistor. During the "seconds" digits display time, the voltage is reduced to +130 Volts, thus reducing the programming current.

The anodes for each of the six digits are switched between the +180 Volt positive supply and +130 Volts via the MC3494 anode drivers. Inter-digit blanking is

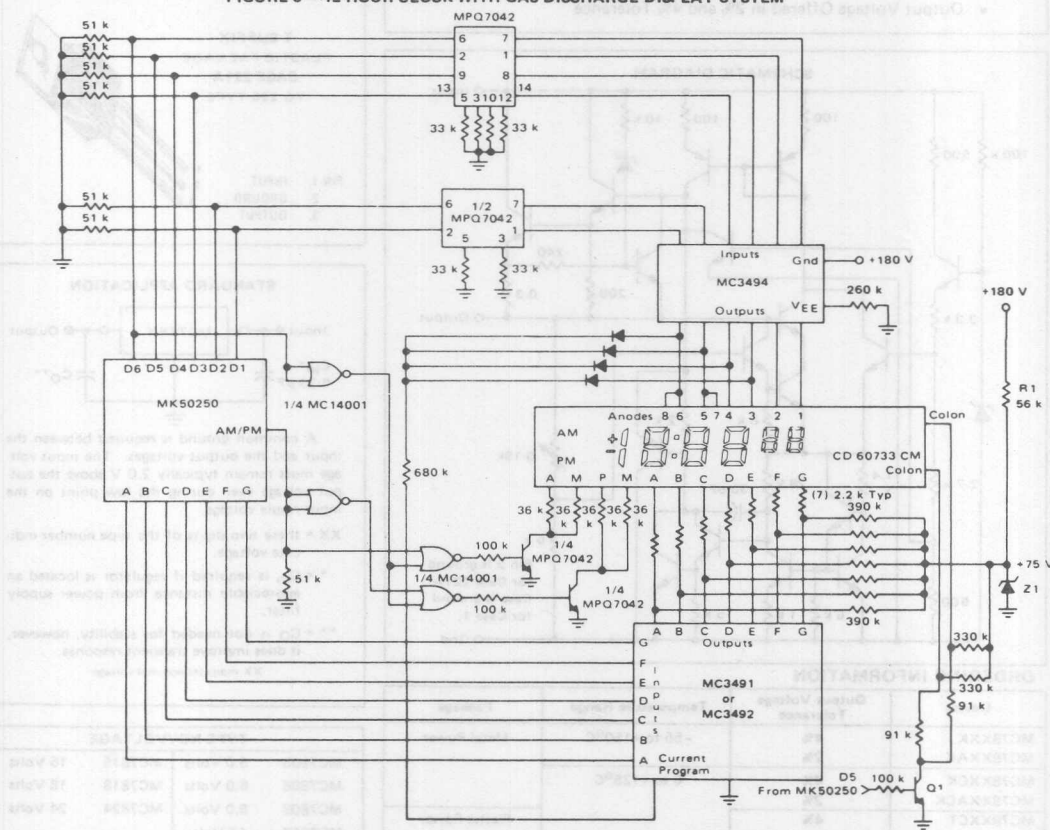
provided in the anode circuits. Level translation from the clock chip output to the input to the MC3494 uses two MPQ7042 quad high voltage transistor packages operating in an emitter-follower current source mode. Each current source turns on one of the MC3494 drivers by sinking 300 μ A to ground for the proper "on" digit.

The AM/PM clock output is in the high state when PM is indicated and has an 85% duty cycle corresponding to each anode on time. A MC14001 Quad NOR Gate decodes this output to turn on the appropriate AM or PM indicator during the D6 digit. These Gates control the AM/PM display indicators with the remaining MPQ7042 high voltage transistors which were not used in anode selection.

The colon separating hours and minutes is switched on during the units of hours digit on time. The colon cathodes are switched from +75 Volts to ground via T1 during the D5 digit time while the anodes are switched between +180 and +130 Volts.

Further information concerning operation or technical specifications on the MOSTEK clock chip, MK50250, and the Burroughs clock display, CD60733-CM is obtainable from the manufacturers.

FIGURE 8 — 12-HOUR CLOCK WITH GAS DISCHARGE DISPLAY SYSTEM



MC7800 Series

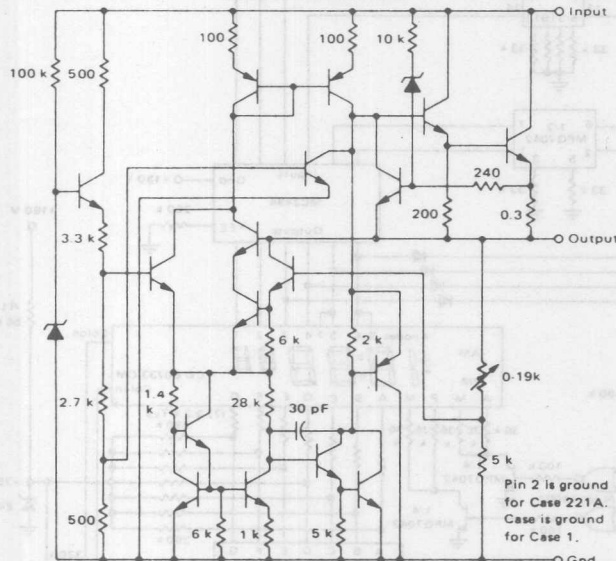
Advance Information

3-TERMINAL POSITIVE VOLTAGE REGULATORS

These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance

SCHEMATIC DIAGRAM



Pin 2 is ground
for Case 221A.
Case is ground
for Case 1.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Temperature Range	Package
MC78XXK	4%	-55 to +150°C	Metal Power
MC78XXAK	2%		
MC78XXCK	4%	0 to +125°C	Plastic Power
MC78XXACK	2%		
MC78XXCT	4%		
MC78XXACT	2%		

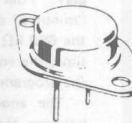
XX Indicates Nominal Voltage

This is advance information and specifications are subject to change without notice.

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

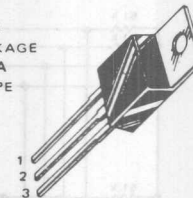
K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 TYPE)

PIN 1. INPUT
2. OUTPUT
CASE GROUND

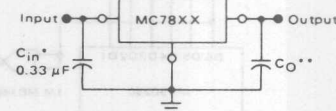


T SUFFIX
PLASTIC PACKAGE
CASE 221A
TO-220 TYPE

PIN 1. INPUT
2. GROUND
3. OUTPUT



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

TYPE NO./VOLTAGE

MC7805	5.0 Volts	MC7815	15 Volts
MC7806	6.0 Volts	MC7818	18 Volts
MC7808	8.0 Volts	MC7824	24 Volts
MC7812	12 Volts		

MC7800 Series

MC7800 Series MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
$T_A = +25^{\circ}\text{C}$	P_D	Internally Limited	Watts
Derate above $T_A = +25^{\circ}\text{C}$	$1/\theta_{JA}$	15.4	mW/ $^{\circ}\text{C}$
Thermal Resistance, Junction to Air	θ_{JA}	65	$^{\circ}\text{C}/\text{W}$
$T_C = +25^{\circ}\text{C}$	P_D	Internally Limited	Watts
Derate above $T_C = +95^{\circ}\text{C}$ (See Figure 1)	$1/\theta_{JC}$	200	mW/ $^{\circ}\text{C}$
Thermal Resistance, Junction to Case	θ_{JC}	5.0	$^{\circ}\text{C}/\text{W}$
Metal Package			
$T_A = +25^{\circ}\text{C}$	P_D	Internally Limited	Watts
Derate above $T_A = +25^{\circ}\text{C}$	$1/\theta_{JA}$	22.5	mW/ $^{\circ}\text{C}$
Thermal Resistance, Junction to Air	θ_{JA}	45	$^{\circ}\text{C}/\text{W}$
$T_C = +25^{\circ}\text{C}$	P_D	Internally Limited	Watts
Derate above $T_C = +65^{\circ}\text{C}$ (See Figure 2)	$1/\theta_{JC}$	182	mW/ $^{\circ}\text{C}$
Thermal Resistance, Junction to Case	θ_{JC}	5.5	$^{\circ}\text{C}/\text{W}$
Storage Junction Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Operating Junction Temperature Range	T_J	-55 to +150	$^{\circ}\text{C}$
		0 to +150	

DEFINITIONS

Line Regulation -- The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation -- The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current - That part of the input current that is not delivered to the load.

Output Noise Voltage -- The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability - Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC7800 Series

MC7805, C

ELECTRICAL CHARACTERISTICS (V_{in} = 10V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted).

Characteristic	Symbol	MC7805			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T _J = +25°C)	V _O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage (5.0 mA < I _O < 1.0 A, P _O < 15W) 7.0 Vdc < V _{in} < 20 Vdc 8.0 Vdc < V _{in} < 20 Vdc	V _O	—	—	—	4.75	5.0	5.25	Vdc
Line Regulation (T _J = +25°C, Note 2) 7.0 Vdc < V _{in} < 25 Vdc 8.0 Vdc < V _{in} < 12 Vdc	Reg _{in}	—	2.0	50	—	7.0	100	mV
Load Regulation (T _J = +25°C, Note 2) 5.0 mA < I _O < 1.5 A 250 mA < I _O < 750 mA	Reg _{load}	—	25	100	—	40	100	mV
Quiescent Current (T _J = +25°C)	I _B	—	3.2	6.0	—	4.3	8.0	mA
Quiescent Current Change 7.0 Vdc < V _{in} < 25 Vdc 8.0 Vdc < V _{in} < 25 Vdc 5.0 mA < I _O < 1.0 A	ΔI _B	—	—	—	—	—	1.3	mA
Ripple Rejection 8.0 Vdc < V _{in} < 18 Vdc, f = 120 Hz	RR	68	75	—	—	68	—	dB
Dropout Voltage (I _O = 1.0 A, T _J = +25°C)	V _{in} - V _O	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T _A = +25°C) 10 Hz < f < 100 kHz	V _n	—	10	40	—	10	—	μV/V _O
Output Resistance f = 1.0 kHz	R _O	—	17	—	—	17	—	mΩ
Short-Circuit Current Limit (T _A = +25°C) V _{in} = 35 Vdc	I _{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T _J = +25°C)	I _{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV _O	—	±0.6	—	—	-1.1	—	mV/°C

MC7805A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1) unless otherwise noted)

Characteristics	Symbol	MC7805A			MC7805AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T _J = +25°C)	V _O	4.9	5.0	5.1	4.9	5.0	5.1	Vdc
Output Voltage (5.0 mA < I _O < 1.0 A, P _O < 15 W) 7.5 Vdc < V _{in} < 20 Vdc	V _O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) 7.5 Vdc < V _{in} < 25 Vdc, I _O = 500 mA 8.0 Vdc < V _{in} < 12 Vdc 8.0 Vdc < V _{in} < 12 Vdc, T _J = +25°C 7.3 Vdc < V _{in} < 20 Vdc, T _J = +25°C	Reg _{in}	—	2.0	10	—	7.0	50	mV
Load Regulation (Note 2) 5.0 mA < I _O < 1.5 A 5.0 mA < I _O < 1.0 A 5.0 mA < I _O < 1.5 A, T _J = +25°C 250 mA < I _O < 750 mA	Reg _{load}	—	25	50	—	25	100	mV
Quiescent Current T _J = +25°C	I _B	—	3.2	5.0	—	4.3	6.0	mA
Quiescent Current Change 8.0 Vdc < V _{in} < 25 Vdc, I _O = 500 mA 7.5 Vdc < V _{in} < 20 Vdc, T _J = +25°C 5.0 mA < I _O < 1.0 A	ΔI _B	—	0.3	0.5	—	—	0.8	mA
Ripple Rejection 8.0 Vdc < V _{in} < 18 Vdc, f = 120 Hz, T _J = +25°C 8.0 Vdc < V _{in} < 18 Vdc, f = 120 Hz, I _O = 500 mA	RR	68	75	—	—	68	—	dB
Dropout Voltage (I _O = 1.0 A, T _J = +25°C)	V _{in} - V _O	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T _A = +25°C) 10 Hz < f < 100 kHz	V _n	—	10	40	—	10	—	μV/V _O
Output Resistance (f = 1.0 kHz)	R _O	—	17	—	—	17	—	mΩ
Short-Circuit Current Limit (T _A = +25°C) V _{in} = 35 Vdc	I _{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T _J = +25°C)	I _{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV _O	—	±0.6	—	—	-1.1	—	mV/°C

Notes: 1. T_{low} = -55°C for MC78XX, A
= 0°C for MC78XXC, AC

T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7806, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 11\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7806			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$)	V_O	—	—	—	5.7	6.0	6.3	Vdc
8.0 Vdc $\leq V_{in} \leq 21\text{ Vdc}$		—	—	—	—	—	—	
9.0 Vdc $\leq V_{in} \leq 21\text{ Vdc}$		5.65	6.0	6.35	—	—	—	
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2)	Reg_{in}	—	3.0	60	—	9.0	120	mV
8.0 Vdc $\leq V_{in} \leq 25\text{ Vdc}$		—	2.0	30	—	3.0	60	
9.0 Vdc $\leq V_{in} \leq 13\text{ Vdc}$		—	—	—	—	—	—	
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2)	Reg_{load}	—	27	100	—	43	120	mV
5.0 mA $\leq I_O \leq 1.5\text{ A}$		—	9.0	30	—	16	60	
250 mA $\leq I_O \leq 750\text{ mA}$		—	—	—	—	—	—	
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.2	6.0	—	4.3	8.0	mA
Quiescent Current Change	ΔI_B	—	—	—	—	—	1.3	mA
8.0 Vdc $\leq V_{in} \leq 25\text{ Vdc}$		—	0.3	0.8	—	—	—	
9.0 Vdc $\leq V_{in} \leq 25\text{ Vdc}$		—	0.04	0.5	—	—	0.5	
5.0 mA $\leq I_O \leq 1.0\text{ A}$		—	—	—	—	—	—	
Ripple Rejection	RR	65	73	—	—	65	—	dB
9.0 Vdc $\leq V_{in} \leq 19\text{ Vdc}$, $f = 120\text{ Hz}$		—	—	—	—	—	—	
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$)	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
10 Hz $\leq f \leq 100\text{ kHz}$		—	—	—	—	—	—	
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	17	—	—	17	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$)	I_{sc}	—	0.2	1.2	—	0.2	—	A
$V_{in} = 35\text{ Vdc}$		—	—	—	—	—	—	
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 0.7	—	—	0.8	—	$\text{mV}/^\circ\text{C}$

MC7806A, AC

ELECTRICAL CHARACTERISTICS ($V_{in} = 11\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7806A			MC7806AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	5.88	6.0	6.12	5.88	6.0	6.12	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$)	V_O	5.76	6.0	6.24	5.76	6.0	6.24	Vdc
8.6 Vdc $\leq V_{in} \leq 21\text{ Vdc}$		—	—	—	—	—	—	
Line Regulation (Note 2)	Reg_{in}	—	3.0	11	—	9.0	60	mV
8.6 Vdc $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$		—	5.0	15	—	11	60	
9.0 Vdc $\leq V_{in} \leq 13\text{ Vdc}$		—	2.0	5.0	—	3.0	30	
9.0 Vdc $\leq V_{in} \leq 13\text{ Vdc}$, $T_J = +25^\circ\text{C}$		—	4.0	11	—	9.0	60	
8.3 Vdc $\leq V_{in} \leq 21\text{ Vdc}$, $T_J = +25^\circ\text{C}$		—	—	—	—	—	—	
Load Regulation (Note 2)	Reg_{load}	—	27	50	—	—	—	mV
5.0 mA $\leq I_O \leq 1.5\text{ A}$		—	—	—	—	43	100	
5.0 mA $\leq I_O \leq 1.0\text{ A}$		—	—	—	—	43	100	
5.0 mA $\leq I_O \leq 1.5\text{ A}$, $T_J = +25^\circ\text{C}$		—	9.0	25	—	16	50	
250 mA $\leq I_O \leq 750\text{ mA}$		—	—	—	—	—	—	
Quiescent Current	I_B	—	—	5.0	—	—	6.0	mA
$T_J = +25^\circ\text{C}$		—	3.2	4.0	—	4.3	6.0	
Quiescent Current Change	ΔI_B	—	0.3	0.5	—	—	0.8	mA
9.0 Vdc $\leq V_{in} \leq 25\text{ Vdc}$, $I_O = 500\text{ mA}$		—	0.2	0.5	—	—	0.8	
8.6 Vdc $\leq V_{in} \leq 21\text{ Vdc}$, $T_J = +25^\circ\text{C}$		—	0.04	0.2	—	—	0.5	
5.0 mA $\leq I_O \leq 1.0\text{ A}$		—	—	—	—	—	—	
Ripple Rejection	RR	65	73	—	—	—	—	dB
9.0 Vdc $\leq V_{in} \leq 19\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$		—	—	—	—	—	—	
9.0 Vdc $\leq V_{in} \leq 19\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$		65	73	—	65	—	—	
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$)	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
10 Hz $\leq f \leq 100\text{ kHz}$		—	—	—	—	—	—	
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	17	—	—	17	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$)	I_{sc}	—	0.2	1.2	—	0.2	—	A
$V_{in} = 35\text{ Vdc}$		—	—	—	—	—	—	
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 0.7	—	—	-0.8	—	$\text{mV}/^\circ\text{C}$

Notes: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, A
 $= 0^\circ\text{C}$ for MC78XXC, AC

$T_{high} = +150^\circ\text{C}$ for MC78XX, A
 $= +125^\circ\text{C}$ for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7808, C

ELECTRICAL CHARACTERISTICS ($V_{in} = 14\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7808			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.7	8.0	8.3	7.7	8.0	8.3	Vdc
Output Voltage ($5.0\text{ mA} < I_O < 1.0\text{ A}$, $P_O < 15\text{ W}$) $10.5\text{ Vdc} < V_{in} < 23\text{ Vdc}$ $11.5\text{ Vdc} < V_{in} < 23\text{ Vdc}$	V_O	—	—	—	7.6	8.0	8.4	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) $10.5\text{ Vdc} < V_{in} < 25\text{ Vdc}$ $11\text{ Vdc} < V_{in} < 17\text{ Vdc}$	Reg_{in}	—	3.0	80	—	12	160	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) $5.0\text{ mA} < I_O < 1.5\text{ A}$ $250\text{ mA} < I_O < 750\text{ mA}$	Reg_{load}	—	28	100	—	45	160	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.2	6.0	—	4.3	8.0	mA
Quiescent Current Change $10.5\text{ Vdc} < V_{in} < 25\text{ Vdc}$ $11.5\text{ Vdc} < V_{in} < 25\text{ Vdc}$ $5.0\text{ mA} < I_O < 1.0\text{ A}$	ΔI_B	—	—	—	—	—	1.0	mA
Ripple Rejection $11.5\text{ Vdc} < V_{in} < 21.5\text{ Vdc}$, $f = 120\text{ Hz}$	RR	62	70	—	—	62	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	V_{in-V_O}	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} < f < 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	18	—	—	18	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.0	—	—	-0.8	—	$\text{mV}/^\circ\text{C}$

MC7808A, AC

ELECTRICAL CHARACTERISTICS ($V_{in} = 14\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7808A			MC7808AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.84	8.0	8.16	7.84	8.0	8.16	Vdc
Output Voltage ($5.0\text{ mA} < I_O < 1.0\text{ A}$, $P_O < 15\text{ W}$) $10.6\text{ Vdc} < V_{in} < 23\text{ Vdc}$	V_O	7.7	8.0	8.3	7.7	8.0	8.3	Vdc
Line Regulation (Note 2) $10.6\text{ Vdc} < V_{in} < 25\text{ Vdc}$, $I_O = 500\text{ mA}$ $11\text{ Vdc} < V_{in} < 17\text{ Vdc}$ $11\text{ Vdc} < V_{in} < 17\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $10.4\text{ Vdc} < V_{in} < 23\text{ Vdc}$, $T_J = +25^\circ\text{C}$	Reg_{in}	—	4.0	13	—	12	80	mV
Load Regulation (Note 2) $5.0\text{ mA} < I_O < 1.5\text{ A}$ $5.0\text{ mA} < I_O < 1.0\text{ A}$ $5.0\text{ mA} < I_O < 1.5\text{ A}$, $T_J = +25^\circ\text{C}$ $250\text{ mA} < I_O < 750\text{ mA}$	Reg_{load}	—	28	50	—	—	—	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	—	—	5.0	—	—	6.0	mA
Quiescent Current Change $11\text{ Vdc} < V_{in} < 25\text{ Vdc}$, $I_O = 500\text{ mA}$ $10.6\text{ Vdc} < V_{in} < 23\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $5.0\text{ mA} < I_O < 1.0\text{ A}$	ΔI_B	—	0.3	0.5	—	—	0.8	mA
Ripple Rejection $11.5\text{ Vdc} < V_{in} < 21.5\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$ $11.5\text{ Vdc} < V_{in} < 21.5\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$	RR	62	70	—	—	—	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	V_{in-V_O}	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} < f < 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	18	—	—	18	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.0	—	—	-0.8	—	$\text{mV}/^\circ\text{C}$

Notes: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, A
 $= 0^\circ\text{C}$ for MC78XXC, AC

$T_{high} = +150^\circ\text{C}$ for MC78XX, A
 $= +125^\circ\text{C}$ for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7812, C

ELECTRICAL CHARACTERISTICS

($V_{in} = 19\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7812			MC7812C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	11.5	12	12.5	11.5	12	12.5	Vdc
Output Voltage ($5.0\text{ mA} < I_O < 1.0\text{ A}$, $P_O < 15\text{ W}$)	V_O	—	—	—	11.4	12	12.6	Vdc
14.5 Vdc $< V_{in} < 27\text{ Vdc}$		11.4	12	12.6	—	—	—	
15.5 Vdc $< V_{in} < 27\text{ Vdc}$		—	—	—	—	—	—	
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2)	Reg_{in}	—	5.0	120	—	13	240	mV
14.5 Vdc $< V_{in} < 30\text{ Vdc}$		—	3.0	60	—	6.0	120	
16 Vdc $< V_{in} < 22\text{ Vdc}$		—	—	—	—	—	—	
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2)	Reg_{load}	—	30	120	—	46	240	mV
5.0 mA $< I_O < 1.5\text{ A}$		—	10	60	—	17	120	
250 mA $< I_O < 750\text{ mA}$		—	—	—	—	—	—	
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.4	6.0	—	4.4	8.0	mA
Quiescent Current Change	ΔI_B	—	—	—	—	—	1.0	mA
14.5 Vdc $< V_{in} < 30\text{ Vdc}$		—	0.3	0.8	—	—	—	
15 Vdc $< V_{in} < 30\text{ Vdc}$		—	0.04	0.5	—	—	0.5	
5.0 mA $< I_O < 1.0\text{ A}$		—	—	—	—	—	—	
Ripple Rejection	RR	61	68	—	—	60	—	dB
15 Vdc $< V_{in} < 25\text{ Vdc}$, $f = 120\text{ Hz}$		—	—	—	—	—	—	
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$)	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
10 Hz $< f < 100\text{ kHz}$		—	—	—	—	—	—	
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	18	—	—	18	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$)	I_{sc}	—	0.2	1.2	—	0.2	—	A
$V_{in} = 35\text{ Vdc}$		—	—	—	—	—	—	
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.5	—	—	-1.0	—	$\text{mV}/^\circ\text{C}$

MC7812A, AC

ELECTRICAL CHARACTERISTICS

($V_{in} = 19\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7812A			MC7812AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	11.75	12	12.25	11.75	12	12.25	Vdc
Output Voltage ($5.0\text{ mA} < I_O < 1.0\text{ A}$, $P_O < 15\text{ W}$)	V_O	11.5	12	12.5	11.5	12	12.5	Vdc
14.8 Vdc $< V_{in} < 27\text{ Vdc}$		—	—	—	—	—	—	
Line Regulation	Reg_{in}	—	5.0	18	—	13	120	mV
14.8 Vdc $< V_{in} < 30\text{ Vdc}$, $I_O = 500\text{ mA}$		—	8.0	30	—	16	120	
16 Vdc $< V_{in} < 22\text{ Vdc}$		—	3.0	9.0	—	6.0	60	
14.5 Vdc $< V_{in} < 27\text{ Vdc}$, $T_J = +25^\circ\text{C}$		—	5.0	18	—	13	120	
Load Regulation (Note 2)	Reg_{load}	—	30	50	—	—	—	mV
5.0 mA $< I_O < 1.5\text{ A}$		—	—	—	—	46	100	
5.0 mA $< I_O < 1.0\text{ A}$		—	—	—	—	46	100	
5.0 mA $< I_O < 1.5\text{ A}$, $T_J = +25^\circ\text{C}$		—	—	—	—	46	100	
250 mA $< I_O < 750\text{ mA}$		—	10	25	—	17	50	
Quiescent Current	I_B	—	—	5.0	—	—	6.0	mA
$T_J = +25^\circ\text{C}$		—	3.4	4.0	—	4.4	6.0	
Quiescent Current Change	ΔI_B	—	0.3	0.5	—	—	0.8	mA
15 Vdc $< V_{in} < 30\text{ Vdc}$, $I_O = 500\text{ mA}$		—	0.2	0.5	—	—	0.8	
14.8 Vdc $< V_{in} < 27\text{ Vdc}$, $T_J = +25^\circ\text{C}$		—	0.04	0.2	—	—	0.5	
5.0 mA $< I_O < 1.0\text{ A}$		—	—	—	—	—	—	
Ripple Rejection	RR	61	68	—	—	—	—	dB
15 Vdc $< V_{in} < 25\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$		61	68	—	—	60	—	
15 Vdc $< V_{in} < 25\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$		—	—	—	—	—	—	
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in}-V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$)	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
10 Hz $< f < 100\text{ kHz}$		—	—	—	—	—	—	
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	18	—	—	18	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$)	I_{sc}	—	0.2	1.2	—	0.2	—	A
$V_{in} = 35\text{ Vdc}$		—	—	—	—	—	—	
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.5	—	—	-1.0	—	$\text{mV}/^\circ\text{C}$

Notes: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, A
 $= 0^\circ\text{C}$ for MC78XXC, AC

$T_{high} = +150^\circ\text{C}$ for MC78XX, A
 $= +125^\circ\text{C}$ for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7815, C

ELECTRICAL CHARACTERISTICS

($V_{in} = 23\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7815			MC7815C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	14.4	15	15.6	14.4	15	15.6	Vdc
Output Voltage ($5.0\text{ mA} < I_O < 1.0\text{ A}$, $P_O < 15\text{ W}$) $17.5\text{ Vdc} < V_{in} < 30\text{ Vdc}$ $18.5\text{ Vdc} < V_{in} < 30\text{ Vdc}$	V_O	—	—	—	14.25	15	15.75	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) $17.5\text{ Vdc} < V_{in} < 30\text{ Vdc}$ $20\text{ Vdc} < V_{in} < 26\text{ Vdc}$	Reg_{in}	—	6.0 3.0	150 75	—	13 6.0	300 150	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) $5.0\text{ mA} < I_O < 1.5\text{ A}$ $250\text{ mA} < I_O < 750\text{ mA}$	Reg_{load}	—	32 10	150 75	—	52 20	300 150	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.4	6.0	—	4.4	8.0	mA
Quiescent Current Change $17.5\text{ Vdc} < V_{in} < 30\text{ Vdc}$ $18.5\text{ Vdc} < V_{in} < 30\text{ Vdc}$ $5.0\text{ mA} < I_O < 1.0\text{ A}$	ΔI_B	—	— 0.3 0.04	— 0.8 0.5	—	— — —	1.0 — 0.5	mA
Ripple Rejection $18.5\text{ Vdc} < V_{in} < 28.5\text{ Vdc}$, $f = 120\text{ Hz}$	RR	60	66	—	—	58	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} < f < 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	19	—	—	19	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.8	—	—	-1.0	—	$\text{mV}/^\circ\text{C}$

MC7815A, AC

ELECTRICAL CHARACTERISTICS

($V_{in} = 23\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7815A			MC7815AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	14.7	15	15.3	14.7	15	15.3	Vdc
Output Voltage ($5.0\text{ mA} < I_O < 1.0\text{ A}$, $P_O < 15\text{ W}$) $17.9\text{ Vdc} < V_{in} < 30\text{ Vdc}$	V_O	14.4	15	15.6	14.4	15	15.6	Vdc
Line Regulation (Note 2) $17.9\text{ Vdc} < V_{in} < 30\text{ Vdc}$, $I_O = 500\text{ mA}$ $20\text{ Vdc} < V_{in} < 26\text{ Vdc}$ $20\text{ Vdc} < V_{in} < 26\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $17.5\text{ Vdc} < V_{in} < 30\text{ Vdc}$, $T_J = +25^\circ\text{C}$	Reg_{in}	—	6.0 9.0 3.0 6.0	22 30 10 22	—	13 16 6.0 13	150 150 75 150	mV
Load Regulation (Note 2) $5.0\text{ mA} < I_O < 1.5\text{ A}$ $5.0\text{ mA} < I_O < 1.0\text{ A}$ $5.0\text{ mA} < I_O < 1.5\text{ A}$, $T_J = +25^\circ\text{C}$ $250\text{ mA} < I_O < 750\text{ mA}$	Reg_{load}	—	32 — — 10	50 — — 25	—	— 52 52 20	— 100 100 50	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	—	— 3.4	5.5 4.5	—	— 4.4	6.0 6.0	mA
Quiescent Current Change $17.5\text{ Vdc} < V_{in} < 30\text{ Vdc}$, $I_O = 500\text{ mA}$ $17.5\text{ Vdc} < V_{in} < 30\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $5.0\text{ mA} < I_O < 1.0\text{ A}$	ΔI_B	—	0.3 0.2 0.04	0.5 0.5 0.2	—	— — —	0.8 0.8 0.5	mA
Ripple Rejection $18.5\text{ Vdc} < V_{in} < 28.5\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$ $18.5\text{ Vdc} < V_{in} < 28.5\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$	RR	60 60	66 66	— —	— 58	— —	— —	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} < f < 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	19	—	—	19	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 1.8	—	—	-1.0	—	$\text{mV}/^\circ\text{C}$

Notes: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, A
 $= 0^\circ\text{C}$ for MC78XXC, AC

$T_{high} = +150^\circ\text{C}$ for MC78XX, A
 $= +125^\circ\text{C}$ for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7818, C

ELECTRICAL CHARACTERISTICS

($V_{in} = 27\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7818			MC7818C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	17.3	18	18.7	17.3	18	18.7	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) 21 Vdc $\leq V_{in} \leq 33\text{ Vdc}$ 22 Vdc $\leq V_{in} \leq 33\text{ Vdc}$	V_O	— 17.1	— 18	— 18.9	17.1	18	18.9	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) 21 Vdc $\leq V_{in} \leq 33\text{ Vdc}$ 24 Vdc $\leq V_{in} \leq 30\text{ Vdc}$	Reg_{in}	— —	7.0 4.0	180 90	— —	25 10	360 180	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) 5.0 mA $\leq I_O \leq 1.5\text{ A}$ 250 mA $\leq I_O \leq 750\text{ mA}$	Reg_{load}	— —	35 12	180 90	— —	55 22	360 180	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.5	6.0	—	4.5	8.0	mA
Quiescent Current Change 21 Vdc $\leq V_{in} \leq 33\text{ Vdc}$ 22 Vdc $\leq V_{in} \leq 33\text{ Vdc}$ 5.0 mA $\leq I_O \leq 1.0\text{ A}$	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	1.0 — 0.5	mA
Ripple Rejection 22 Vdc $\leq V_{in} \leq 32\text{ Vdc}$, $f = 120\text{ Hz}$	RR	59	65	—	57	—	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/\sqrt{\text{O}}$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	19	—	—	19	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 2.3	—	—	-1.0	—	$\text{mV}/^\circ\text{C}$

MC7818A, AC

ELECTRICAL CHARACTERISTICS

($V_{in} = 27\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7818A			MC7818AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	17.64	18	18.36	17.64	18	18.36	Vdc
Output Voltage ($5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P_O \leq 15\text{ W}$) 21 Vdc $\leq V_{in} \leq 33\text{ Vdc}$	V_O	17.3	18	18.7	17.3	18	18.7	Vdc
Line Regulation (Note 2) 21 Vdc $\leq V_{in} \leq 33\text{ Vdc}$, $I_O = 500\text{ mA}$ 24 Vdc $\leq V_{in} \leq 30\text{ Vdc}$ 24 Vdc $\leq V_{in} \leq 30\text{ Vdc}$, $T_J = +25^\circ\text{C}$ 20.6 Vdc $\leq V_{in} \leq 33\text{ Vdc}$, $T_J = +25^\circ\text{C}$	Reg_{in}	— — — —	7.0 12 4.0 7.0	31 45 15 31	— — — —	25 28 10 25	180 180 90 180	mV
Load Regulation (Note 2) 5.0 mA $\leq I_O \leq 1.5\text{ A}$ 5.0 mA $\leq I_O \leq 1.0\text{ A}$ 5.0 mA $\leq I_O \leq 1.5\text{ A}$, $T_J = +25^\circ\text{C}$ 250 mA $\leq I_O \leq 750\text{ mA}$	Reg_{load}	— — — —	35 — — 12	50 — — 25	— — — —	— 55 55 22	— 100 100 50	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	— —	— 3.4	5.5 4.5	— —	— 4.5	6.0 6.0	mA
Quiescent Current Change 21 Vdc $\leq V_{in} \leq 33\text{ Vdc}$, $I_O = 500\text{ mA}$ 21 Vdc $\leq V_{in} \leq 33\text{ Vdc}$, $T_J = +25^\circ\text{C}$ 5.0 mA $\leq I_O \leq 1.0\text{ A}$	ΔI_B	— — —	0.3 0.2 0.04	0.5 0.5 0.2	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 22 Vdc $\leq V_{in} \leq 32\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$ 22 Vdc $\leq V_{in} \leq 32\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$	RR	59 59	65 65	— —	— —	— 57	— —	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) 10 Hz $\leq f \leq 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/\sqrt{\text{O}}$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	19	—	—	19	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 2.3	—	—	-1.0	—	$\text{mV}/^\circ\text{C}$

Notes: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, A
= 0°C for MC78XXC, AC

$T_{high} = +150^\circ\text{C}$ for MC78XX, A
= $+125^\circ\text{C}$ for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800 Series

MC7824, C

ELECTRICAL CHARACTERISTICS

($V_{in} = 33\text{ V}$, $I_O = 500\text{ mA}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7824			MC7824C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	23	24	25	23	24	25	Vdc
Output Voltage ($5.0\text{ mA} < I_O < 1.0\text{ A}$, $P_O < 15\text{ W}$) $27\text{ Vdc} < V_{in} < 38\text{ Vdc}$ $28\text{ Vdc} < V_{in} < 38\text{ Vdc}$	V_O	—	—	—	22.8	24	25.2	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, Note 2) $27\text{ Vdc} < V_{in} < 38\text{ Vdc}$ $30\text{ Vdc} < V_{in} < 36\text{ Vdc}$	Reg_{in}	—	10	240	—	31	480	mV
Load Regulation ($T_J = +25^\circ\text{C}$, Note 2) $5.0\text{ mA} < I_O < 1.5\text{ A}$ $250\text{ mA} < I_O < 750\text{ mA}$	Reg_{load}	—	40	240	—	60	480	mV
Quiescent Current ($T_J = +25^\circ\text{C}$)	I_B	—	3.6	6.0	—	4.6	8.0	mA
Quiescent Current Change $27\text{ Vdc} < V_{in} < 38\text{ Vdc}$ $28\text{ Vdc} < V_{in} < 38\text{ Vdc}$ $5.0\text{ mA} < I_O < 1.0\text{ A}$	ΔI_B	—	—	—	—	—	1.0	mA
Ripple Rejection $28\text{ Vdc} < V_{in} < 38\text{ Vdc}$, $f = 120\text{ Hz}$	RR	56	62	—	—	54	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} < f < 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	20	—	—	20	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 3.0	—	—	-1.5	—	$\text{mV}/^\circ\text{C}$

MC7824A, AC

ELECTRICAL CHARACTERISTICS

($V_{in} = 33\text{ V}$, $I_O = 1.0\text{ A}$, $T_J = T_{low}$ to T_{high} (Note 1) unless otherwise noted.)

Characteristic	Symbol	MC7824A			MC7824AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	23.5	24	24.5	23.5	24	24.5	Vdc
Output Voltage ($5.0\text{ mA} < I_O < 1.0\text{ A}$, $P_O < 15\text{ W}$) $27.3\text{ Vdc} < V_{in} < 38\text{ Vdc}$	V_O	23	24	25	23	24	25	Vdc
Line Regulation (Note 2) $27\text{ Vdc} < V_{in} < 38\text{ Vdc}$, $I_O = 500\text{ mA}$ $30\text{ Vdc} < V_{in} < 36\text{ Vdc}$ $30\text{ Vdc} < V_{in} < 36\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $26.7\text{ Vdc} < V_{in} < 38\text{ Vdc}$, $T_J = +25^\circ\text{C}$	Reg_{in}	—	10	36	—	31	240	mV
Load Regulation (Note 2) $5.0\text{ mA} < I_O < 1.5\text{ A}$ $5.0\text{ mA} < I_O < 1.0\text{ A}$ $5.0\text{ mA} < I_O < 1.5\text{ A}$, $T_J = +25^\circ\text{C}$ $250\text{ mA} < I_O < 750\text{ mA}$	Reg_{load}	—	40	50	—	—	—	mV
Quiescent Current $T_J = +25^\circ\text{C}$	I_B	—	3.6	6.0	—	4.6	6.0	mA
Quiescent Current Change $27.3\text{ Vdc} < V_{in} < 38\text{ Vdc}$, $I_O = 500\text{ mA}$ $27.3\text{ Vdc} < V_{in} < 38\text{ Vdc}$, $T_J = +25^\circ\text{C}$ $5.0\text{ mA} < I_O < 1.0\text{ A}$	ΔI_B	—	0.3	0.5	—	—	0.8	mA
Ripple Rejection $28\text{ Vdc} < V_{in} < 38\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$ $28\text{ Vdc} < V_{in} < 38\text{ Vdc}$, $f = 120\text{ Hz}$, $I_O = 500\text{ mA}$	RR	56	62	—	—	—	—	dB
Dropout Voltage ($I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage ($T_A = +25^\circ\text{C}$) $10\text{ Hz} < f < 100\text{ kHz}$	V_n	—	10	40	—	10	—	$\mu\text{V}/V_O$
Output Resistance ($f = 1.0\text{ kHz}$)	R_O	—	20	—	—	20	—	$\text{m}\Omega$
Short-Circuit Current Limit ($T_A = +25^\circ\text{C}$) $V_{in} = 35\text{ Vdc}$	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current ($T_J = +25^\circ\text{C}$)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	± 3.0	—	—	-1.5	—	$\text{mV}/^\circ\text{C}$

Notes: 1. $T_{low} = -55^\circ\text{C}$ for MC78XX, A

$= 0^\circ\text{C}$ for MC78XXC, AC

$T_{high} = +150^\circ\text{C}$ for MC78XX, A

$= +125^\circ\text{C}$ for MC78XXC, AC

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION
versus AMBIENT TEMPERATURE (Case 221A)

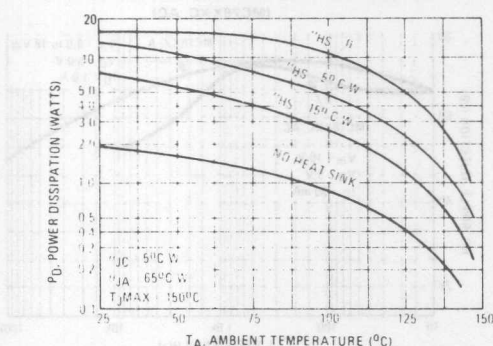


FIGURE 2 – WORST CASE POWER DISSIPATION
versus AMBIENT TEMPERATURE (Case 1)

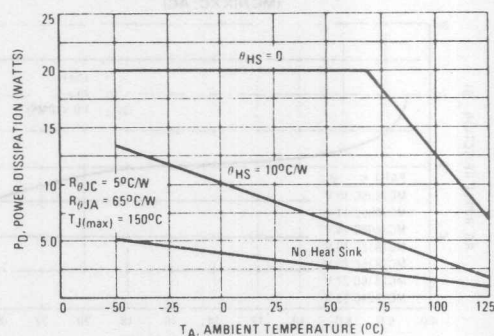


FIGURE 3 – INPUT OUTPUT DIFFERENTIAL AS A
FUNCTION OF JUNCTION TEMPERATURE
(MC78XXC, AC)

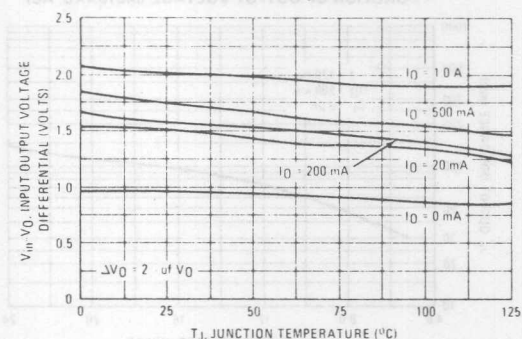


FIGURE 4 – INPUT OUTPUT DIFFERENTIAL AS A
FUNCTION OF JUNCTION TEMPERATURE
(MC78XX, A)

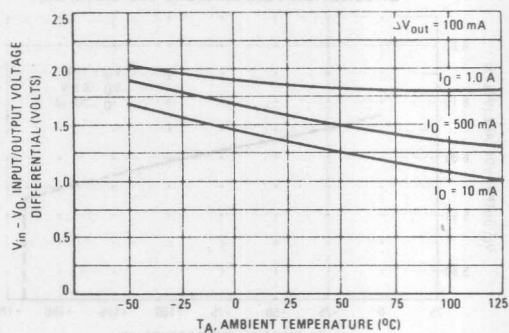


FIGURE 5 – PEAK OUTPUT CURRENT AS A FUNCTION
OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE
(MC78XXC, AC)

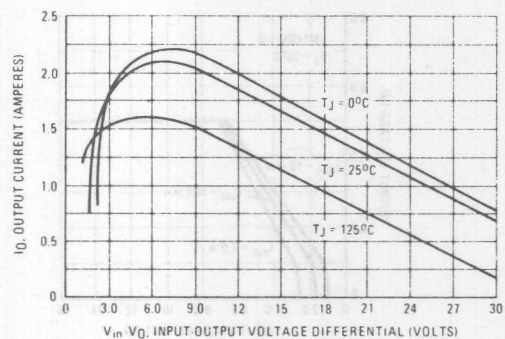
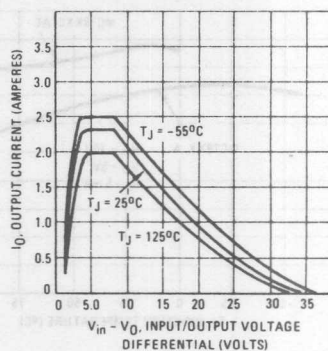


FIGURE 6 – PEAK OUTPUT CURRENT AS A
FUNCTION OF INPUT-OUTPUT DIFFERENTIAL
VOLTAGE (MC78XX, A)



TYPICAL CHARACTERISTICS (continued)
($T_A = 25^\circ\text{C}$ unless otherwise noted.)

FIGURE 7 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES (MC78XXC, AC)

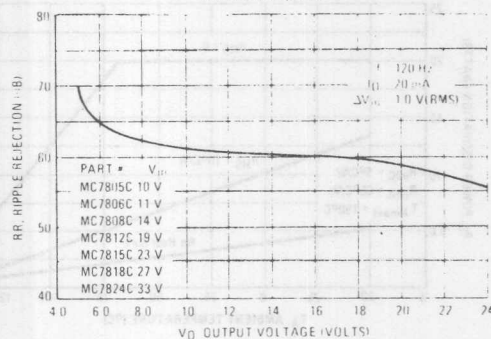


FIGURE 8 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY (MC78XXC, AC)

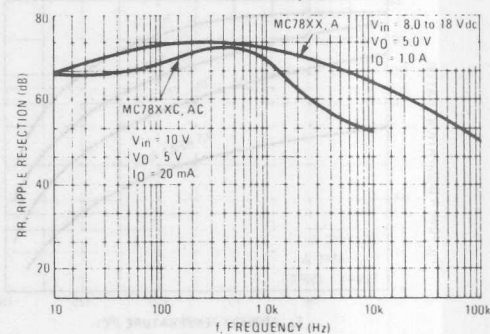


FIGURE 9 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC)

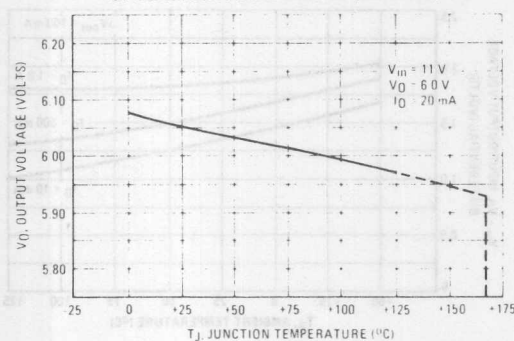


FIGURE 10 – OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE (MC78XXC, AC)

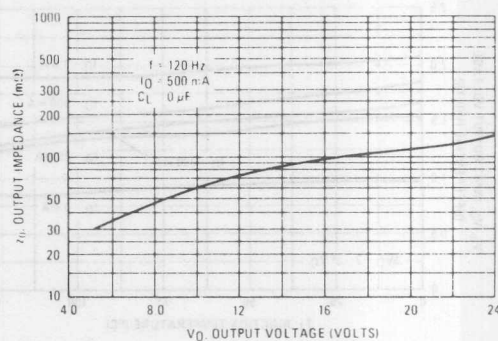


FIGURE 11 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE (MC78XXC, AC)

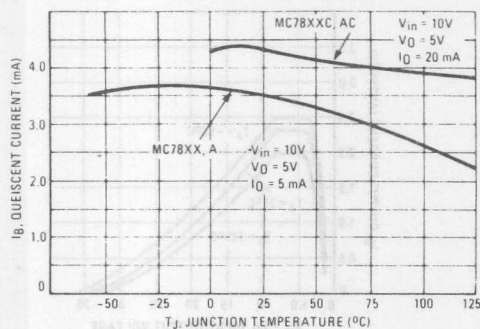
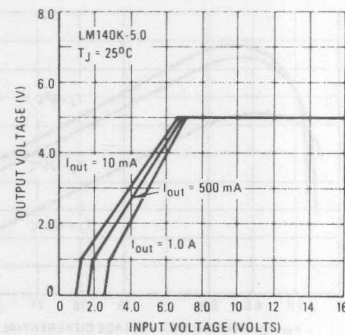


FIGURE 12 – DROPOUT CHARACTERISTICS (MC78XX, A)



MC7800 Series

APPLICATIONS INFORMATION

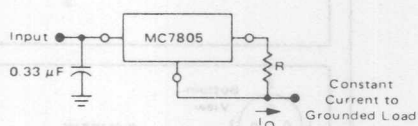
Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected

to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 13 – CURRENT REGULATOR



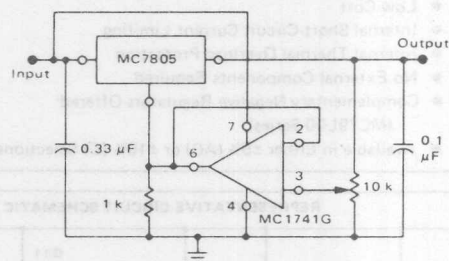
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5 \text{ V}}{R} + I_Q$$

$$I_Q \approx 1.5 \text{ mA over line and load changes}$$

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 14 – ADJUSTABLE OUTPUT REGULATOR

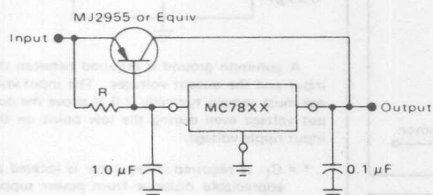


$$V_O, 7.0 \text{ V to } 20 \text{ V}$$

$$V_{IN} \quad V_O \geq 2.0 \text{ V}$$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

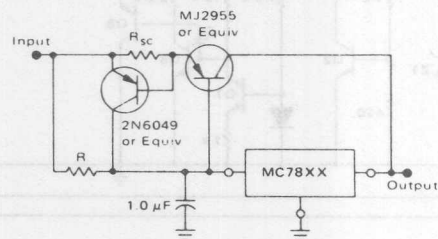
FIGURE 15 – CURRENT BOOST REGULATOR



XX - 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 16 – SHORT-CIRCUIT PROTECTION



XX - 2 digits of type number indicating voltage.

The circuit of Figure 15 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{sc} , and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MC78L00C, AC Series

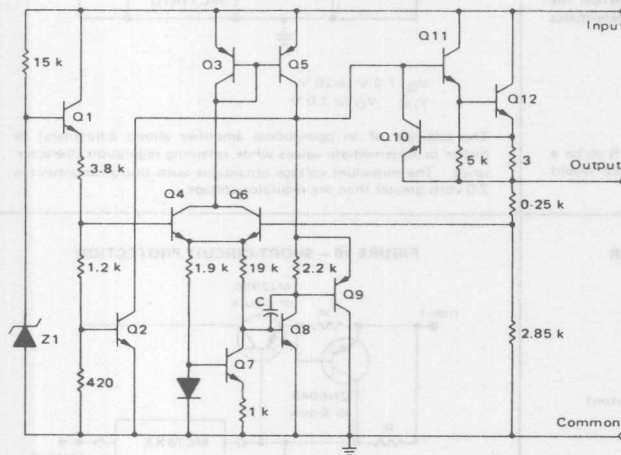
THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either $\pm 5\%$ (AC) or $\pm 10\%$ (C) Selections

REPRESENTATIVE CIRCUIT SCHEMATIC

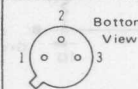


Device No. :10%	Device No. :5%	Nominal Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

P SUFFIX
CASE 29
TO-92

Pin 1. Output
2. Ground
3. Input

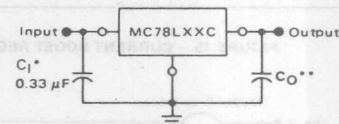


G SUFFIX
CASE 79
TO-39

Pin 1. Input
2. Output
3. Ground

(Case connected to pin 3)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_1 is required if regulator is located an appreciable distance from power supply filter.

** = C_0 is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Device	Temperature Range	Package
MC78LXXACG	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Metal Can
MC78LXXACP	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Plastic Transistor
MC78LXXCG	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Metal Can
MC78LXXCP	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Plastic Transistor

XX indicates nominal voltage

MC78L00C, AC Series

MC78L00 Series MAXIMUM RATINGS (T_A = +125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V – 8.0 V) (12 V – 18 V) (24 V)	V _I	30 35 40	Vdc
Storage Junction Temperature Range	T _{stg}	-65 to +150	°C
Operating Junction Temperature Range	T _J	0 to +150	°C

MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L05C			MC78L05AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T _J = +25°C)	V _O	4.6	5.0	5.4	4.8	5.0	5.2	Vdc
Input Regulation (T _J = +25°C, I _O = 40 mA) 7.0 Vdc ≤ V _I ≤ 20 Vdc 8.0 Vdc ≤ V _I ≤ 20 Vdc	Reg _{line}	—	55 45	200 150	—	55 45	150 100	mV
Load Regulation (T _J = +25°C, 1.0 mA ≤ I _O ≤ 100 mA) (T _J = +25°C, 1.0 mA ≤ I _O ≤ 40 mA)	Reg _{load}	—	11 5.0	60 30	—	11 5.0	60 30	mV
Output Voltage (7.0 Vdc ≤ V _I ≤ 20 Vdc, 1.0 mA ≤ I _O ≤ 40 mA) (V _I = 10 V, 1.0 mA ≤ I _O ≤ 70 mA)	V _O	4.5 4.5	—	5.5 5.5	4.75 4.75	—	5.25 5.25	Vdc
Input Bias Current (T _J = +25°C) (T _J = +125°C)	I _{IB}	—	3.8 —	6.0 5.5	—	3.8 —	6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V _I ≤ 20 Vdc) (1.0 mA ≤ I _O ≤ 40 mA)	ΔI _{IB}	—	—	1.5 0.2	—	—	1.5 0.1	mA
Output Noise Voltage (T _A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V _N	—	40	—	—	40	—	μV
Long-Term Stability	ΔV _O /Δt	—	12	—	—	12	—	mV/1.0 k Hrs
Ripple Rejection (I _O = 40 mA, f = 120 Hz, 8.0 V ≤ V _I ≤ 18 V, T _J = +25°C)	RR	40	49	—	41	49	—	dB
Input-Output Voltage Differential (T _J = +25°C)	V _I /V _O	—	1.7	—	—	1.7	—	Vdc

MC78L00C, AC Series

MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS ($V_I = 14\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L08C			MC78L08AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.36	8.0	8.64	7.7	8.0	8.3	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $10.5\text{ Vdc} \leq V_I \leq 23\text{ Vdc}$ $11\text{ Vdc} \leq V_I \leq 23\text{ Vdc}$	Reg _{line}	—	20	200	—	20	175	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Reg _{load}	—	15	80	—	15	80	mV
Output Voltage ($10.5\text{ Vdc} \leq V_I \leq 23\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 14\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	7.2	—	8.8	7.6	—	8.4	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	3.0	6.0	—	3.0	6.0	mA
Input Bias Current Change ($11\text{ Vdc} \leq V_I \leq 23\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_N	—	52	—	—	60	—	μV
Long-Term Stability	$\Delta V_O/\Delta t$	—	20	—	—	20	—	mV/1.0 k Hrs.
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $12\text{ V} \leq V_I \leq 23\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	36	55	—	37	57	—	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I/V_O	—	1.7	—	—	1.7	—	Vdc

MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS ($V_I = 19\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L12C			MC78L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	11.1	12	12.9	11.5	12	12.5	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $14.5\text{ Vdc} \leq V_I \leq 27\text{ Vdc}$ $16\text{ Vdc} \leq V_I \leq 27\text{ Vdc}$	Reg _{line}	—	120	250	—	120	250	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Reg _{load}	—	20	100	—	20	100	mV
Output Voltage ($14.5\text{ Vdc} \leq V_I \leq 27\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 19\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	10.8	—	13.2	11.4	—	12.6	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	4.2	6.5	—	4.2	6.5	mA
Input Bias Current Change ($16\text{ Vdc} \leq V_I \leq 27\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_N	—	80	—	—	80	—	μV
Long-Term Stability	$\Delta V_O/\Delta t$	—	24	—	—	24	—	mV/1.0 k Hrs.
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $15\text{ V} \leq V_I \leq 25\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	36	42	—	37	42	—	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I/V_O	—	1.7	—	—	1.7	—	Vdc

MC78L00C, AC Series

MC78L15C, MC78L15AC ELECTRICAL CHARACTERISTICS ($V_I = 23\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L15C			MC78L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	13.8	15	16.2	14.4	15	15.6	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $17.5\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$ $20\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$	Reg_{line}	—	130	300	—	130	300	mV
		—	110	250	—	110	250	
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Reg_{load}	—	25	150	—	25	150	mV
		—	12	75	—	12	75	
Output Voltage ($17.5\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 23\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	13.5	—	16.5	14.25	—	15.75	Vdc
		13.5	—	16.5	14.25	—	15.75	
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	4.4	6.5	—	4.4	6.5	mA
		—	—	6.0	—	—	6.0	
Input Bias Current Change ($20\text{ Vdc} \leq V_I \leq 30\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
		—	—	0.2	—	—	0.1	
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_N	—	90	—	—	90	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	30	—	—	30	—	mV/1.0 k Hrs.
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $18.5\text{ V} \leq V_I \leq 28.5\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	33	39	—	34	39	—	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I / V_O	—	1.7	—	—	1.7	—	Vdc

MC78L18C, MC78L18AC ELECTRICAL CHARACTERISTICS ($V_I = 27\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L18C			MC78L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	16.6	18	19.4	17.3	18	18.7	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) $21.4\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$ $20.7\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$ $22\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$ $21\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$	Reg_{line}	—	32	325	—	45	325	mV
		—	27	275	—	35	275	
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Reg_{load}	—	30	170	—	30	170	mV
		—	15	85	—	15	85	
Output Voltage ($21.4\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($20.7\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) ($V_I = 27\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$) ($V_I = 27\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	16.2	—	17.8	17.1	—	18.9	Vdc
		16.2	—	17.8	17.1	—	18.9	
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	3.1	6.5	—	3.1	6.5	mA
		—	—	6.0	—	—	6.0	
Input Bias Current Change ($22\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$) ($21\text{ Vdc} \leq V_I \leq 33\text{ Vdc}$) ($1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
		—	—	0.2	—	—	0.1	
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_N	—	150	—	—	150	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	45	—	—	45	—	mV/1.0 k Hrs.
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $23\text{ V} \leq V_I \leq 33\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	32	46	—	33	48	—	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I / V_O	—	1.7	—	—	1.7	—	Vdc

MC78L00C, AC Series

MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS ($V_I = 33\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC78L24C			MC78L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	22.1	24	25.9	23	24	25	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) 27.5 Vdc $\leq V_I \leq 38\text{ Vdc}$ 28 Vdc $\leq V_I \leq 38\text{ Vdc}$ 27 Vdc $\leq V_I \leq 38\text{ Vdc}$	Reg _{line}	—	35	350	—	—	—	mV
		—	30	300	—	50	300	
		—	—	—	—	60	350	
		—	—	—	—	—	—	
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$)	Reg _{load}	—	40	200	—	40	200	mV
		—	20	100	—	20	100	
Output Voltage (28 Vdc $\leq V_I \leq 38\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) (27 Vdc $\leq V_I \leq 38\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) (28 Vdc $\leq V_I \leq 33\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$) (27 Vdc $\leq V_I \leq 33\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	21.6	—	26.4	—	—	—	Vdc
		—	—	—	22.8	—	25.2	
		21.6	—	26.4	—	—	—	
		—	—	—	22.8	—	25.2	
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	3.1	6.5	—	3.1	6.5	mA
		—	—	6.0	—	—	6.0	
Input Bias Current Change (28 Vdc $\leq V_I \leq 38\text{ Vdc}$) (1.0 mA $\leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
		—	—	0.2	—	—	0.1	
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} < f < 100\text{ kHz}$)	V_N	—	200	—	—	200	—	μV
Long-Term Stability	$\Delta V_O/\Delta t$	—	56	—	—	56	—	mV/1.0 k Hrs.
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $29\text{ V} \leq V_I \leq 35\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	30	43	—	31	45	—	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I/V_O	—	1.7	—	—	1.7	—	Vdc

Characteristic	Symbol	MC78L24C			MC78L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	22.1	24	25.9	23	24	25	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$, $I_O = 40\text{ mA}$) 27.5 Vdc $\leq V_I \leq 38\text{ Vdc}$ 28 Vdc $\leq V_I \leq 38\text{ Vdc}$ 27 Vdc $\leq V_I \leq 38\text{ Vdc}$	Reg _{line}	—	35	350	—	—	—	mV
		—	30	300	—	50	300	
		—	—	—	—	60	350	
		—	—	—	—	—	—	
Load Regulation ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 100\text{ mA}$) ($T_J = +25^\circ\text{C}$, $1.0\text{ mA} < I_O < 40\text{ mA}$)	Reg _{load}	—	40	200	—	40	200	mV
		—	20	100	—	20	100	
Output Voltage (28 Vdc $\leq V_I \leq 38\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) (27 Vdc $\leq V_I \leq 38\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$) (28 Vdc $\leq V_I \leq 33\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$) (27 Vdc $\leq V_I \leq 33\text{ V}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$)	V_O	21.6	—	26.4	—	—	—	Vdc
		—	—	—	22.8	—	25.2	
		21.6	—	26.4	—	—	—	
		—	—	—	22.8	—	25.2	
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	3.1	6.5	—	3.1	6.5	mA
		—	—	6.0	—	—	6.0	
Input Bias Current Change (28 Vdc $\leq V_I \leq 38\text{ Vdc}$) (1.0 mA $\leq I_O \leq 40\text{ mA}$)	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
		—	—	0.2	—	—	0.1	
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} < f < 100\text{ kHz}$)	V_N	—	200	—	—	200	—	μV
Long-Term Stability	$\Delta V_O/\Delta t$	—	56	—	—	56	—	mV/1.0 k Hrs.
Ripple Rejection ($I_O = 40\text{ mA}$, $f = 120\text{ Hz}$, $29\text{ V} \leq V_I \leq 35\text{ V}$, $T_J = +25^\circ\text{C}$)	RR	30	43	—	31	45	—	dB
Input-Output Voltage Differential ($T_J = +25^\circ\text{C}$)	V_I/V_O	—	1.7	—	—	1.7	—	Vdc

TYPICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

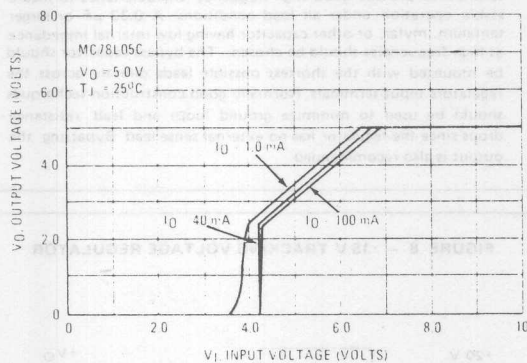


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

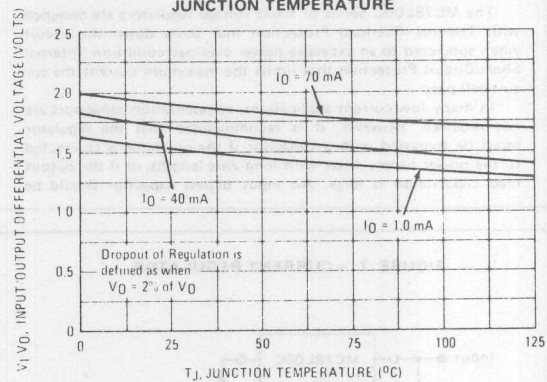


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

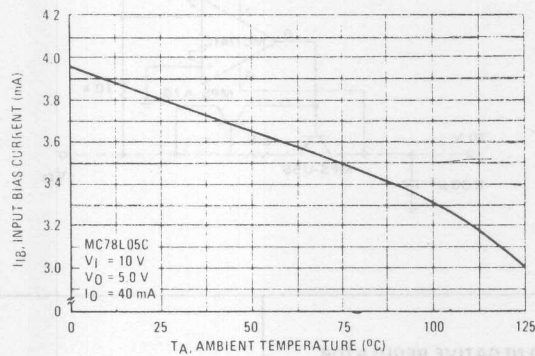


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

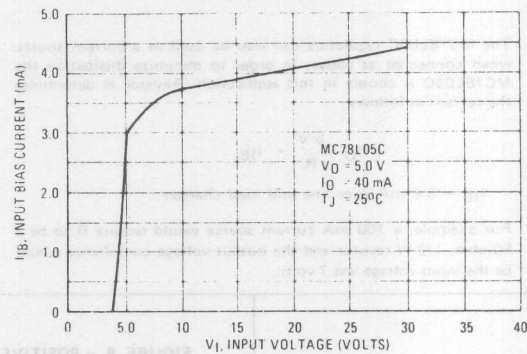


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

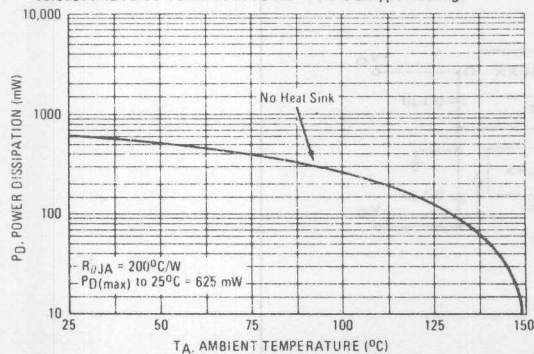
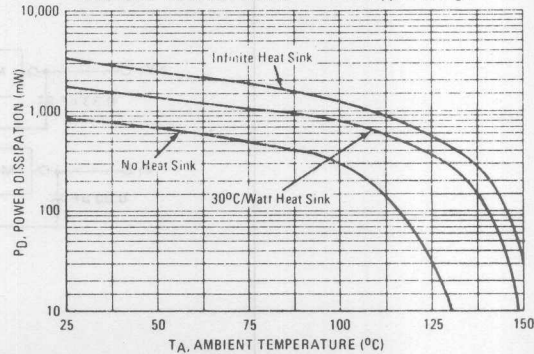


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



APPLICATIONS INFORMATION

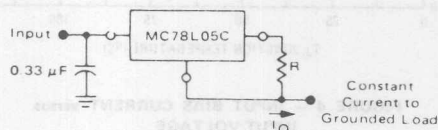
Design Considerations

The MC78L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be

selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A $0.33 \mu\text{F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 - CURRENT REGULATOR



The MC78L00C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows

$$I_O = \frac{5 \text{ V}}{R} + I_{IB}$$

$$I_{IB} = 3.8 \text{ mA over line and load changes}$$

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts.

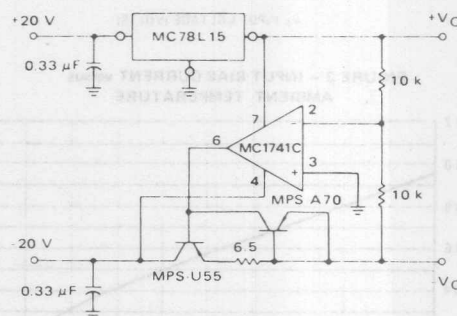
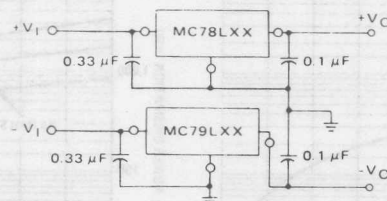
FIGURE 8 - $\pm 15 \text{ V}$ TRACKING VOLTAGE REGULATOR

FIGURE 9 - POSITIVE AND NEGATIVE REGULATOR



MC78M00C series

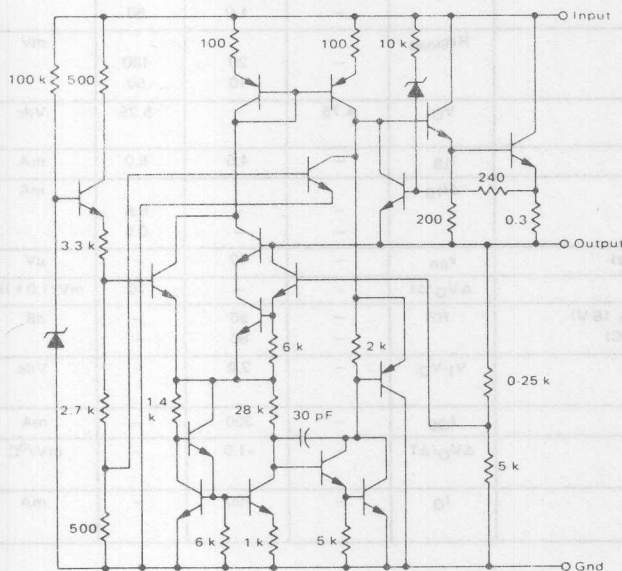
MC78M00C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78M00 Series positive voltage regulators are identical to the popular MC7800C Series devices, except that they are specified for only one-third the output current. Like the MC7800C devices, the MC78M00C three-terminal regulators are intended for local, on-card voltage regulation.

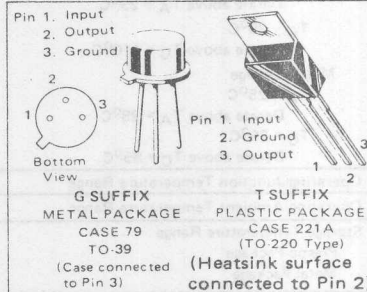
Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 79 (TO-220 and Hermetic TO-39)

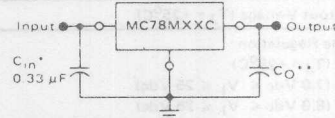
REPRESENTATIVE
SCHEMATIC DIAGRAM



THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC78MXXCG	$T_J: 0^\circ\text{C to } +150^\circ\text{C}$	Metal Can
MC78MXXCT	$T_J: 0^\circ\text{C to } +150^\circ\text{C}$	Plastic Power

XX indicates nominal voltage

TYPE NO./VOLTAGE

MC78M05C	5.0 Volts
MC78M06C	6.0 Volts
MC78M08C	8.0 Volts
MC78M12C	12 Volts
MC78M15C	15 Volts
MC78M18C	18 Volts
MC78M20C	20 Volts
MC78M24C	24 Volts

MC78M00C Series

MC78M00C Series MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (20 V - 24 V)	V_I	35 40	Vdc
Power Dissipation (Package Limitation)			
Plastic Package			
$T_A = 25^{\circ}\text{C}$	P_D	Internally Limited	$^{\circ}\text{C}/\text{W}$
Derate above $T_A = 25^{\circ}\text{C}$	θ_{JA}	70	$^{\circ}\text{C}/\text{W}$
$T_C = 25^{\circ}\text{C}$	P_D	Internally Limited	$^{\circ}\text{C}/\text{W}$
Derate above $T_C = 110^{\circ}\text{C}$	θ_{JC}	5.0	$^{\circ}\text{C}/\text{W}$
Metal Package			
$T_A = 25^{\circ}\text{C}$	P_D	Internally Limited	$^{\circ}\text{C}/\text{W}$
Derate above $T_A = 25^{\circ}\text{C}$	θ_{JA}	185	$^{\circ}\text{C}/\text{W}$
$T_C = 25^{\circ}\text{C}$	P_D	Internally Limited	$^{\circ}\text{C}/\text{W}$
Derate above $T_C = 85^{\circ}\text{C}$	θ_{JC}	25	$^{\circ}\text{C}/\text{W}$
Operating Junction Temperature Range	T_J	0 to +150	$^{\circ}\text{C}$
Operating Ambient Temperature Range	T_A	0 to +85	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}		
Plastic Package		-65 to +150	$^{\circ}\text{C}$
Metal Package		-65 to +150	$^{\circ}\text{C}$

MC78M05C ELECTRICAL CHARACTERISTICS ($V_I = 10\text{ V}$, $I_O = 200\text{ mA}$, $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^{\circ}\text{C}$)	V_O	4.8	5.0	5.2	Vdc
Line Regulation ($T_J = +25^{\circ}\text{C}$) (7.0 Vdc $\leq V_I \leq 25\text{ Vdc}$) (8.0 Vdc $\leq V_I \leq 25\text{ Vdc}$)	Reg_{line}	— —	3.0 1.0	100 50	mV
Load Regulation ($T_J = +25^{\circ}\text{C}$, 5.0 mA $\leq I_O \leq 500\text{ mA}$) ($T_J = +25^{\circ}\text{C}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	Reg_{load}	— —	20 10	100 50	mV
Output Voltage (7.0 Vdc $\leq V_I \leq 25\text{ Vdc}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	V_O	4.75	—	5.25	Vdc
Input Bias Current ($T_J = +25^{\circ}\text{C}$)	I_{IB}	—	4.5	6.0	mA
Quiescent Current Change (8.0 Vdc $\leq V_I \leq 25\text{ Vdc}$) (5.0 mA $\leq I_O \leq 200\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^{\circ}\text{C}$, 10 Hz $\leq f \leq 100\text{ kHz}$)	e_{on}	—	40	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	20	mV/1.0 k Hrs
Ripple Rejection ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, 8.0 V $\leq V_I \leq 18\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, 8.0 $\leq V_I \leq 18\text{ V}$, $T_J = 25^{\circ}\text{C}$)	RR	— —	80 80	— —	dB
Input-Output Voltage Differential ($T_A = +25^{\circ}\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short-Circuit Current Limit ($T_J = +25^{\circ}\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	300	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^{\circ}\text{C}$
Peak Output Current ($T_J = 25^{\circ}\text{C}$)	I_O	—	700	—	mA

MC78M06C ELECTRICAL CHARACTERISTICS ($V_I = 11\text{ V}$, $I_O = 200\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	5.75	6.0	6.25	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$) ($8.0\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$) ($9.0\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$)	Reg_{line}	— —	5.0 1.5	100 50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Reg_{load}	— —	20 10	120 60	mV
Output Voltage ($8.0\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	V_O	5.7	—	6.3	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.5	6.0	mA
Quiescent Current Change ($9.0\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$) ($5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	45	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	24	mV/1.0 k Hrs
Ripple Rejection ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $9.0\text{ V} \leq V_I \leq 19\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $9.0\text{ V} \leq V_I \leq 19\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	— —	80 80	— —	dB
Input-Output Voltage Differential ($T_A = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	270	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$) ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M08C ELECTRICAL CHARACTERISTICS ($V_I = 14\text{ V}$, $I_O = 200\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	7.7	8.0	8.3	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$) ($10.5\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$) ($11\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$)	Reg_{line}	— —	6.0 2.0	100 50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Reg_{load}	— —	25 10	160 80	mV
Output Voltage ($10.5\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	V_O	7.6	—	8.4	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.6	6.0	mA
Quiescent Current Change ($10.5\text{ Vdc} \leq V_I \leq 25\text{ Vdc}$) ($5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	52	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	32	mV/1.0 k Hrs
Ripple Rejection ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $11.5\text{ V} \leq V_I \leq 21.5\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $11.5\text{ V} \leq V_I \leq 21.5\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	— —	80 80	— —	dB
Input-Output Voltage Differential ($T_A = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	250	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$)	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M00C Series

MC78M12C ELECTRICAL CHARACTERISTICS ($V_I = 19\text{ V}$, $I_O = 200\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	11.5	12	12.5	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$) (14.5 Vdc $\leq V_I \leq 30\text{ Vdc}$) (16 Vdc $\leq V_I \leq 22\text{ Vdc}$)	Reg_{line}	—	8.0 2.0	100 50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, 5.0 mA $\leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	Reg_{load}	—	25 10	240 120	mV
Output Voltage (14.5 Vdc $\leq V_I \leq 27\text{ Vdc}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	V_O	11.4	—	12.6	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.8	6.0	mA
Quiescent Current Change (14.5 Vdc $\leq V_I \leq 30\text{ Vdc}$) (5.0 mA $\leq I_O \leq 200\text{ mA}$)	ΔI_{IB}	—	—	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq 100\text{ kHz}$)	e_{on}	—	75	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	48	mV/1.0 k Hrs
Ripple Rejection ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, 15 V $\leq V_I \leq 25\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, 15 V $\leq V_I \leq 25\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	—	80 80	—	dB
Input-Output Voltage Differential ($T_A = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$, $0^\circ\text{C} < T_A \leq +125^\circ\text{C}$)	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M15C ELECTRICAL CHARACTERISTICS ($V_I = 23\text{ V}$, $I_O = 200\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	14.4	15	15.6	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) (17.5 Vdc $\leq V_I \leq 30\text{ Vdc}$) (20 Vdc $\leq V_I \leq 30\text{ Vdc}$)	Reg_{line}	—	10 3.0	100 50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, 5.0 mA $\leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	Reg_{load}	—	25 10	300 150	mV
Output Voltage (17.5 Vdc $\leq V_I \leq 30\text{ Vdc}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	V_O	14.25	—	15.75	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.8	6.0	mA
Quiescent Current Change (18.5 Vdc $\leq V_I \leq 30\text{ Vdc}$) (5.0 mA $\leq I_O \leq 200\text{ mA}$)	ΔI_{IB}	—	—	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq 100\text{ kHz}$)	e_{on}	—	90	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	60	mV/1.0 k Hrs
Ripple Rejection ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, 18.5 V $\leq V_I \leq 28.5\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, 18.5 V $\leq V_I \leq 28.5\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	—	70 70	—	dB
Input-Output Voltage Differential ($T_A = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$, $0^\circ\text{C} < T_A \leq +125^\circ\text{C}$)	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M00C Series

MC78M18C ELECTRICAL CHARACTERISTICS ($V_I = 27\text{ V}$, $I_O = 200\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	17.3	18	18.7	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$) (21 Vdc $\leq V_I \leq 33\text{ Vdc}$) (24 Vdc $\leq V_I \leq 33\text{ Vdc}$)	Reg_{line}	—	10 40	100 50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, 5.0 mA $\leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	Reg_{load}	—	30 10	360 180	mV
Output Voltage (21 Vdc $\leq V_I \leq 33\text{ Vdc}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	V_O	17.1	—	18.9	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.8	6.5	mA
Quiescent Current Change (21 Vdc $\leq V_I \leq 33\text{ Vdc}$) (5.0 mA $\leq I_O \leq 200\text{ mA}$)	ΔI_{IB}	—	—	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq 100\text{ kHz}$)	e_{on}	—	100	—	μV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	72	mV/1.0 k Hrs
Ripple Rejection ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, 22 V $\leq V_I \leq 32\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, 22 V $\leq V_I \leq 32\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	—	70 70	—	dB
Input-Output Voltage Differential ($T_A = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$)	$\Delta V_O/\Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M20C ELECTRICAL CHARACTERISTICS ($V_I = 29\text{ V}$, $I_O = 200\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	19.2	20	20.8	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$) (23 Vdc $\leq V_I \leq 35\text{ Vdc}$) (24 Vdc $\leq V_I \leq 35\text{ Vdc}$)	Reg_{line}	—	10 5.0	100 50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, 5.0 mA $\leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	Reg_{load}	—	30 10	400 200	mV
Output Voltage (23 Vdc $\leq V_I \leq 35\text{ Vdc}$, 5.0 mA $\leq I_O \leq 200\text{ mA}$)	V_O	19	—	21	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.9	6.5	mA
Quiescent Current Change (23 Vdc $\leq V_I \leq 35\text{ Vdc}$) (5.0 mA $\leq I_O \leq 200\text{ mA}$)	ΔI_{IB}	—	—	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq 100\text{ kHz}$)	e_{on}	—	110	—	μV
Long-Term Stability	$\Delta V_O/\Delta t$	—	—	80	mV/1.0 k Hrs
Ripple Rejection ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, 24 V $\leq V_I \leq 34\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, 24 V $\leq V_I \leq 34\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	—	70 70	—	dB
Input-Output Voltage Differential ($T_A = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$, $V_I = 35\text{ V}$)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$)	$\Delta V_O/\Delta T$	—	-1.1	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

MC78M24C ELECTRICAL CHARACTERISTICS ($V_I = 33\text{ V}$, $I_O = 200\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $P_D \leq 5.0\text{ W}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	23	24	25	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$) ($27\text{ Vdc} \leq V_I \leq 38\text{ Vdc}$) ($28\text{ Vdc} \leq V_I \leq 38\text{ Vdc}$)	Regline	— —	10 5.0	100 50	mV
Load Regulation ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 500\text{ mA}$) ($T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	Regload	— —	30 10	480 240	mV
Output Voltage ($27\text{ Vdc} \leq V_I \leq 38\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	V_O	22.8	—	25.2	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	5.0	7.0	mA
Quiescent Current Change ($27\text{ Vdc} \leq V_I \leq 38\text{ Vdc}$) ($5.0\text{ mA} \leq I_O \leq 200\text{ mA}$)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	170	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	96	mV/1.0 kHrs
Ripple Rejection ($I_O = 100\text{ mA}$, $f = 120\text{ Hz}$, $28\text{ V} \leq V_I \leq 38\text{ V}$) ($I_O = 300\text{ mA}$, $f = 120\text{ Hz}$, $28\text{ V} \leq V_I \leq 38\text{ V}$, $T_J = 25^\circ\text{C}$)	RR	— —	70 70	— —	dB
Input-Output Voltage Differential ($T_A = +25^\circ\text{C}$)	$V_I - V_O$	—	2.0	—	Vdc
Short-Circuit Current Limit ($T_J = +25^\circ\text{C}$)	I_{OS}	—	240	—	mA
Average Temperature Coefficient of Output Voltage ($I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$)	$\Delta V_O / \Delta T$	—	-1.2	—	mV/ $^\circ\text{C}$
Peak Output Current ($T_J = 25^\circ\text{C}$)	I_O	—	700	—	mA

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

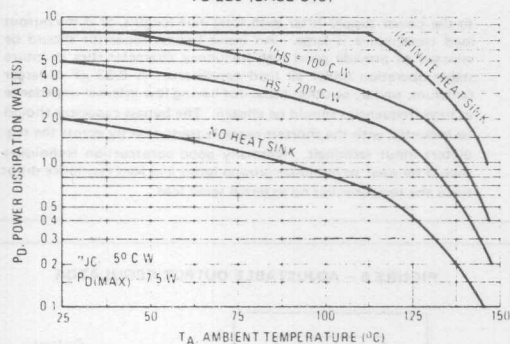
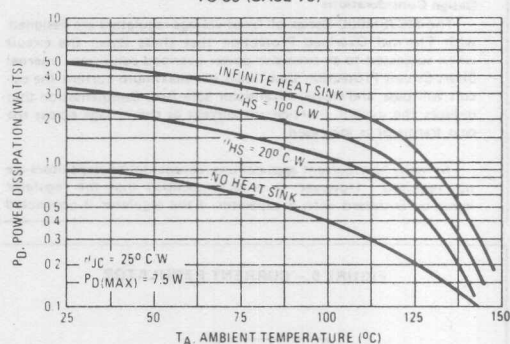
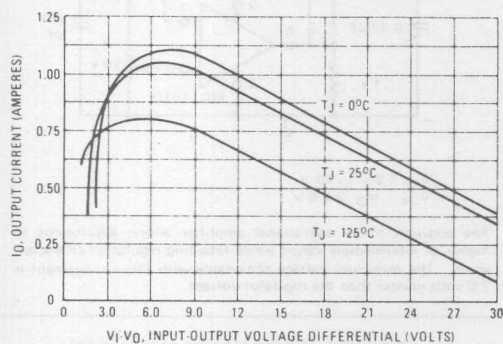
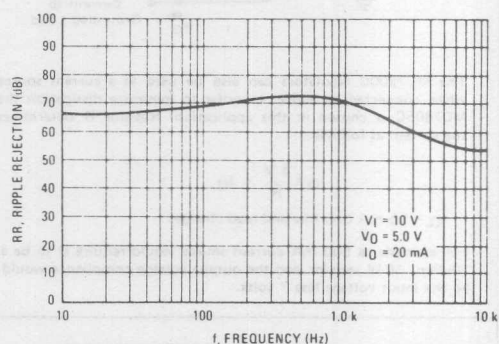
Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – WORST CASE POWER DISSIPATION
versus AMBIENT TEMPERATURE
TO-220 (CASE 313)FIGURE 2 – WORST CASE POWER DISSIPATION
versus AMBIENT TEMPERATURE
TO-39 (CASE 79)FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF
INPUT-OUTPUT DIFFERENTIAL VOLTAGEFIGURE 4 – RIPPLE REJECTION AS A FUNCTION
OF FREQUENCY

APPLICATIONS INFORMATION

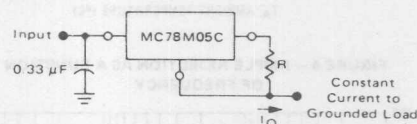
Design Considerations

The MC78M00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected

to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 5 – CURRENT REGULATOR



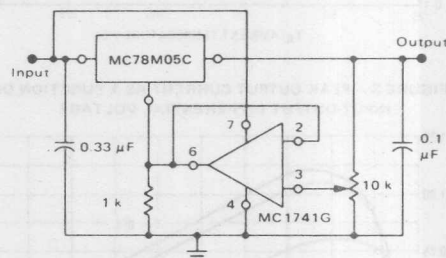
The MC7800C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5 \text{ V}}{R} + I_Q$$

$$I_Q = 1.5 \text{ mA over line and load changes}$$

For example, a 500 mA current source would require R to be a 10-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 6 – ADJUSTABLE OUTPUT REGULATOR

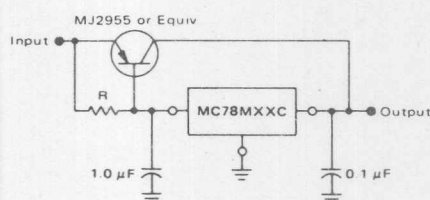


$$V_O: 7.0 \text{ V to } 20 \text{ V}$$

$$V_{IN} \quad V_O \geq 2.0 \text{ V}$$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

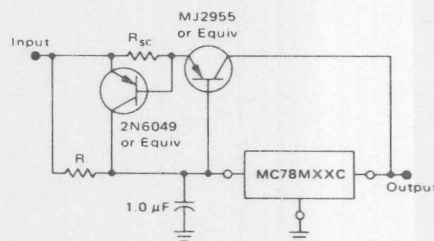
FIGURE 7 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78M00C series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 8 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{sc} , and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified.

MC7900C Series

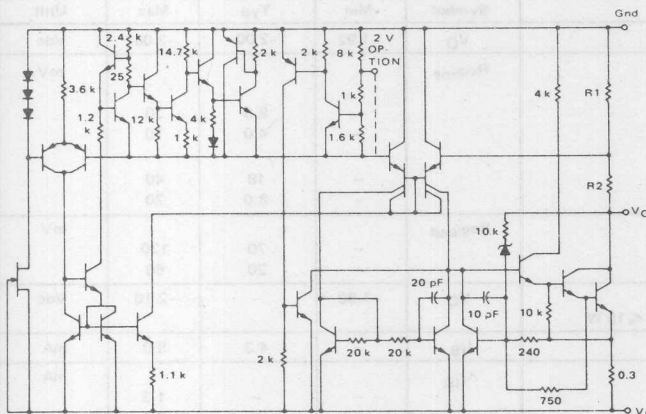
MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 1 (TO-220 and Hermetic TO-3)

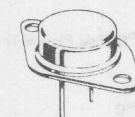
SCHEMATIC DIAGRAM



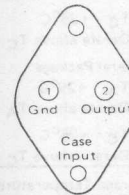
DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C - 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS



K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 TYPE)



(bottom view)

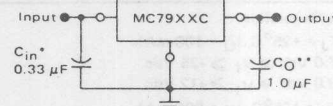
T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Ground
2. Input
3. Output

(Heatsink surface
connected to Pin2)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC79XXCK	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Metal Power
MC79XXCT	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Plastic Power

XX indicates nominal voltage

MC7900C Series

MC7900C Series MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.0 V – 18 V) (24 V)	V_I	-35 -40	Vdc
Power Dissipation Plastic Package $T_A = +25^{\circ}\text{C}$ Derate above $T_A = +25^{\circ}\text{C}$ $T_C = +25^{\circ}\text{C}$ Derate above $T_C = +95^{\circ}\text{C}$ (See Figure 1)	P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$	Internally Limited 15.4 Internally Limited 200	Watts $\text{mW}/^{\circ}\text{C}$ Watts $\text{mW}/^{\circ}\text{C}$
Metal Package $T_A = +25^{\circ}\text{C}$ Derate above $T_A = +25^{\circ}\text{C}$ $T_C = +25^{\circ}\text{C}$ Derate above $T_C = +65^{\circ}\text{C}$	P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$	Internally Limited 22.2 Internally Limited 182	Watts $\text{mW}/^{\circ}\text{C}$ Watts $\text{mW}/^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Junction Temperature Range	T_J	0 to +150	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient – Plastic Package	$R_{\theta JA}$	65	$^{\circ}\text{C}/\text{W}$
– Metal Package		45	
Thermal Resistance, Junction to Case – Plastic Package	$R_{\theta JC}$	5.0	$^{\circ}\text{C}/\text{W}$
– Metal Package		5.5	

MC7902C ELECTRICAL CHARACTERISTICS ($V_I = -10\text{ V}$, $I_O = 500\text{ mA}$, $0^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^{\circ}\text{C}$)	V_O	-1.92	-2.00	-2.08	Vdc
Line Regulation ($T_J = +25^{\circ}\text{C}$, $I_O = 100\text{ mA}$) -7.0 Vdc $\geq V_I \geq -25\text{ Vdc}$ -8.0 Vdc $\geq V_I \geq -12\text{ Vdc}$ ($T_J = +25^{\circ}\text{C}$, $I_O = 500\text{ mA}$) -7.0 Vdc $\geq V_I \geq -25\text{ Vdc}$ -8.0 Vdc $\geq V_I \geq -12\text{ Vdc}$	Reg _{line}	– – – –	8.0 4.0 18 8.0	20 10 40 20	mV
Load Regulation $T_J = +25^{\circ}\text{C}$, $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg _{load}	– –	70 20	120 60	mV
Output Voltage -7.0 Vdc $\geq V_I \geq -20\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-1.90	–	-2.10	Vdc
Input Bias Current ($T_J = +25^{\circ}\text{C}$)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change -7.0 Vdc $\geq V_I \geq -25\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	– –	– –	1.3 0.5	mA
Output Noise Voltage ($T_A = +25^{\circ}\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	–	65	–	dB
Input-Output Voltage Differential $I_O = 1.0\text{ A}$, $T_J = +25^{\circ}\text{C}$	$ V_I - V_O $	–	3.5	–	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	$\Delta V_O/\Delta T$	–	-1.0	–	mV/ $^{\circ}\text{C}$

MC7900C Series

MC7905C ELECTRICAL CHARACTERISTICS ($V_I = -10\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-4.8	-5.0	-5.2	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) $-7.0\text{ Vdc} \geq V_I \geq -25\text{ Vdc}$ $-8.0\text{ Vdc} \geq V_I \geq -12\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) $-7.0\text{ Vdc} \geq V_I \geq -25\text{ Vdc}$ $-8.0\text{ Vdc} \geq V_I \geq -12\text{ Vdc}$	Reg_{line}	—	7.0 2.0	50 25	mV
Load Regulation $T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	—	11 4.0	100 50	mV
Output Voltage $-7.0\text{ Vdc} \geq V_I \geq -20\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-4.75	—	-5.25	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change $-7.0\text{ Vdc} \geq V_{I\text{in}} \geq -25\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	—	—	1.3 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	40	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	20	mV/1.0 k Hrs
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	70	—	dB
Input-Output Voltage Differential $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7905.2C ELECTRICAL CHARACTERISTICS ($V_I = -10\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-5.0	-5.2	-5.4	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) $-7.2\text{ Vdc} \geq V_I \geq -25\text{ Vdc}$ $-8.0\text{ Vdc} \geq V_I \geq -12\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) $-7.2\text{ Vdc} \geq V_I \geq -25\text{ Vdc}$ $-8.0\text{ Vdc} \geq V_I \geq -12\text{ Vdc}$	Reg_{line}	—	8.0 2.2	52 27	mV
Load Regulation $T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	—	12 4.5	105 52	mV
Output Voltage $-7.2\text{ Vdc} \geq V_I \geq -20\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-4.94	—	-5.46	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change $-7.2\text{ Vdc} \geq V_I \geq -25\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	—	—	1.3 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	42	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	20	mV/1.0 k Hrs
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	68	—	dB
Input-Output Voltage Differential $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7900C Series

MC7906C ELECTRICAL CHARACTERISTICS ($V_I = -11\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-5.75	-6.0	-6.25	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -8.0 Vdc $\geq V_I \geq -25\text{ Vdc}$ -9.0 Vdc $\geq V_I \geq -13\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -8.0 Vdc $\geq V_I \geq -25\text{ Vdc}$ -9.0 Vdc $\geq V_I \geq -13\text{ Vdc}$	Reg_{line}	— — — — —	9.0 3.0 43 10	60 30 120 60	mV
Load Regulation $T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	— —	13 5.0	120 60	mV
Output Voltage -8.0 Vdc $\geq V_I \geq -21\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-5.7	—	-6.3	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -8.0 Vdc $\geq V_I \geq -25\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	— —	— —	1.3 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	45	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	24	mV/1.0 k Hrs
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	65	—	dB
Input-Output Voltage Differential $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7908C ELECTRICAL CHARACTERISTICS ($V_I = -14\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-7.7	-8.0	-8.3	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -10.5 Vdc $\geq V_I \geq -25\text{ Vdc}$ -11 Vdc $\geq V_I \geq -17\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -10.5 Vdc $\geq V_I \geq -25\text{ Vdc}$ -11 Vdc $\geq V_I \geq -17\text{ Vdc}$	Reg_{line}	— — — — —	12 5.0 50 22	80 40 160 80	mV
Load Regulation $T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	— —	26 9.0	160 80	mV
Output Voltage -10.5 Vdc $\geq V_I \geq -23\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-7.6	—	-8.4	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -10.5 Vdc $\geq V_I \geq -25\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	— —	— —	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	52	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	32	mV/1.0 k Hrs
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	62	—	dB
Input-Output Voltage Differential $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7900C Series

MC7912C ELECTRICAL CHARACTERISTICS ($V_I = -19\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-11.5	-12	-12.5	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -14.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ -16 Vdc $\geq V_I \geq -22\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -14.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ -16 Vdc $\geq V_I \geq -22\text{ Vdc}$	Reg_{line}	— — —	13 6.0 55 24	120 60 240 120	mV
Load Regulation $T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	— —	46 17	240 120	mV
Output Voltage -14.5 Vdc $\geq V_I \geq -27\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-11.4	—	-12.6	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -14.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	— —	— —	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	75	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	48	mV/1.0 k Hrs
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	61	—	dB
Input-Output Voltage Differential $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7915C ELECTRICAL CHARACTERISTICS ($V_I = -23\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -17.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ -20 Vdc $\geq V_I \geq -26\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -17.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ -20 Vdc $\geq V_I \geq -26\text{ Vdc}$	Reg_{line}	— — —	14 6.0 57 27	150 75 300 150	mV
Load Regulation $T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Reg_{load}	— —	68 25	300 150	mV
Output Voltage -17.5 Vdc $\geq V_I \geq -30\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-14.25	—	-15.75	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -17.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.5\text{ A}$	ΔI_{IB}	— —	— —	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	90	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	60	mV/1.0 k Hrs
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	60	—	dB
Input-Output Voltage Differential $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7900C Series

MC7918C ELECTRICAL CHARACTERISTICS ($V_I = -27\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-17.3	-18	-18.7	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -21 Vdc $\geq V_I \geq -33\text{ Vdc}$ -24 Vdc $\geq V_I \geq -30\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -21 Vdc $\geq V_I \geq -33\text{ Vdc}$ -24 Vdc $\geq V_I \geq -30\text{ Vdc}$	Regline	— — — — —	25 10 90 50	180 90 360 180	mV
Load Regulation $T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Regload	— —	110 55	360 180	mV
Output Voltage -21 Vdc $\geq V_I \geq -33\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-17.1	—	-18.9	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.5	8.0	mA
Input Bias Current Change -21 Vdc $\geq V_I \geq -33\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_{IB}	— —	— —	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	110	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	72	mV/1.0 k Hrs
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	59	—	dB
Input-Output Voltage Differential $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

MC7924C ELECTRICAL CHARACTERISTICS ($V_I = -33\text{ V}$, $I_O = 500\text{ mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-23	-24	-25	Vdc
Line Regulation ($T_J = +25^\circ\text{C}$, $I_O = 100\text{ mA}$) -27 Vdc $\geq V_I \geq -38\text{ Vdc}$ -30 Vdc $\geq V_I \geq -36\text{ Vdc}$ ($T_J = +25^\circ\text{C}$, $I_O = 500\text{ mA}$) -27 Vdc $\geq V_I \geq -38\text{ Vdc}$ -30 Vdc $\geq V_I \geq -36\text{ Vdc}$	Regline	— — — — —	31 14 118 70	240 120 480 240	mV
Load Regulation $T_J = +25^\circ\text{C}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$ $250\text{ mA} \leq I_O \leq 750\text{ mA}$	Regload	— —	150 85	480 240	mV
Output Voltage -27 Vdc $\geq V_I \geq -38\text{ Vdc}$, $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$, $P \leq 15\text{ W}$	V_O	-22.8	—	-25.2	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$)	I_{IB}	—	4.6	8.0	mA
Input Bias Current Change -27 Vdc $\geq V_I \geq -38\text{ Vdc}$ $5.0\text{ mA} \leq I_O \leq 1.0\text{ A}$	ΔI_{IB}	— —	— —	1.0 0.5	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	e_{on}	—	170	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	—	96	mV/1.0 k Hrs
Ripple Rejection ($I_O = 20\text{ mA}$, $f = 120\text{ Hz}$)	RR	—	56	—	dB
Input-Output Voltage Differential $I_O = 1.0\text{ A}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage $I_O = 5.0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	$\Delta V_O / \Delta T$	—	-1.0	—	mV/ $^\circ\text{C}$

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220)

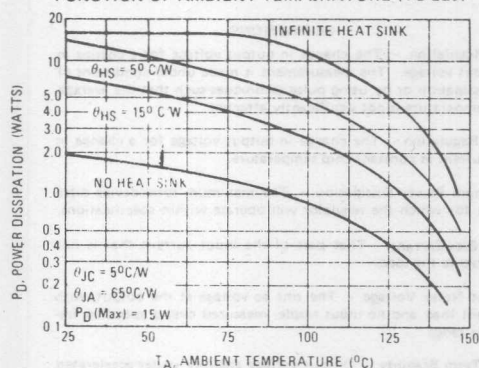


FIGURE 2 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3)

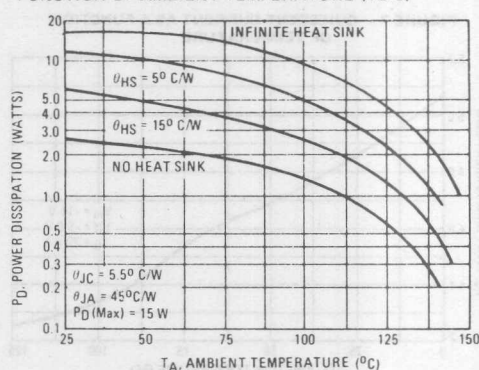


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

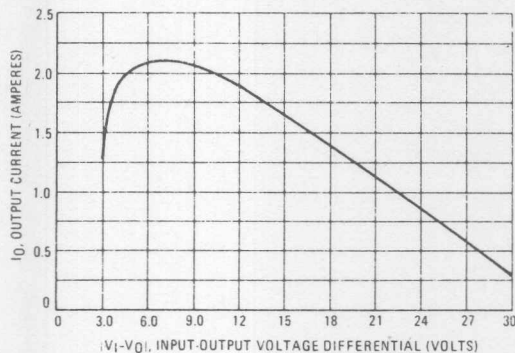


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

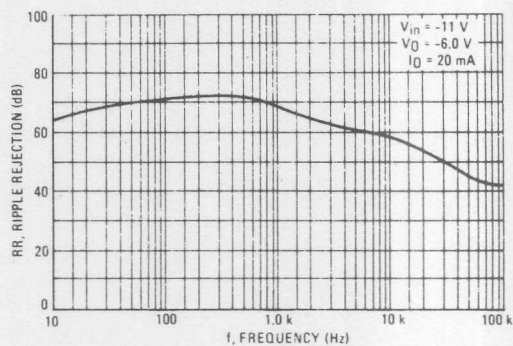


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

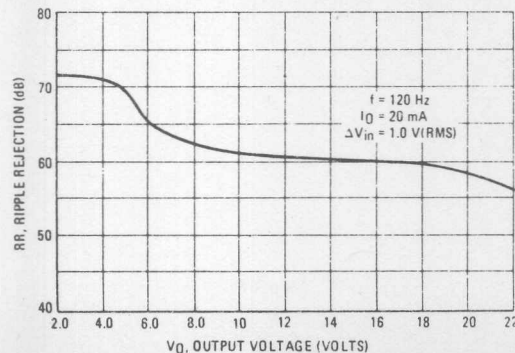
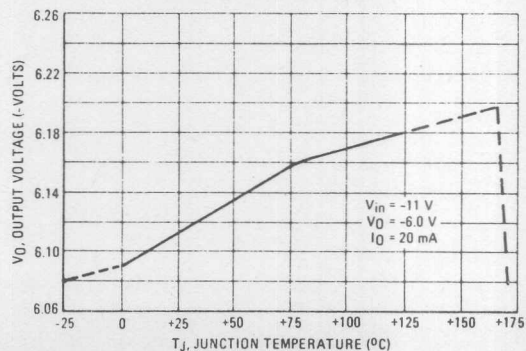
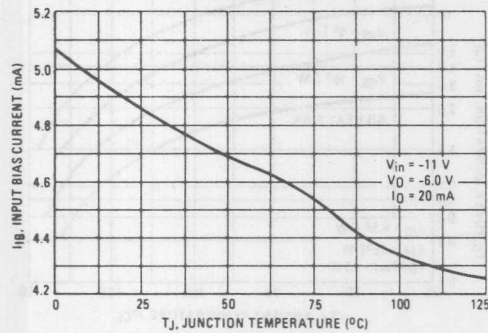


FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation -- The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation -- The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation -- The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current -- That part of the input current that is not delivered to the load.

Output Noise Voltage -- The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability -- Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC7900C Series

APPLICATIONS INFORMATION

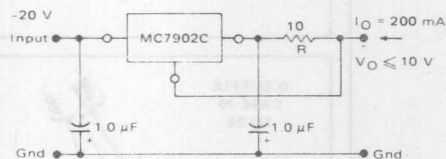
Design Considerations

The MC7900C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected

to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A $0.33 \mu\text{F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 – CURRENT REGULATOR

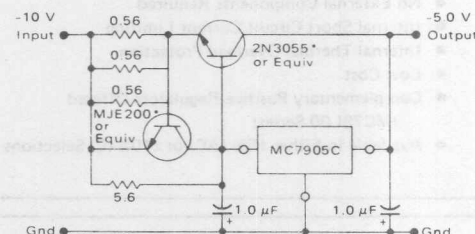


The MC7902, -2.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{2 \text{ V}}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 2.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

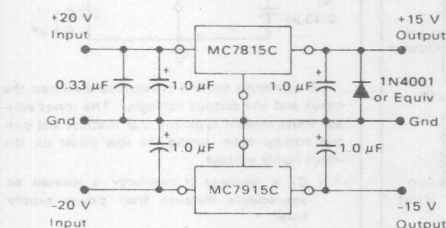
FIGURE 9 – CURRENT BOOST REGULATOR
(-5.0 V @ 4.0 A, with 5.0 A current limiting)



* Mounted on common heat sink, Motorola MS 10 or equivalent.

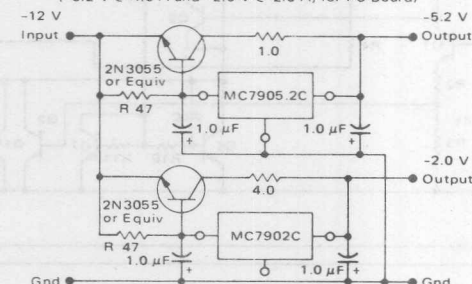
When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to $0.6 \text{ V}/R_{SC}$. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 – OPERATIONAL AMPLIFIER SUPPLY
(±15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems.

FIGURE 11 – TYPICAL MECL SYSTEM POWER SUPPLY
(-5.2 V @ 4.0 A and -2.0 V @ 2.0 A; for PC Board)



When current-boost power transistors are used, 47-ohm base-emitter resistors (R) must be used to bypass the quiescent current at no load. These resistors, in conjunction with the V_{BE} of the NPN transistors, determine when the pass transistors begin conducting. The 1-ohm and 4-ohm dropping resistors were chosen to reduce the power dissipated in the boost transistors but still leave at least 2.0 V across these devices for good regulation.

MC79L00C, AC series

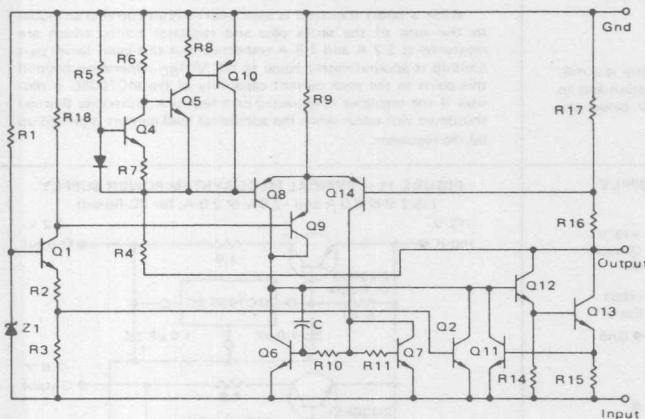
THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either $\pm 5\%$ (AC) or $\pm 10\%$ (C) Selections

REPRESENTATIVE CIRCUIT SCHEMATIC



Device No. -10%	Device No. ±5%	Nominal Voltage
MC79L03C	MC79L03AC	-3.0
MC79L05C	MC79L05AC	-5.0
MC79L12C	MC79L12AC	-12
MC79L15C	MC79L15AC	-15
MC79L18C	MC79L18AC	-18
MC79L24C	MC79L24AC	-24

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

P SUFFIX
CASE 29
TO-92

Pin 1. Ground
2. Input
3. Output



G SUFFIX
CASE 79
TO-39

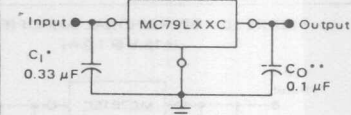
Pin 1. Ground
2. Output
3. Input

(Case connected
to pin 3)

Bottom View



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_1 is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

Device	Temperature Range	Package
MC79LXXACG	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Metal Can
MC79LXXACP	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Plastic Power
MC79LXXCG	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Metal Can
MC79LXXCP	$T_J = 0^\circ\text{C to } +150^\circ\text{C}$	Plastic Power

XX indicates nominal voltage

MC79L00C, AC Series

MC79L00C Series MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (-3, -5 V) (-12, -15, -18 V) (-24 V)	V_I	-30 -35 -40	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Junction Temperature Range	T_J	0 to +150	$^\circ\text{C}$

MC79L03C, AC ELECTRICAL CHARACTERISTICS ($V_I = -10\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC79L03C			MC79L03AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-2.76	-3.00	-3.24	-2.88	-3.0	-3.12	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$)	Regline	—	—	80	—	—	60	mV
-7.0 Vdc $\geq V_I \geq -20\text{ Vdc}$ -8.0 Vdc $\geq V_I \geq -20\text{ Vdc}$		—	—	60	—	—	40	
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Regload	—	—	72 36	—	—	72 36	mV
Output Voltage -7.0 Vdc $\geq V_I \geq -20\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -10\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	-2.7 -2.7	—	-3.3 -3.3	-2.85 -2.85	—	-3.15 -3.15	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	—	6.0 5.5	—	—	6.0 5.5	mA
Input Bias Current Change -8.0 Vdc $\geq V_I \geq -20\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	ΔI_{IB}	—	—	-1.5 -0.2	—	—	-1.5 -0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_N	—	30	—	—	30	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	10	—	—	10	—	mV/1.0 k Hrs.
Ripple Rejection (-8.0 $\geq V_I \geq -18\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = 25^\circ\text{C}$)	RR	44	51	—	45	51	—	dB
Input-Output Voltage Differential $I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	1.7	—	—	1.7	—	Vdc

MC79L00C, AC Series

MC79L00C, AC Series

MC79L05C, AC Series ELECTRICAL CHARACTERISTICS ($V_I = -10\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC79L05C			MC79L05AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-4.6	-5.0	-5.4	-4.8	-5.0	-5.2	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$)	Reg _{line}							mV
-7.0 Vdc $\geq V_I \geq -20\text{ Vdc}$		—	—	200	—	—	150	
-8.0 Vdc $\geq V_I \geq -20\text{ Vdc}$		—	—	150	—	—	100	
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Reg _{load}	—	—	60 30	—	—	60 30	mV
Output Voltage -7.0 Vdc $\geq V_I \geq -20\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -10\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	-4.5 -4.5	—	-5.5 -5.5	-4.75 -4.75	—	-5.25 -5.25	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	— —	— —	6.0 5.5	— —	— —	6.0 5.5	mA
Input Bias Current Change -8.0 Vdc $\geq V_I \geq -20\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	ΔI_{IB}	— —	— —	1.5 0.2	— —	— —	1.5 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_N	—	40	—	—	40	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	12	—	—	12	—	mV/1.0 k Hrs.
Ripple Rejection (-8.0 $\geq V_I \geq 18\text{ Vdc}$, $f = 120\text{ kHz}$, $T_J = 25^\circ\text{C}$)	RR	40	49	—	41	49	—	dB
Input-Output Voltage Differential $I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	1.7	—	—	1.7	—	Vdc

MC79L12C, AC ELECTRICAL CHARACTERISTICS ($V_I = -19\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC79L12C			MC79L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-11.1	-12	-12.9	-11.5	-12	-12.5	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$)	Reg _{line}							mV
-14.5 Vdc $\geq V_I \geq -27\text{ Vdc}$		—	—	250	—	—	250	
-16 Vdc $\geq V_I \geq -27\text{ Vdc}$		—	—	200	—	—	200	
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Reg _{load}	—	—	100 50	—	—	100 50	mV
Output Voltage -14.5 Vdc $\geq V_I \geq -27\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -19\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	-10.8 -10.8	—	-13.2 -13.2	-11.4 -11.4	—	-12.6 -12.6	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	— —	— —	6.5 6.0	— —	— —	6.5 6.0	mA
Input Bias Current Change -16 Vdc $\geq V_I \geq -27\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	ΔI_{IB}	— —	— —	1.5 0.2	— —	— —	1.5 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_N	—	80	—	—	80	—	μV
Long-Term Stability	$\Delta V_O / \Delta t$	—	24	—	—	24	—	mV/1.0 k Hrs.
Ripple Rejection (-15 $\leq V_I \leq -25\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$)	RR	36	42	—	37	42	—	dB
Input-Output Voltage Differential $I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	1.7	—	—	1.7	—	Vdc

MC79L00C, AC Series

MC79L15C, AC ELECTRICAL CHARACTERISTICS ($V_I = -23\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC79L15C			MC79L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-13.8	-15	-16.2	-14.4	-15	-15.6	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) $-17.5\text{ Vdc} \geq V_I > -30\text{ Vdc}$ $-20\text{ Vdc} \geq V_I > -30\text{ Vdc}$	Regline	—	—	300 250	—	—	300 250	mV
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Regload	—	—	150 75	—	—	150 75	mV
Output Voltage $-17.5\text{ Vdc} \geq V_I > -30\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -23\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	-13.5 -13.5	—	-16.5 -16.5	-14.25 -14.25	—	-15.75 -15.75	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	—	6.5 6.0	—	—	6.5 6.0	mA
Input Bias Current Change $-20\text{ Vdc} \geq V_I > -30\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	ΔI_{IB}	—	—	1.5 0.2	—	—	1.5 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_N	—	90	—	—	90	—	μV
Long-Term Stability $\Delta V_O/\Delta t$	$\Delta V_O/\Delta t$	—	30	—	—	30	—	mV/1.0 k Hrs.
Ripple Rejection ($-18.5 \leq V_I \leq -28.5\text{ Vdc}$, $f = 120\text{ Hz}$)	RR	33	39	—	34	39	—	dB
Input-Output Voltage Differential $I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	1.7	—	—	1.7	—	Vdc

MC79L18C, AC ELECTRICAL CHARACTERISTICS ($V_I = -27\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-16.6	-18	-19.4	-17.3	-18	-18.7	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) $-20.7\text{ Vdc} \geq V_I > -33\text{ Vdc}$ $-21.4\text{ Vdc} \geq V_I > -33\text{ Vdc}$ $-22\text{ Vdc} \geq V_I > -33\text{ Vdc}$ $-21\text{ Vdc} \geq V_I > -33\text{ Vdc}$	Regline	—	—	— 325 275 —	—	—	325 — — 275	mV
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Regload	—	—	170 85	—	—	170 85	mV
Output Voltage $-20.7\text{ Vdc} \geq V_I > -33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $-21.4\text{ Vdc} \geq V_I > -33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -27\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	— -16.2 -16.2	—	— -19.8 -19.8	-17.1 — -17.1	—	-18.9 — -18.9	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	—	6.5 6.0	—	—	6.5 6.0	mA
Input Bias Current Change $-21\text{ Vdc} \geq V_I > -33\text{ Vdc}$ $-27\text{ Vdc} \geq V_I > -33\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	ΔI_{IB}	—	—	— 1.5 0.2	—	—	1.5 — 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_N	—	150	—	—	150	—	μV
Long-Term Stability $\Delta V_O/\Delta t$	$\Delta V_O/\Delta t$	—	45	—	—	45	—	mV/1.0 k Hrs.
Ripple Rejection ($-23 \leq V_I \leq -33\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$)	RR	32	46	—	33	48	—	dB
Input-Output Voltage Differential $I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	1.7	—	—	1.7	—	Vdc

MC79L00C, AC Series

MC79L24C, AC ELECTRICAL CHARACTERISTICS ($V_I = -33$ V, $I_O = 40$ mA, $C_I = 0.33$ μ F, $C_O = 0.1$ μ F, $0^\circ\text{C} < T_J < +125^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	MC79L24C			MC79L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-22.1	-24	-25.9	-23	-24	-25	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$)	Reg _{line}	—	—	—	—	—	—	mV
-27 Vdc $\geq V_I > -38$ V		—	—	—	—	—	350	
-27.5 Vdc $\geq V_I > -38$ Vdc		—	—	350	—	—	—	
-28 Vdc $\geq V_I > -38$ Vdc		—	—	300	—	—	300	
Load Regulation $T_J = +25^\circ\text{C}$, 1.0 mA $\leq I_O \leq 100$ mA 1.0 mA $\leq I_O \leq 40$ mA	Reg _{load}	—	—	200	—	—	200	mV
		—	—	100	—	—	100	
Output Voltage -27 Vdc $\geq V_I > -38$ V, 1.0 mA $\leq I_O \leq 40$ mA -28 Vdc $\geq V_I > -38$ Vdc, 1.0 mA $\leq I_O \leq 40$ mA $V_I = -33$ Vdc, 1.0 mA $\leq I_O \leq 70$ mA	V_O	—	—	—	-22.8	—	-25.2	Vdc
		-21.4	—	-26.4	—	—	—	
		-21.4	—	-26.4	-22.8	—	-25.2	
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	—	—	6.5	—	—	6.5	mA
		—	—	6.0	—	—	6.0	
Input Bias Current Change -28 Vdc $\geq V_I > -38$ Vdc 1.0 mA $\leq I_O \leq 40$ mA	ΔI_{IB}	—	—	1.5	—	—	1.5	mA
		—	—	0.2	—	—	0.1	
Output Noise Voltage ($T_A = +25^\circ\text{C}$, 10 Hz $\leq f \leq 100$ kHz)	V_N	—	200	—	—	200	—	μ V
Long-Term Stability	$\Delta V_O / \Delta t$	—	56	—	—	56	—	mV/1.0 k Hrs.
Ripple Rejection ($-29 \leq V_I \leq -35$ Vdc, $f = 120$ Hz, $T_J = 25^\circ\text{C}$)	RR	30	43	—	31	47	—	dB
Input-Output Voltage Differential $I_O = 40$ mA, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	—	1.7	—	—	1.7	—	Vdc

APPLICATIONS INFORMATION

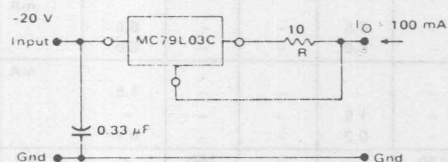
Design Considerations

The MC79L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be

selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μ F or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

CURRENT REGULATOR

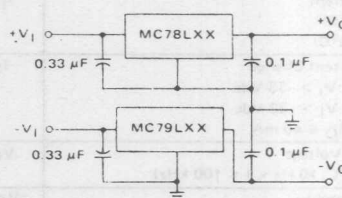


The MC79L03, -3.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{3 \text{ V}}{R} + I_B$$

The quiescent current for this regulator is typically 3.8 mA. The -3.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

POSITIVE AND NEGATIVE REGULATOR



MC79L00C, AC Series

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

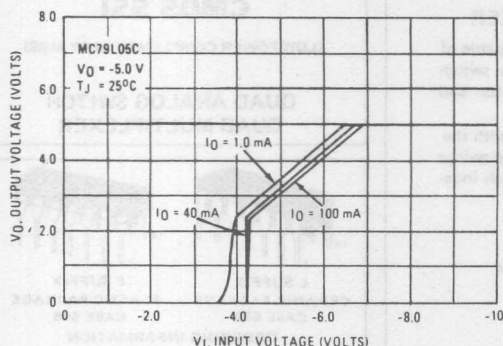


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

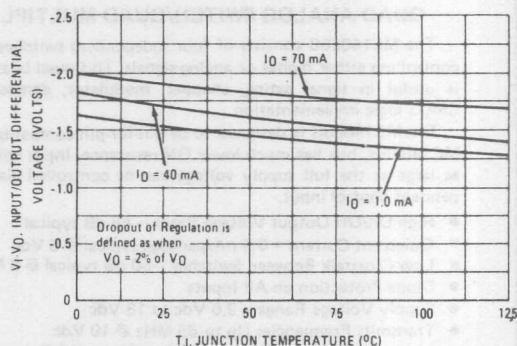


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

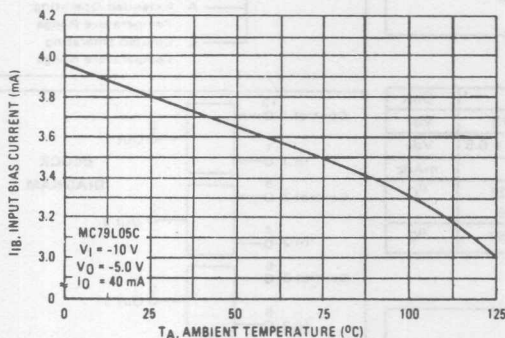


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

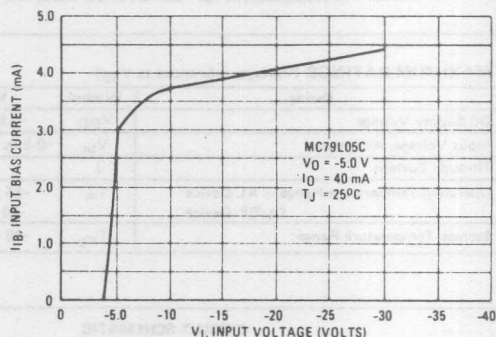


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

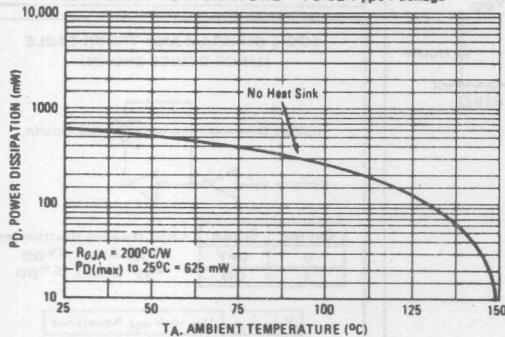
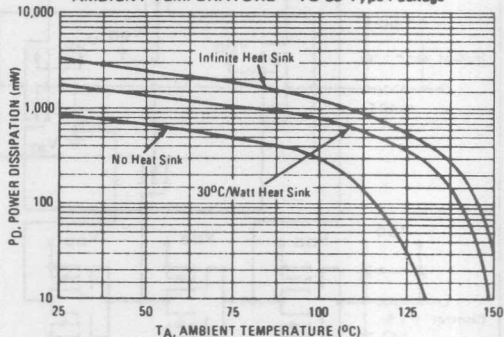


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



MC14066B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

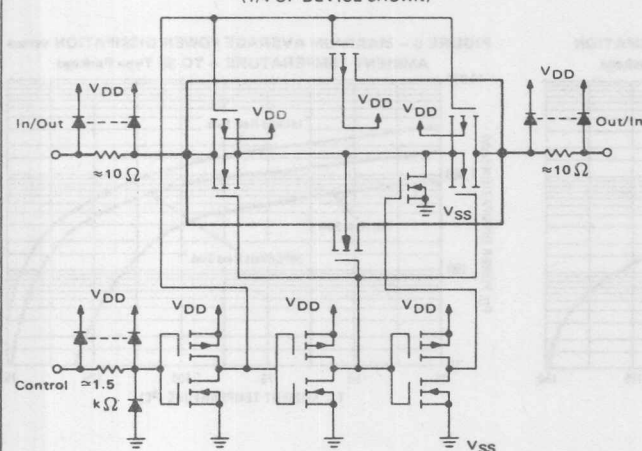
The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- High On/Off Output Voltage Ratio – 65 dB typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches –50 dB typical @ 8 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 65 MHz @ 10 Vdc
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60 \Omega$ for $V_{in} = V_{DD}$ to V_{SS} (at 15V)
- Low Noise – 12 nV/ $\sqrt{\text{Cycle}}$, $f \geq 1$ kHz typical
- Pin-for-Pin Replacement for CD4016, CD4066, MC14016

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
Through Current	I	25	mA
Operating Temperature Range – AL Device	T_A	-55 to +125	$^{\circ}\text{C}$
CL/CP Device		-40 to +85	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$

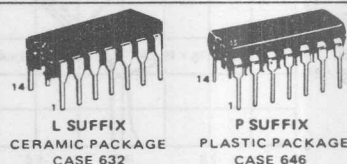
CIRCUIT SCHEMATIC (1/4 OF DEVICE SHOWN)



CMOS SSI

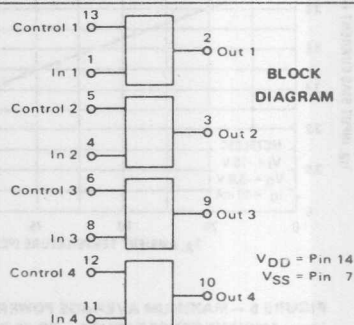
(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH QUAD MULTIPLEXER

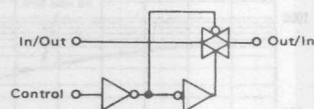


ORDERING INFORMATION

MC14XXX	Suffix	Denotes
L	Ceramic Package	
P	Plastic Package	
A	Extended Operating Temperature Range	
C	Limited Operating Temperature Range	



LOGIC DIAGRAM AND TRUTH TABLE (1/4 OF DEVICE SHOWN)



Control	Switch	Logic Diagram Restrictions
0	OFF	$V_{SS} \leq V_{in} \leq V_{DD}$
1	ON	$V_{SS} \leq V_{out} \leq V_{DD}$

$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$> 10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} Vdc	T _{low} *		25°C			T _{high} *		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Input Voltage (Control) "0" Level (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	3.75	—	6.75	3.75	—	3.75	
"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11.25	—	11.25	8.25	—	11.25	—	
Input Current (AL Device) Control	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Current (CL/CP Device) Control	I _{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μAdc
Input Capacitance (V _{in} = 0) Control Input Switch Inputs	C _{in}	—	—	—	—	—	—	—	—	pF
		10	—	—	—	5.0 8.0	7.5 15	—	—	
Output Capacitance	C _{out}	10	—	—	—	8.0	—	—	—	pF
Feedthrough Capacitance	C _{in-out}	10	—	—	—	0.5	—	—	—	pF
Quiescent Current (AL Device) (Per Package)	I _O	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.50	—	0.0010	0.50	—	15	
		15	—	1.00	—	0.0015	1.00	—	30	
Quiescent Current (CL/CP Device) (Per Package)	I _Q	5.0	—	1.0	—	0.0005	1.0	—	7.5	μAdc
		10	—	2.0	—	0.0010	2.0	—	15	
		15	—	4.0	—	0.0015	4.0	—	30	
ON Resistance (AL Device)	R _{ON}	5.0	—	800	—	250	1050	—	1200	Ω
		10	—	400	—	120	500	—	520	
		15	—	220	—	80	280	—	300	
ON Resistance (CL/CP Device)	R _{ON}	5.0	—	880	—	250	1050	—	1300	Ω
		10	—	450	—	120	500	—	550	
		15	—	250	—	80	280	—	320	
Δ ON Resistance Between Any Two of Four Switches	Δ R _{ON}	5.0	—	—	—	25	—	—	—	Ω
		10	—	—	—	10	—	—	—	
		15	—	—	—	5.0	—	—	—	
Input/Output Leakage Current Switch OFF (AL Device)	—	15	—	±100	—	±0.01	±100	—	±1000	nAdc
Input/Output Leakage Current Switch OFF (CL/CP Device)	—	15	—	±300	—	±0.01	±300	—	±1000	nAdc

*The formulas given are for the typical characteristics only.

T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < (V_{in} or V_{out}) < V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Times $V_{SS} = 0 \text{ Vdc}$						
Input to Output ($R_L = 10 \text{ k}\Omega$) $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 15.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 6.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 4.0 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	20 10 7.0	40 20 15	ns
Control to Output ($R_L = 1 \text{ k}\Omega$) Output "1" to High Impedance	t_{PHZ}	5.0 10 15	— — —	40 35 30	80 70 60	ns
Output "0" to High Impedance	t_{PLZ}	5.0 10 15	— — —	40 35 30	80 70 60	ns
High Impedance to Output "1"	t_{PZH}	5.0 10 15	— — —	60 20 15	120 40 30	ns
High Impedance to Output "0"	t_{PZL}	5.0 10 15	— — —	60 20 15	120 40 30	ns
Sine Wave Distortion ($V_{in} = 1.77 \text{ Vdc}$, RMS Centered @ 0.0 Vdc , $R_L = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	—	5.0	—	0.1	—	%
Frequency Response (Switch ON) ($R_L = 1 \text{ k}\Omega$, $20 \text{ Log}_{10} \frac{V_{out}}{V_{in}} = -3 \text{ dB}$)	—	5.0	—	65	—	MHz
Feedthrough Attenuation (Switch OFF) ($R_L = 1 \text{ k}\Omega$, $20 \text{ Log}_{10} \frac{V_{out}}{V_{in}} = -50 \text{ dB}$)	—	5.0	—	1.0	—	MHz
Crosstalk Between Any Two Switches ($R_L = 1 \text{ k}\Omega$, $20 \text{ Log}_{10} \frac{V_{out(B)}}{V_{in(A)}} = -50 \text{ dB}$, (Switch A ON, Switch B OFF)	—	5.0	—	8.0	—	MHz
Crosstalk, Control Input to Signal Output	—	5.0	—	300	—	mV
Maximum Control Input Frequency ($20 \text{ Log}_{10} \frac{V_{out}}{V_{in}} = -6 \text{ dB}$)	—	5.0 10 15	— — —	6.0 8.0 8.5	— — —	MHz

*The formulas given are for the typical characteristics only.

TEST CIRCUITS

FIGURE 1 - INPUT VOLTAGE

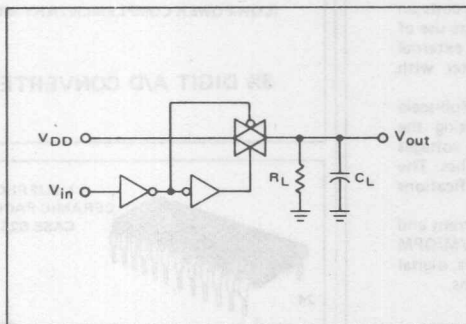


FIGURE 2 - PROPAGATION DELAY TIME, CONTROL TO OUTPUT

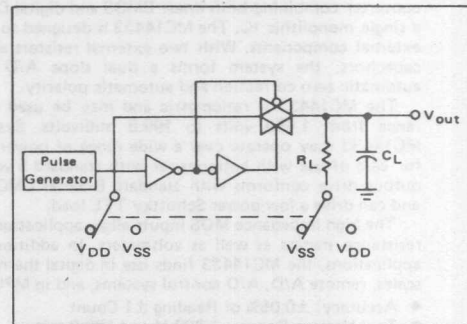


FIGURE 3 - BANDWIDTH AND FEEDTHROUGH ATTENUATION

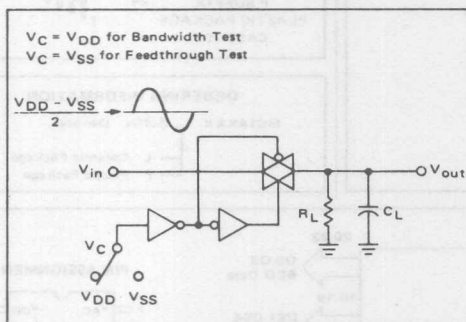


FIGURE 4 - CROSSTALK BETWEEN ANY TWO SWITCHES

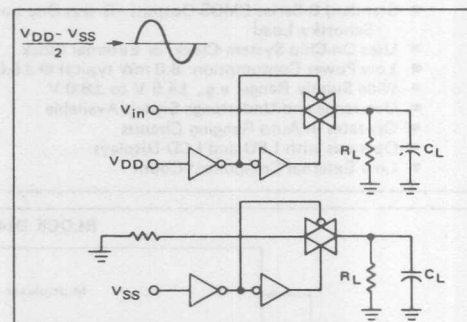


FIGURE 5 - CROSSTALK, CONTROL TO OUTPUT

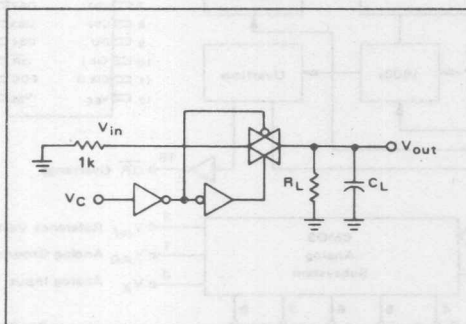
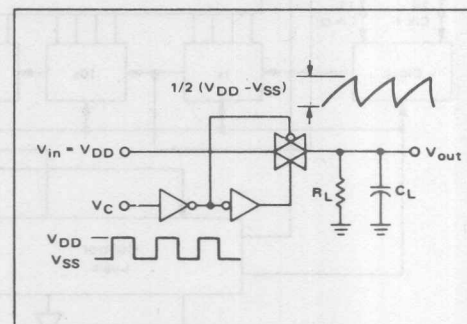


FIGURE 6 - MAXIMUM CONTROL FREQUENCY



MC14433

3½ DIGIT A/D CONVERTER

The MC14433 is a high performance, low power, 3½ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The MC14433 is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual slope A/D converter with automatic zero correction and automatic polarity.

The MC14433 is ratiometric and may be used over a full-scale range from 1.999 volts to 199.9 millivolts. Systems using the MC14433 may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5 volt supplies. The output drive conforms with standard B-Series CMOS specifications and can drive a low-power Schottky TTL load.

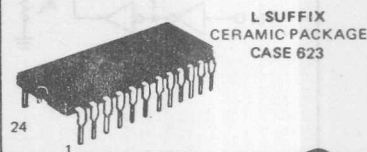
The high impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the MC14433 finds use in digital thermometers, digital scales, remote A/D, A/D control systems, and in MPU systems.

- Accuracy: $\pm 0.05\%$ of Reading ± 1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions/s
- $Z_{in} > 1000$ M ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs—Drives One Low Power Schottky Load
- Uses On-Chip System Clock, or External Clock
- Low Power Consumption: 8.0 mW typical @ ± 5.0 V
- Wide Supply Range: e.g., ± 4.5 V to ± 8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates with LED and LCD Displays
- Low External Component Count

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

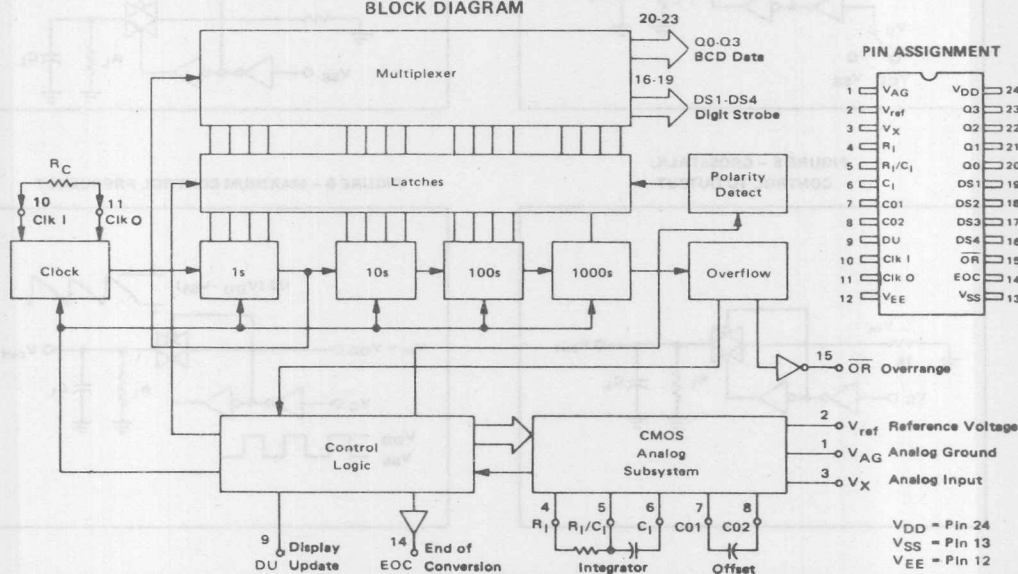
3½ DIGIT A/D CONVERTER



ORDERING INFORMATION

MC14XXX Suffix Denotes
 L Ceramic Package
 P Plastic Package

BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18	Vdc
Voltage, any pin, referenced to V_{EE}	V	-0.5 to $V_{DD} + 0.5$	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0$ or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage — V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	-2.8 to -8.0	Vdc
Clock Frequency	f_{Clk}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 \pm 20%	μ F

ELECTRICAL CHARACTERISTICS ($C_I = 0.1 \mu$ F mylar, $R_I = 470 \text{ k}\Omega$ @ $V_{ref} = 2.000 \text{ V}$, $R_I = 27 \text{ k}\Omega$ @ $V_{ref} = 200.0 \text{ mV}$, $C_O = 0.1 \mu$ F, $R_C = 300 \text{ k}\Omega$; all voltages referenced to Analog Ground, pin 1.)

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	-40°C		25°C			85°C		Unit
				Min	Max	Min	Typ	Max	Min	Max	
Linearity-Output Reading (Note 1) ($V_{ref} = 2.000 \text{ V}$)	—	5.0	-5.0	—	—	-0.05 -Count	+0.05	+0.05 +Count	—	—	%rdg
($V_{ref} = 200.0 \text{ mV}$)	—	5.0	-5.0	—	—	—	+0.05	—	—	—	
Stability-Output Reading (Note 2) ($V_X = 1.990 \text{ V}$, $V_{ref} = 2.000 \text{ V}$) ($V_X = 199.0 \text{ mV}$, $V_{ref} = 200.0 \text{ mV}$)	—	5.0	-5.0	—	—	—	—	2	—	—	LSD
($V_X = 199.0 \text{ mV}$, $V_{ref} = 200.0 \text{ mV}$)	—	5.0	-5.0	—	—	—	—	3	—	—	
Zero-Output Reading ($V_X = 0 \text{ V}$, $V_{ref} = 2.000 \text{ V}$)	—	5.0	-5.0	—	—	—	0	0	—	—	LSD
Bias Current — Analog Input	—	5.0	-5.0	—	—	—	± 20	± 100	—	—	pAdc
Reference Input	—	5.0	-5.0	—	—	—	± 20	± 100	—	—	
Analog Ground	—	5.0	-5.0	—	—	—	± 20	± 500	—	—	
Common Mode Rejection ($V_X = 1.4 \text{ V}$, $V_{ref} = 2.000 \text{ V}$, $f_{oc} = 32 \text{ kHz}$)	—	5.0	-5.0	—	—	—	65	—	—	—	dB
Output Voltage — Pins 14 to 23 ($V_{SS} = 0 \text{ V}$) "0" Level	V_{OL}	5.0	-5.0	—	0.05	—	0	0.05	—	0.05	Vdc
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	
($V_{SS} = -5.0 \text{ V}$) "0" Level	V_{OL}	5.0	-5.0	—	4.95	—	-5.0	-4.95	—	-4.95	
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	
Output Current — Pins 14 to 23 ($V_{SS} = 0 \text{ V}$) ($V_{OH} = 4.6 \text{ V}$) Source ($V_{OL} = 0.4 \text{ V}$) Sink	I_{OH} I_{OL}	5.0 5.0	-5.0 -5.0	-0.25 0.64	—	-0.2 0.51	-0.36 0.88	—	-0.14 0.36	—	mAdc
($V_{SS} = -5.0 \text{ V}$) ($V_{OH} = 4.5 \text{ V}$) Source ($V_{OL} = -4.5 \text{ V}$) Sink	I_{OH} I_{OL}	5.0 5.0	-5.0 -5.0	-0.62 1.6	—	-0.5 1.3	-0.9 2.25	—	-0.35 0.9	—	
Clock Frequency ($R_C = 300 \text{ k}\Omega$)	f_{Clk}	5.0	-5.0	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5.0	-5.0	—	± 0.3	—	0.00001	± 0.3	—	± 1.0	μ Adc
Quiescent Current (V_{DD} to V_{EE} , $I_{SS} = 0$)	I_Q	5.0 8.0	-5.0 -8.0	—	3.7 7.4	—	0.9 1.8	2.0 4.0	—	1.6 3.2	mAdc
DC Supply Rejection (V_{DD} to V_{EE} , $I_{SS} = 0$, $V_{ref} = 2.000 \text{ V}$)	—	5.0	-5.0	—	—	—	0.5	—	—	—	mV/V

Note 1: Accuracy — The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

Note 2: 3 LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL ROLLOVER ERROR
versus POWER SUPPLY SKEW

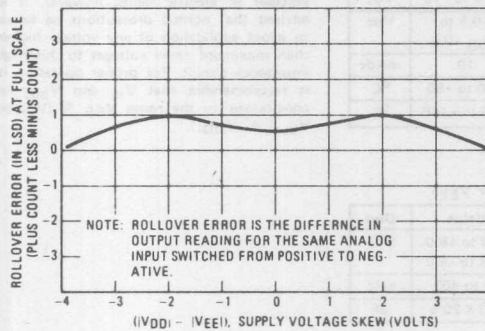


FIGURE 2 – TYPICAL QUIESCENT POWER SUPPLY CURRENT
versus TEMPERATURE

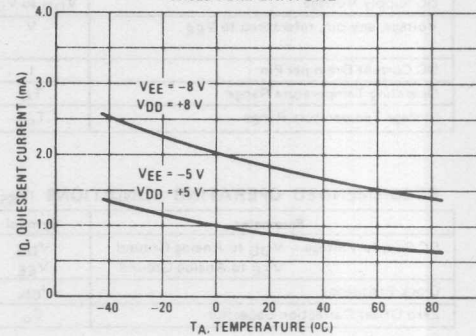


FIGURE 3 – TYPICAL N-CHANNEL SINK CURRENT
AT VDD-VSS = 5 VOLTS

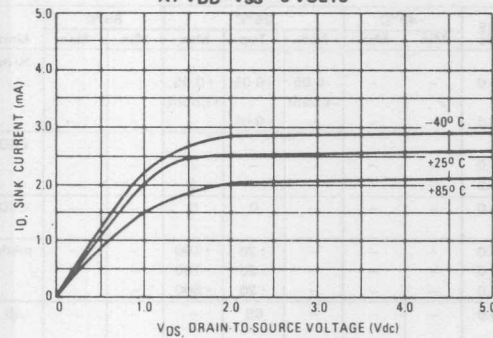


FIGURE 4 – TYPICAL P-CHANNEL SOURCE CURRENT
AT VDD-VSS = 5 VOLTS

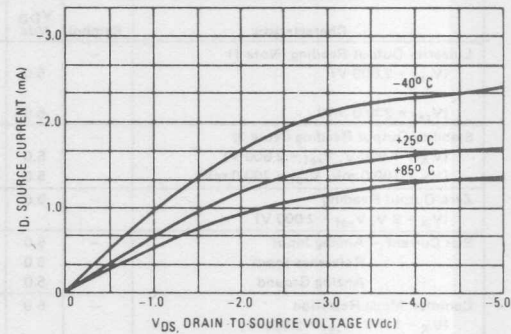


FIGURE 5 – TYPICAL CLOCK FREQUENCY
versus RESISTOR (R_C)

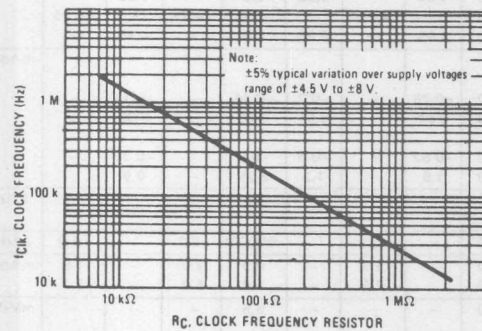
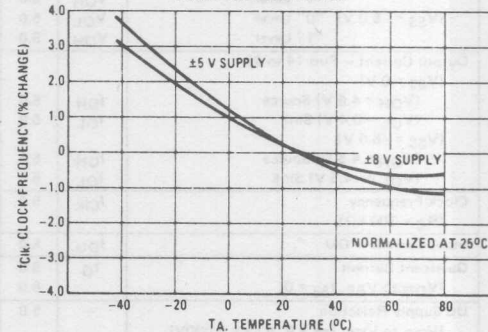


FIGURE 6 – TYPICAL % CHANGE OF CLOCK FREQUENCY
versus TEMPERATURE



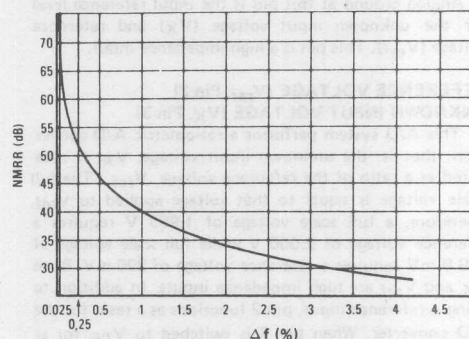
CONVERSION RATE	$= \frac{\text{CLOCK FREQUENCY}}{16,400} \pm 1.5\%$
MULTIPLEX RATE	$= \frac{\text{CLOCK FREQUENCY}}{80}$

TYPICAL CHARACTERISTICS

FIGURE (Table) 7 — FOR BEST 50 Hz
NMRR (Normal Mode Rejection Ratio)
AT DIFFERENT CLOCK FREQUENCIES

Clock frequency (KHz)	Integration time (msec)	Conversion rate (~ Hz)
200	20	12.5
100	40	6.25
66.6	60	4.16
50	80	3.12
40	100	2.5

The NMRR depends on the difference Δf (°/o) between a multiple of the power line frequency and the clock frequency.

FIGURE 8 — NMRR (dB) vs Δf (%)

DEVICE OPERATION

ANALOG GROUND (V_{AG} , Pin 1)

Analog ground at this pin is the input reference level for the unknown input voltage (V_X) and reference voltage (V_{ref}). This pin is a high impedance input.

REFERENCE VOLTAGE (V_{ref} , Pin 2)

UNKNOWN INPUT VOLTAGE (V_X , Pin 3)

This A/D system performs a ratiometric A/D conversion; that is, the unknown input voltage, V_X , is measured as a ratio of the reference voltage, V_{ref} . The full scale voltage is equal to that voltage applied to V_{ref} . Therefore, a full scale voltage of 1.999 V requires a reference voltage of 2.000 V while full scale voltage of 199.9 mV requires a reference voltage of 200 mV. Both V_X and V_{ref} are high impedance inputs. In addition to being a reference input, pin 2 functions as a reset for the A/D converter. When pin 2 is switched to V_{EE} for at least 5 clock cycles, the system is reset to the beginning of a conversion cycle.

EXTERNAL COMPONENTS (R_I , R_I/C_I , C_I ; Pins 4, 5, 6)

These pins are for external components for the integration used in the dual ramp A/D conversion. A typical value for the capacitor is 0.1 μ F (mylar) while the resistor should be 470 k Ω for 2.0 V full scale operation and 27 k Ω for 200 mV full scale operation. These values are for a 66 kHz clock frequency which will produce a conversion time of approximately 250 ms. The equations governing the calculation for the values for integrator components are as follows:

$$R_I = \frac{V_X(\max)}{C_I} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X(\max) - 0.5$$

$$T = 4000 \times \frac{1}{f_{Clk}}$$

where:

R_I is in k Ω

V_{DD} is the voltage at pin 24 referenced to V_{AG}

V_X is the voltage at pin 3 referenced to V_{AG}

f_{Clk} is the clock frequency at pin 10 in kHz

Example:

$C_I = 0.1 \mu$ F

$V_{DD} = 5.0$ volts

$f_{Clk} = 66$ kHz

For $V_X(\max) = 2.0$ volts

$R_I = 480$ k Ω (use 470 k $\Omega \pm 5\%$)

For $V_X(\max) = 200$ mV

$R_I = 28$ k Ω (use 27 k $\Omega \pm 5\%$)

Note that for worst case conditions, the minimum allowable value for R_I is a function of C_I min, V_{DD} min, and f_{Clk} max. The worst-case condition does not allow

$V + V_X$ to exceed V_{DD} . The 0.5 V factor in the above equation for ΔV is for safety margin.

OFFSET CAPACITOR ($CO1$, $CO2$; Pins 7, 8)

These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μ F.

DISPLAY UPDATE INPUT (DU , Pin 9)

If a positive edge is received on this input prior to the ramp-down cycle, new data will be strobed into the output latches during that conversion cycle. When this pin is wired directly to the EOC output (pin 14), every conversion will be displayed. When this pin is driven from an external source, the voltage should be referenced to V_{SS} .

CLOCK ($Clk I$, $Clk O$, Pins 10, 11)

The MC14433 device contains its own oscillator system clock. A single resistor connected between pins 10 and 11 sets the clock frequency. If increased stability is desired, these pins will support a crystal or LC circuit. The clock input, pin 10, may also be driven from an external clock source which need have only standard CMOS output drive. For external clock inputs this pin is referenced to V_{EE} . A 300 k Ω resistor results in clock frequency of about 66 kHz. (See the typical characteristic curves.) For alternate circuits see Figure 7.

NEGATIVE POWER SUPPLY (V_{EE} , Pin 12)

This is the connection for the most negative power supply voltage. The typical current is 0.8 mA. Note the current for the output drive circuit is not returned through this pin, but through pin 13.

NEGATIVE POWER SUPPLY FOR OUTPUT CIRCUITRY (V_{SS} , Pin 13)

This is the low voltage level for the output pins of the MC14433 (BCD, Digit Selects, EOC, \overline{OR}). When this pin is connected to analog ground, the output voltage is from analog ground to V_{DD} . When connected to V_{EE} , the output swing is from V_{EE} to V_{DD} . The allowable operating range for V_{SS} is between $V_{DD} - 3.0$ volts and V_{EE} .

END OF CONVERSION (EOC, Pin 14)

The EOC output produces a pulse at the end of each conversion cycle. This pulse width is equivalent to one half the period of the system clock (pin 11).

OVERRANGE (\overline{OR} , Pin 15)

The \overline{OR} pin is low when V_X exceeds V_{ref} . Normally it is high.

DIGIT SELECT ($DS4$, $DS3$, $DS2$, $DS1$; Pins 16, 17, 18, 19)

The digit select output is high when the respective

digit is selected. The most significant digit (1/2 digit) turns on immediately after an EOC pulse followed by the remaining digits, sequencing from MSD to LSD. An inter-digit blanking time of two clock periods is included to ensure that the BCD data has settled. The multiplex rate is equal to the clock frequency divided by 80. Thus, with a system clock rate of 66 kHz, the multiplex rate would be 0.8 kHz. Relative timing among digital select output and EOC signals is shown in the Digit Select Timing Diagram, Figure 8.

BCD DATA OUTPUTS (Q0, Q1, Q2, Q3, Pins 20, 21, 22, 23)

Multiplexed BCD outputs contain 3 full digits of information during DS2, 3, 4, while during DS1, the 1/2 digit, overrange, underrange and polarity are available. The adjacent truth table shows the formats of the information during DS1.

POSITIVE POWER SUPPLY (V_{DD}, Pin 24)

The most positive supply voltage pin.

TRUTH TABLE

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
-0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
-0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1
-1	0	0	0	0	0 → 1
+1 OR	0	1	1	1	7 → 1
-1 OR	0	0	1	1	3 → 1

Notes for Truth Table

Q3 - 1/2 digit, low for "1", high for "0"

Q2 - Polarity: "1" = positive, "0" = negative

Q0 - Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the 1/2 digit of the display, 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoring circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

Caution: If the most significant digit is connected to a display other than a "1" only, such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

FIGURE 7 - ALTERNATE OSCILLATOR CIRCUITS

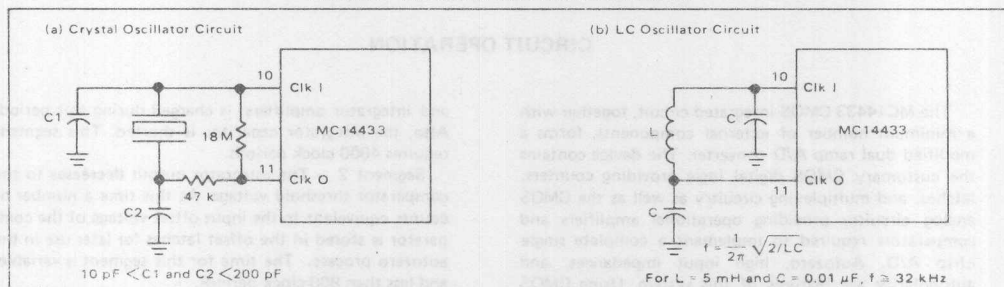


FIGURE 8 - DIGIT SELECT TIMING DIAGRAM

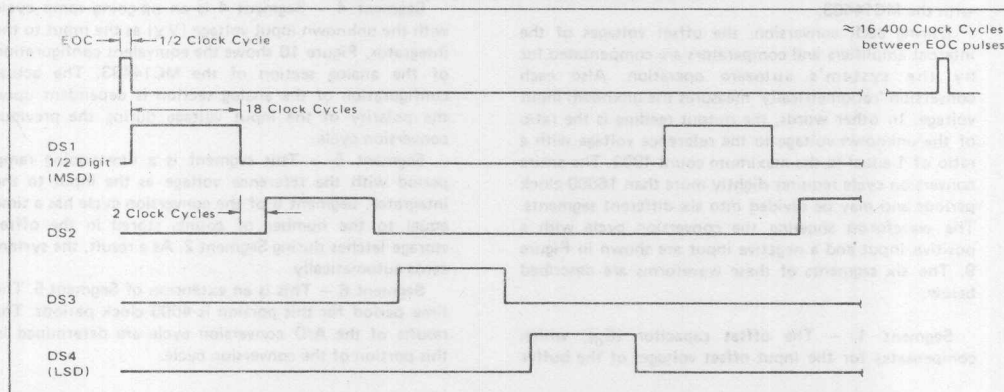


FIGURE 9 – INTEGRATOR WAVEFORMS AT PIN 6

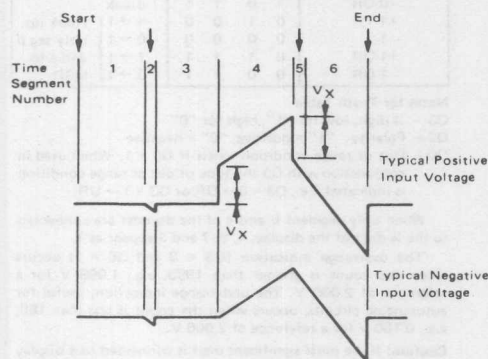
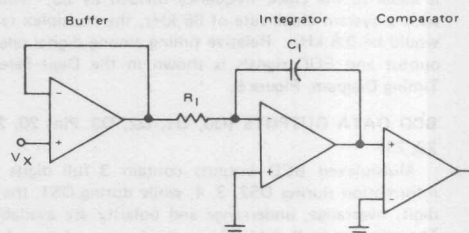


FIGURE 10 – EQUIVALENT CIRCUIT DIAGRAMS OF THE ANALOG SECTION DURING SEGMENT 4 OF THE TIMING CYCLE



CIRCUIT OPERATION

The MC14433 CMOS integrated circuit, together with a minimum number of external components, forms a modified dual ramp A/D converter. The device contains the customary CMOS digital logic providing counters, latches, and multiplexing circuitry as well as the CMOS analog circuitry providing operational amplifiers and comparators required to implement a complete single chip A/D. Autozero, high input impedances, and autopolarity are features of this system. Using CMOS technology, an A/D with a wide range of power supply voltage and low power consumption is now available with the MC14433.

During each conversion, the offset voltages of the internal amplifiers and comparators are compensated for by the system's autozero operation. Also each conversion 'ratiometrically' measures the unknown input voltage. In other words, the output reading is the ratio of the unknown voltage to the reference voltage with a ratio of 1 equal to the maximum count 1999. The entire conversion cycle requires slightly more than 16000 clock periods and may be divided into six different segments. The waveforms showing the conversion cycle with a positive input and a negative input are shown in Figure 9. The six segments of these waveforms are described below.

Segment 1 – The offset capacitor (C_O), which compensates for the input offset voltages of the buffer

and integrator amplifiers, is charged during this period. Also, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 – The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the autozero process. The time for this segment is variable, and less than 800 clock periods.

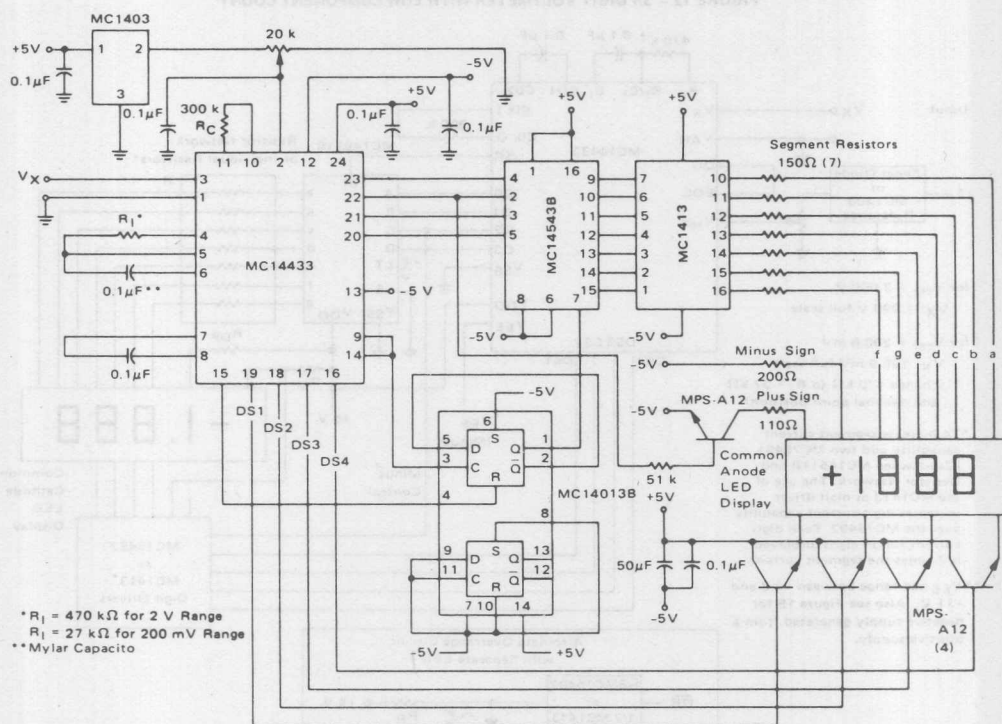
Segment 3 – This segment of the conversion cycle is the same as Segment 1.

Segment 4 – Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. Figure 10 shows the equivalent configuration of the analog section of the MC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 – This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 – This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

FIGURE 11 – 3-1/2 DIGIT VOLTMEETER—COMMON ANODE DISPLAYS, FLASHING OVERRANGE



APPLICATIONS INFORMATION

3½ DIGIT VOLTMEETER – COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3½ digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 11. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_1 is also changed, as shown on the diagram.

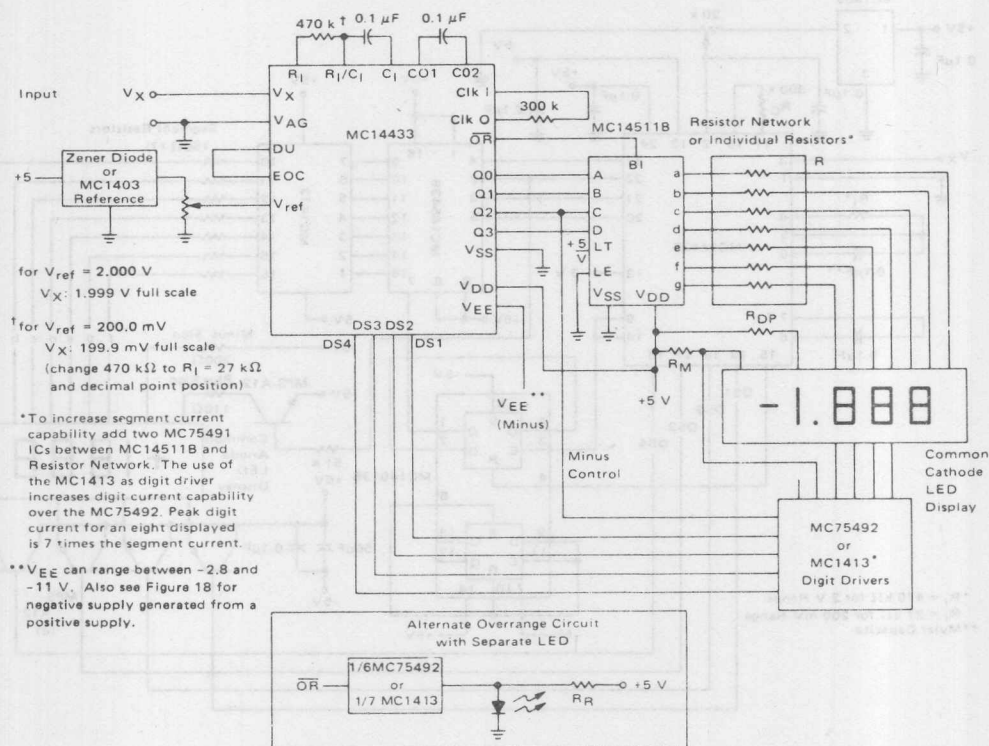
When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with ½ MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 darlington transistors operating in an emitter follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in the above figure.

The power supply for the system is shown as a dual $\pm 5 \text{ V}$ supply. However, the MC14433 will operate over a wide range of voltages, and balance between the +5 and -5 V supplies is *not* required. See the recommended operating conditions and Figure 1, on pages 2 and 3.

FIGURE 12 — 3½ DIGIT VOLT METER WITH LOW COMPONENT COUNT



3½ DIGIT VOLT METER WITH LOW COMPONENT COUNT USING COMMON CATHODE DISPLAYS

The 3½ digit voltmeter of Figure 12 is an example of the use of the MC14433 in a system with a minimum of components. This circuit uses only 11 components in addition to the MC14433 to operate the MC14433 and drive the LED displays.

In this circuit the MC14511B provides the segment drive for the 3½ digits. The MC75492 or MC1413 provides sink for digit current. (The MC75492 or MC1413 are devices with 6 or 7 darlington transistors respectively with common emitters.) The worst case digit current is 7 times the segment current at ¼ duty cycle. The peak segment current is limited by the value of R . The current for the display flows from V_{DD} (+5 V) to ground and does not flow through the V_{EE} (negative) supply. The minus sign is controlled by one section of the MC75492 or MC1413 and is turned off by shunting the current through R_M to ground, bypassing the minus sign LED. The minus sign is derived from the Q2 output. The decimal point brightness is controlled by resistor R_{DP} . Since the brightness and the type and size of LED

display are the choice of the designer, the values of resistors R , R_M , R_{DP} , and R_R that govern brightness are not given.

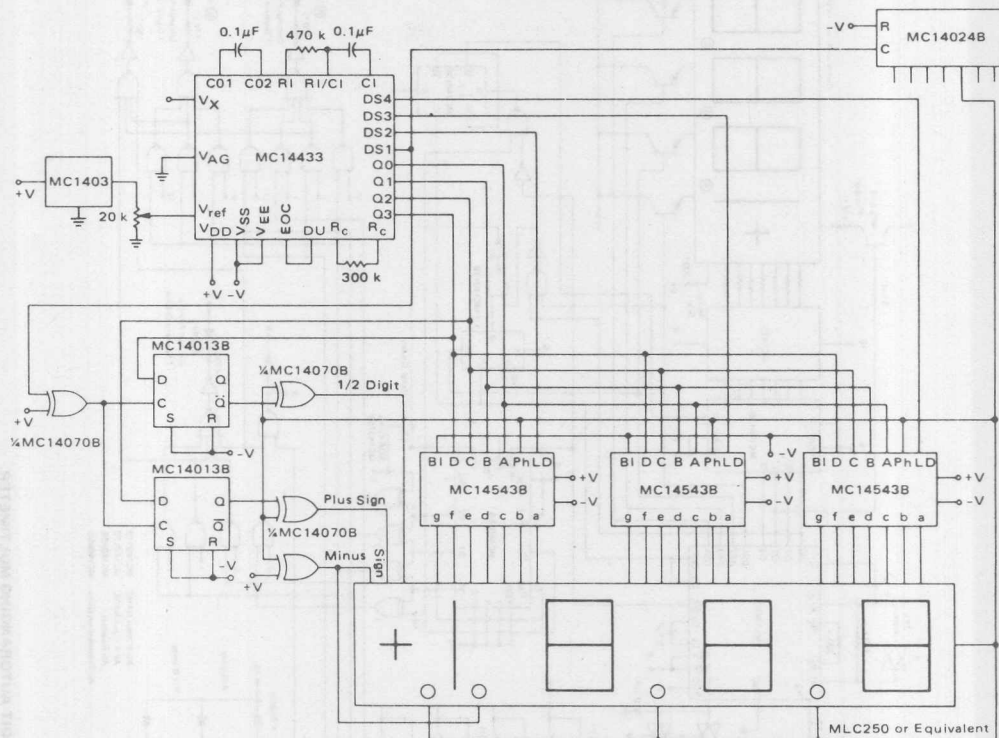
During an overrange condition the 3½ digit display is blanked at the BI pin on the MC14511B. The decimal point and minus sign will remain on during a negative overrange condition. In addition, an alternate overrange circuit with separate LED is shown. There are leftover sections in either the MC75492 or MC1413.

3½ DIGIT VOLT METER WITH LCD DISPLAY

A circuit for a 3½ digit voltmeter with a liquid crystal display is shown in Figure 13. Three MC14543B LCD latch/decoder/display drivers are used to demultiplex, decode the three digits, and drive the LCD. The half digit and polarity are demultiplexed with the MC14013B dual D flip-flop.

Since the LCD is best driven by an ac signal across the LCD, the low-frequency square wave drive for the LCD is derived from the MC14024B binary counter which divides the digit select output from the A/D. This low frequency square wave is connected to the backplane of

FIGURE 13 – 3½ DIGIT VOLTMETER WITH LCD DISPLAY



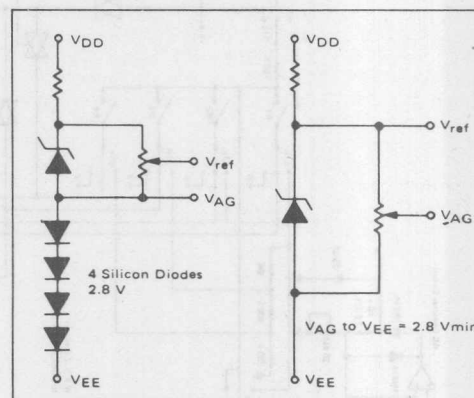
the LCD and to the individual segments through the combination of the output circuitry of the MC14543B and the exclusive OR gates at the outputs of the MC14013B. Alternatively the square wave can be derived from a 50/60 Hz input signal when available.

The minus sign and the decimal point to the right of the half digit are connected to the inverted low frequency square wave signal. Unused decimal points are tied directly to the low frequency square wave.

The system shown operates from two power supplies (plus and minus). Alternatively one supply can be used when V_{SS} is connected to V_{EE} . In this case a level must be set for analog ground, V_{AG} , which must be at least 2.8 V above V_{EE} . This circuit may be implemented with a resistor network, resistor/forward-biased diode network or resistor-zener diode network. For example, a 9 V supply can be used with 3 V between V_{AG} and V_{EE} , leaving 6 V for V_{DD} to V_{AG} . This system leaves a comfortable margin for battery degeneration (end of life). Two versions of this circuit for single supply operation is shown in Figure 14.

For panel meter operation from a single 5 V supply, a negative supply can be generated as shown in Figure 18.

FIGURE 14 – TWO CIRCUITS FOR GENERATION OF V_{ref} AND V_{AG} FROM A SINGLE SUPPLY



3½ DIGIT AUTORANGING MULTIMETER

An autoranging multimeter including ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A fullscale and resistance ranges from 2 k Ω to 2 M Ω fullscale is shown in Figure 15. In this multimeter only two input jacks are required for all ranges and functions, eliminating the need for changing leads on the instrument when changing ranges or functions. Although only four ranges are provided for each function, the technique used may be expanded to more ranges if desired. Range switching uses mechanical relays. However, the relays may be replaced with solid state analog switches.

The MC14433 provides the overrange and underrange control signals for the automatic ranging circuits. For additional information, see Motorola Application Note AN-769, "Autoranging Digital Multimeter Using the MC14433 CMOS A/D Converter."

PARALLEL BCD DATA OUTPUT CIRCUIT

The output of the MC14433 may be demultiplexed to produce parallel BCD data as shown in Figure 16. Two levels of latches are required for a complete demultiplexing of the data since the outputs of the MC14042B latches change sequentially with the DS1 to DS4 strobe pulses. To key output validity to one leading edge, i.e., that of the EOC signal of the MC14433, information is transferred to the second set of latches (MC14175B latches). A single set of latches can be used when reading of output is restricted to within 12,000 clock pulses after EOC. This requires synchronous system operation with respect to the BCD data bus.

In this system the output ground level is V_{SS} . In most cases, a two supply system with V_{SS} connected to V_{AG} is recommended. This allows connecting analog ground and digital ground together without destroying a power supply. This circuit works well with that of Figure 12.

FIGURE 16 — DEMULTIPLEXING FOR MC14433 BCD DATA

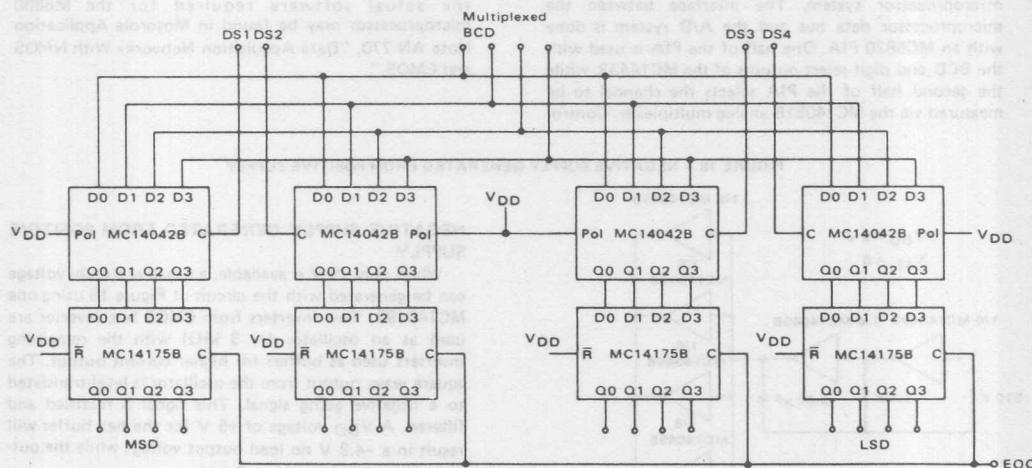
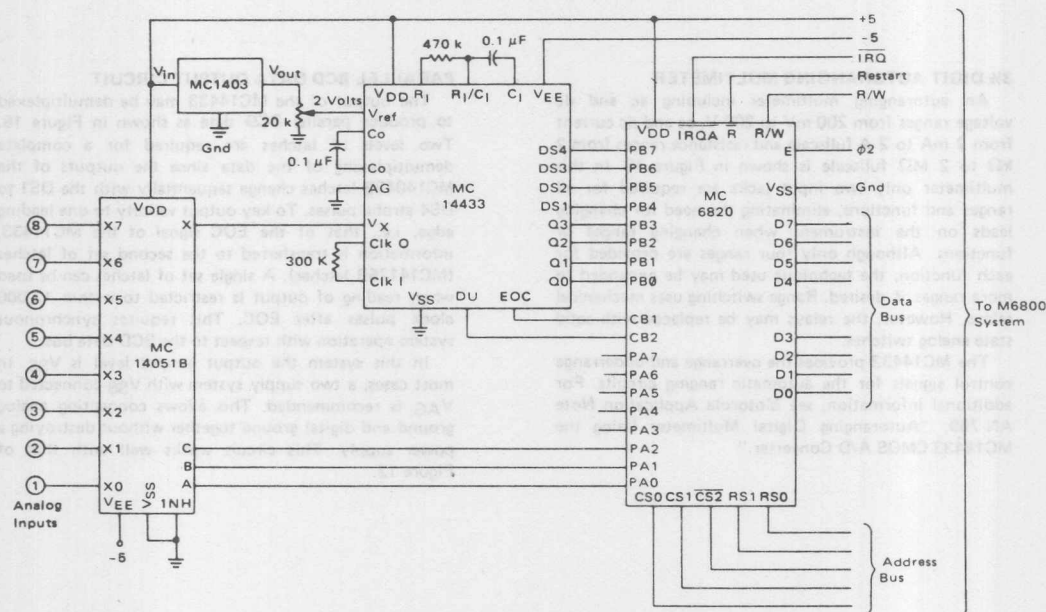


FIGURE 17 - CHANNEL DATA ACQUISITION HARDWARE



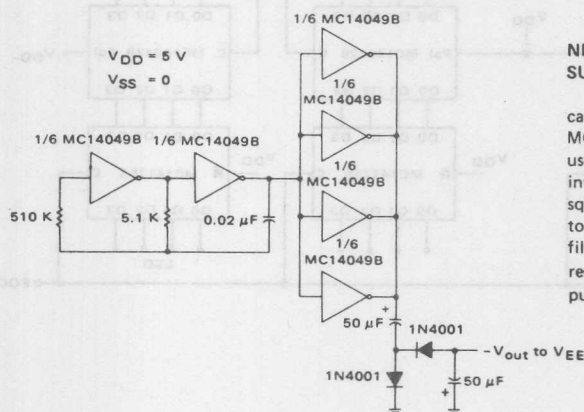
8 CHANNEL DATA ACQUISITION NETWORK

Figure 17 shows an 8 channel data acquisition network using the MC14433 and an M6800 microprocessor system. The interface between the microprocessor data bus and the A/D system is done with an MC6820 PIA. One half of the PIA is used with the BCD and digit select outputs of the MC14433, while the second half of the PIA selects the channel to be measured via the MC14051B analog multiplexer. Control

lines CB1 and CB2 are used for data flow control and are connected to DU and EOC of the MC14433.

A more detailed explanation of this system including the actual software required for the M6800 microprocessor may be found in Motorola Application Note AN-770, "Data Acquisition Networks With NMOS and CMOS."

FIGURE 18 - NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY



NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY

When only +5 V is available, a negative supply voltage can be generated with the circuit of Figure 18 using one MC14049B. Two inverters from CMOS hex inverter are used as an oscillator (≈ 3 kHz) with the remaining inverters used as buffers for higher current output. The square wave output from the oscillator is level-translated to a negative going signal. This signal is rectified and filtered. A V_{DD} voltage of +5 V for the hex buffer will result in a -4.3 V no load output voltage; while the output with a 2 mA load is ≈ 3.4 V.

MC14495

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT HEXADECIMAL LATCH/DECODER/DRIVER

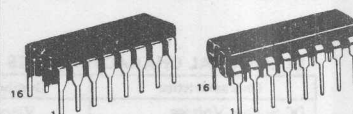
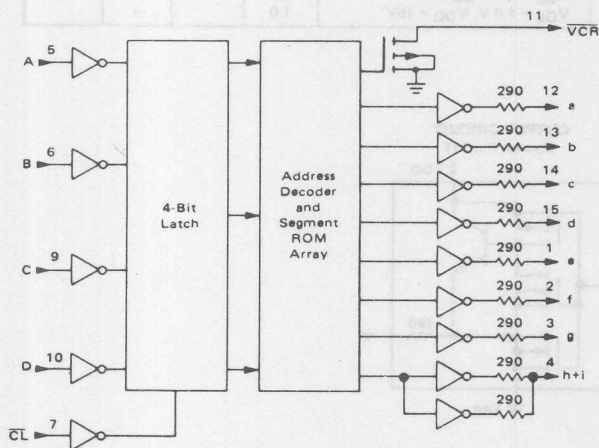
BCD-TO-SEVEN SEGMENT HEXADECIMAL LATCH/ DECODER/DRIVER

The MC14495 BCD-to-seven segment hexadecimal latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch. It can be used with LED seven segment displays without resistor interface at 5 volt supply. The resistors of typically 290 ohms are internal to the part.

Applications include MPU systems display driver, instrument display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs With Internal Limiting Resistance
- Latch Storage of Code
- Supply Voltage Range = 4.5 Vdc to 16 Vdc
- Internal Input Level Shift:
Input +5 CMOS to V_{DD} of +5 to +16 Vdc
Input +5 V TTL with Pull-up, to V_{DD} of +5 to +16 Vdc

BLOCK DIAGRAM



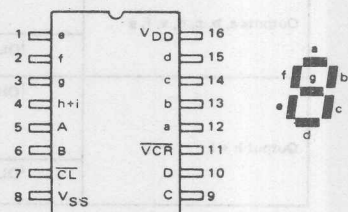
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

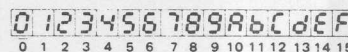
ORDERING INFORMATION

MC14XXX Suffix Denotes

L Ceramic Package
P Plastic Package



ALPHANUMERIC DISPLAY



TRUTH TABLE

INPUTS					OUTPUTS									
D	C	B	A		a	b	c	d	e	f	g	h+i	VCR	DISPLAY
0	0	0	0		1	1	1	1	1	0	0	0	Open	0
0	0	0	1		0	1	1	0	0	0	0	0	Open	1
0	0	1	0		1	1	0	1	1	0	1	0	Open	2
0	0	1	1		1	1	1	1	0	0	1	0	Open	3
0	1	0	0		0	1	1	0	0	1	1	0	Open	4
0	1	0	1		1	0	1	1	0	1	1	0	Open	5
0	1	1	0		1	0	1	1	1	1	1	0	Open	6
0	1	1	1		1	1	1	0	0	0	0	0	Open	7
1	0	0	0		1	1	1	1	1	1	1	0	Open	8
1	0	0	1		1	1	1	1	0	1	1	0	Open	9
1	0	1	0		1	1	1	0	1	1	1	1	Open	A
1	0	1	1		0	0	1	1	1	1	1	1	Open	b
1	1	0	0		1	0	0	1	1	1	0	1	Open	C
1	1	0	1		0	1	1	1	1	0	1	1	Open	d
1	1	1	0		1	0	0	1	1	1	1	1	Open	E
1	1	1	1		1	0	0	0	1	1	1	1	0	F

MC14495

MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Power (Source) per Output @ 25 °C Pins 1, 2, 3, 12, 13, 14, 15 Pin 14	P_{OHmax}	50 100	mW

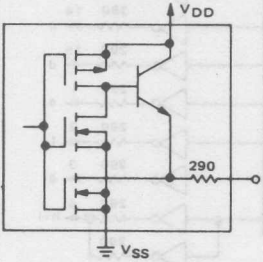
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

$$\pm P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$$

ELECTRICAL CHARACTERISTICS (All voltages referenced to $V_{SS} = 0$, $T_A = -25^\circ\text{C}$)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}		4.5		16	Vdc
Input Voltage	V_{IL}		—		0.8	Vdc
	V_{IH}	$V_{DD} = 15\text{V}$ $V_{DD} = 5.0\text{V}$	4.0 3.5		—	Vdc
Input Current	I_{in}		—		± 10	μA
Output VCR, Pin 11	I_{OH}	$V_{OH} = V_{DD}$	—		± 10	μA
Open Drain Output	I_{OL}	$V_{OL} = 0.5\text{V}$, $V_{DD} = 5.0\text{V}$ $V_{OL} = 0.5\text{V}$, $V_{DD} = 15\text{V}$	0.2 1.0		—	mA
Outputs a, b, c, d, e, f, g	I_{OH}	$V_{OH} = 2.0\text{V}$, $V_{DD} = 5.0\text{V}$ $V_{OH} = 1.5\text{V}$, $V_{DD} = 5.0\text{V}$ $V_{OH} = 12\text{V}$, $V_{DD} = 15\text{V}$ $V_{OH} = 11.5\text{V}$, $V_{DD} = 15\text{V}$	-7.5 — -7.5 —		-11.5 — -11.5	mA
	I_{OL}	$V_{OL} = 1.0\text{V}$, $V_{DD} = 5.0\text{V}$ $V_{OL} = 1.0\text{V}$, $V_{DD} = 15\text{V}$	0.1 0.5		—	mA
Output h + i	I_{OH}	$V_{OH} = 2.0\text{V}$, $V_{DD} = 5.0\text{V}$ $V_{OH} = 1.5\text{V}$, $V_{DD} = 5.0\text{V}$ $V_{OH} = 12\text{V}$, $V_{DD} = 15\text{V}$ $V_{OH} = 11.5\text{V}$, $V_{DD} = 15\text{V}$	-15 — -15 —		— -23 -23	mA
	I_{OL}	$V_{OL} = 1\text{V}$, $V_{DD} = 5.0\text{V}$ $V_{OL} = 1.0\text{V}$, $V_{DD} = 15\text{V}$	0.2 1.0		—	mA

OUTPUT CIRCUIT (Except Pin 11)



INPUT/OUTPUT FUNCTIONS

Segment Driver (a, b, c, d, e, f, g, h, i; Pins 1; 2, 3, 4, 12, 13, 14, 15)

The segment drivers are emitter-follower NPN-transistors. To limit the output current, a resistor typically 290 ohms is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of $V_{DD} = 5.0$ volts.

OUTPUT (\overline{VCR} ; Pin 11)

This output is activated (goes to low) whenever the address corresponding to program 16 is selected. Otherwise the output is open. See the truth table.

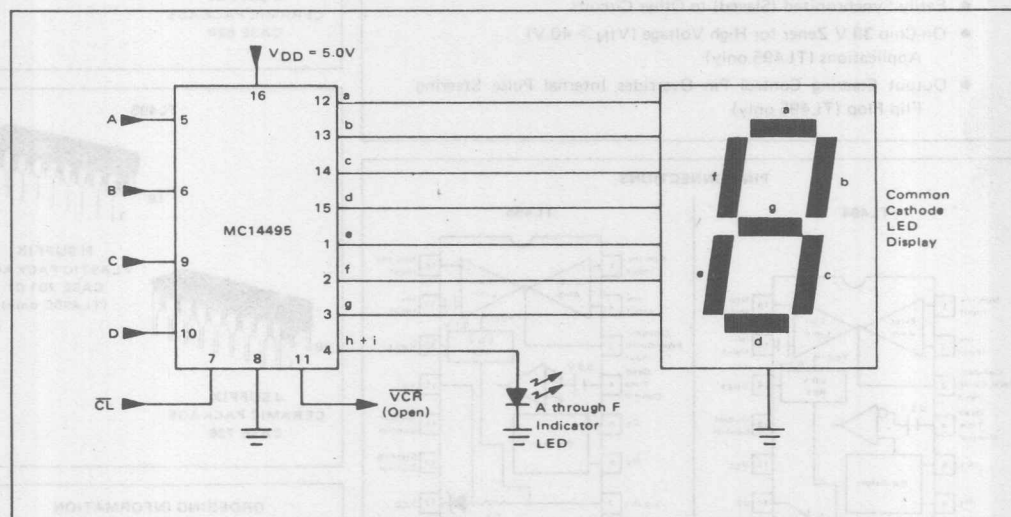
INPUT LATCH (A, B, C, D; Pins 5, 6, 8, 10)

The block diagram is shown on page 1. The inputs A, B, C, and D are fed to a 4-bit latch which is controlled by clock (\overline{CL}). Two modes of operation are available.

CLOCK (\overline{CL} ; Pin 7)

The data on the inputs A, B, C and D will pass through the latch and will be displayed immediately when the clock is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when $\overline{CL} = \text{low}$ and will be latched with the rising edge of \overline{CL} . The data will remain stored as long as \overline{CL} is high.

TYPICAL CIRCUIT • $V_{DD} = 5.0V$



TL494 TL495

Advance Information

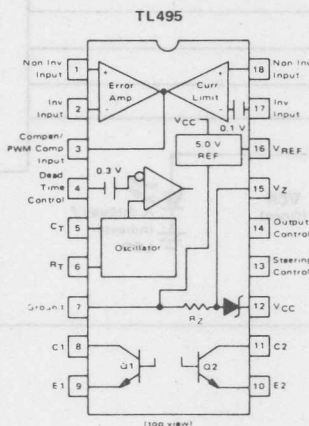
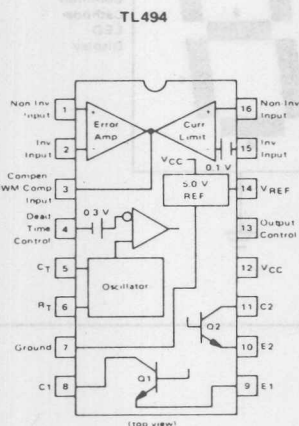
SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The TL494 and TL495 combine the best features of existing PWM control circuits and add other on-chip functions. These devices provide, on a single monolithic chip, all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

The TL494M/495M are specified over the military operating range of -55°C to $+125^{\circ}\text{C}$. The TL494C/495C are specified from 0°C to $+70^{\circ}\text{C}$.

- Uncommitted Output Transistors Capable of 250 mA Source or Sink
- On-Chip Error Amplifier and Current Limit Sense Amplifier
- On-Chip 5 V Reference
- Internal Protection from Double Pulsing of Outputs with Narrow Pulse Widths or with Supply Voltages below Specified Limits
- Dead Time Control Comparator
- Pulse-Steering Flip-Flop and Output Control Circuitry
- Easily Synchronized (Slaved) to Other Circuits
- On-Chip 39 V Zener for High Voltage ($V_{IN} > 40\text{ V}$) Applications (TL495 only)
- Output Steering Control Pin Overrides Internal Pulse Steering Flip-Flop (TL495 only)

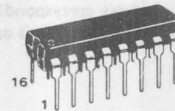
PIN CONNECTIONS



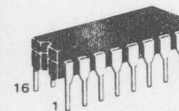
SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

TL494



N SUFFIX
PLASTIC PACKAGE
CASE 648
(TL494C only)



J SUFFIX
CERAMIC PACKAGE
CASE 620

TL495



N SUFFIX
PLASTIC PACKAGE
CASE 701-01
(TL495C only)



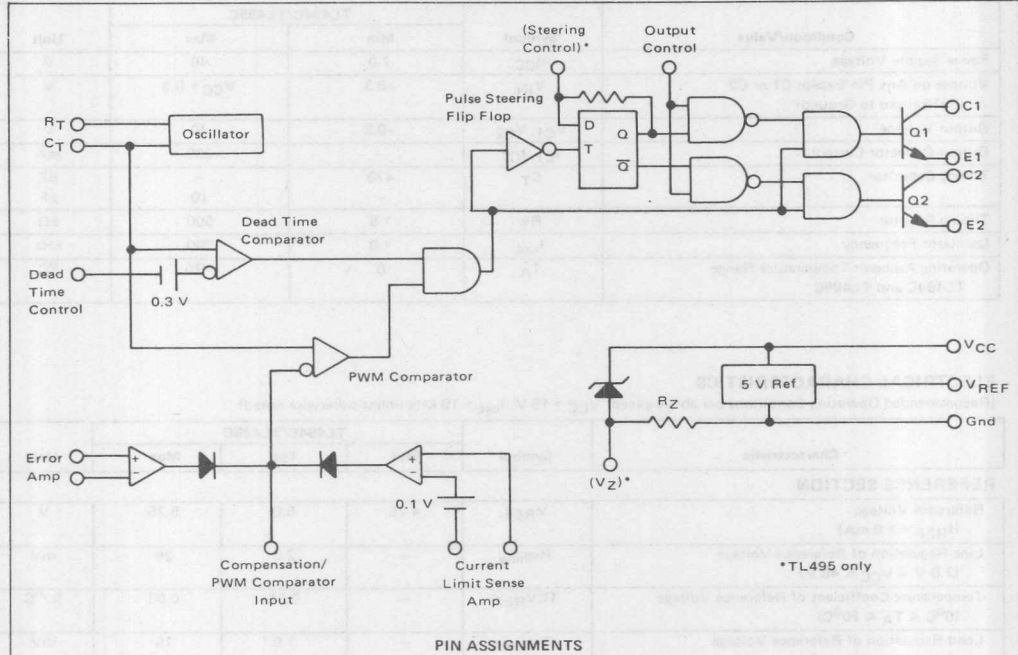
J SUFFIX
CERAMIC PACKAGE
CASE 726

ORDERING INFORMATION

Device	Temperature Range	Package
TL494CJ	0 to $+70^{\circ}\text{C}$	Ceramic DIP
TL494CN	0 to $+70^{\circ}\text{C}$	Plastic DIP
TL494MJ	-55 to $+125^{\circ}\text{C}$	Ceramic DIP
TL495CJ	0 to $+70^{\circ}\text{C}$	Ceramic DIP
TL495CN	0 to $+70^{\circ}\text{C}$	Plastic DIP
TL495MJ	-55 to $+125^{\circ}\text{C}$	Ceramic DIP

This is advance information and specifications are subject to change without notice.

EQUIVALENT CIRCUIT



PIN ASSIGNMENTS

Device	RT	CT	Dead Time Cntrl	Error Amp		C.L. Sense		VZ	Gnd	VREF	VCC	Q1		Q2		Out-put Cntrl	Steer-ing Cntrl	Compen-/ PWM Comp Input
				+	-	+	-					E1	C1	E2	C2			
TL494	6	5	4	1	2	16	15	N.A.	7	14	12	9	8	10	11	13	N.A.	3
TL495	6	5	4	1	2	18	17	15	7	16	12	9	8	10	11	14	13	3

MAXIMUM RATINGS (Operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL494M/495M	TL494C/495C	Unit
Power Supply Voltage	VCC	42		V
Any Pin to Gnd except C1 and C2	VIN	VCC + 0.3		V
Output Voltage	VC1, VC2	42		V
Output Collector Current	IC1, IC2	250		mA
Power Dissipation (TA ≤ 25°C)	PD	1000		mW
		See Thermal Information		
Operating Junction Temperature	TJ			°C
Plastic Package		-	125	
Ceramic Package		150	150	
Operating Ambient Temperature Range	TA	-55 to +125	0 to +70	°C
Storage Temperature Range	Tstg			°C
Ceramic Package		-65 to +150	-65 to +150	
Plastic Package		-	-55 to +125	

TL494, TL495

88A1T, 88A1T

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL494C/TL495C		Unit
		Min	Max	
Power Supply Voltage	V_{CC}	7.0	40	V
Voltage on Any Pin Except C1 or C2 (Referenced to Ground)	V_{IN}	-0.3	$V_{CC} + 0.3$	V
Output Voltage	V_{C1}, V_{C2}	-0.3	40	V
Output Collector Current	I_{C1}, I_{C2}	—	200	mA
Timing Capacitor	C_T	470	—	pF
		—	10	μF
Timing Resistor	R_T	1.8	500	k Ω
Oscillator Frequency	f_{osc}	1.0	300	kHz
Operating Ambient Temperature Range TL494C and TL495C	T_A	0	+70	$^{\circ}C$

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions per above except $V_{CC} = 15$ V, $f_{osc} = 10$ kHz unless otherwise noted)

Characteristic	Symbol	TL494C/TL495C			Unit
		Min	Typ	Max	

REFERENCE SECTION

Reference Voltage ($I_{REF} = 1.0$ mA)	V_{REF}	4.75	5.0	5.25	V
Line Regulation of Reference Voltage (7.0 V $\leq V_{CC} \leq 40$ V)	Reg_{line}	—	2.0	25	mV
Temperature Coefficient of Reference Voltage ($0^{\circ}C \leq T_A \leq 70^{\circ}C$)	TCV_{REF}	—	0.01	0.03	%/ $^{\circ}C$
Load Regulation of Reference Voltage ($0 \leq I_{REF} \leq 10$ mA)	Reg_{load}	—	1.0	15	mV

OSCILLATOR SECTION

Oscillator Frequency ($C_T = 0.01$ μF , $R_T = 12$ k Ω)	f_{osc}	—	10	—	kHz
Oscillator Frequency Change with Temperature $0^{\circ}C \leq T_A \leq +70^{\circ}C$ ($C_T = 0.01$ μF , $R_T = 12$ k Ω)	Δf_{osc}	—	—	2	%

DEAD-TIME CONTROL SECTION

Input Bias Current (Pin 4) ($V_{CC} = 15$ V, 0 V $\leq V_{IN} \leq 5.25$ V)	$I_{B(DT)}$	-10	-2.0	0	μA
Maximum Duty Cycle, Each Output ($V_{CC} = 15$ V, Pin 4 = 0 V, "Output Control" Pin = V_{REF})	DC_{max}	45	—	—	%
Input Threshold Voltage Zero Duty Cycle Maximum Duty Cycle	$V_{TH(in)}$	— 0	3.0 —	3.3 —	V

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	TL494C/TL495C			Unit
		Min	Typ	Max	

ERROR AND CURRENT LIMIT AMPLIFIER SECTIONS

Error Amplifier Input Offset Voltage ($V_{O3} = 2.5 \text{ V}$)	$V_{IO(EA)}$	—	2.0	10	mV
Current Limit Amplifier Input Offset Voltage ($V_{ICM} = 0 \text{ V}$)	$V_{IO(CL)}$	88	110	132	mV
Input Offset Current ($V_{O3} = 2.5 \text{ V}$)	I_{IO}	—	25	250	nA
Input Bias Current ($V_{O3} = 2.5 \text{ V}$)	I_{IB}	—	0.2	1.0	μA
Input Common Mode Voltage Range ($7 \text{ V} \leq V_{CC} \leq 40 \text{ V}$)	V_{ICR}	-0.3	—	$V_{CC} - 2.0$	V
Large Signal Open Loop Voltage Gain ($\Delta V_{O3} = 3 \text{ V}, 0.5 \text{ V} \leq V_{O3} \leq 3.5 \text{ V}$)	A_{VOL}	60	74	—	db
Unity Gain Crossover Frequency	f_c	—	650	—	kHz
Output Sink Current ($0.5 \text{ V} \leq V_{O3} \leq 3.5 \text{ V}$)	I_{O-}	-0.3	-0.6	—	mA
Output Source Current ($0.5 \text{ V} \leq V_{O3} \leq 3.5 \text{ V}$)	I_{O+}	2.0	—	—	mA

PWM COMPARATOR SECTION (Pin 3)

Inhibit Threshold Voltage (Zero Duty Cycle)	V_{THI}	—	4.0	4.5	V
Input Sink Current	I_{I-}	-0.3	-0.6	—	mA

OUTPUT SECTION

Output Saturation Voltage Common-Emitter Configuration ($V_E = 0 \text{ V}, I_C = 200 \text{ mA}$)	$V_{CE(sat)}$	—	1.1	1.3	V
Emitter-Follower Configuration ($V_C = 15 \text{ V}, I_E = 200 \text{ mA}$)		—	1.5	2.5	
Output Collector Leakage Current ($V_{CC} = 40 \text{ V}, V_{CE} = 40 \text{ V}$)	I_{CEO}	—	2.0	200	μA
Output Short-Circuit Current, Each Output ($T_A = 25^\circ\text{C}$)	I_{OS}	—	450	—	mA

TL494, TL495

OUTPUT CONTROL PIN FUNCTIONAL TABLE

Output Control Pin		Output Control Pin Condition	Output Function
TL494	TL495		
13	14	$0\text{ V} \leq V_{OC} \leq 0.4\text{ V}$	Single-Ended or Parallel Output
		$2.4\text{ V} \leq V_{OC} \leq V_{REF}$	Push-Pull Output

OUTPUT CONTROL PIN

Characteristic	Symbol	TL494C/TL495C			Unit
		Min	Typ	Max	
Low-Level Input Current ($V_{OC} = 0.4\text{ V}$)	I_{OCL}	—	—	-1600	μA
High-Level Input Current ($V_{OC} = 2.4\text{ V}$)	I_{OCH}	—	—	+200	μA

STEERING CONTROL PIN FUNCTIONAL TABLE (Pin 13 on TL495 only)

Pin 13 Condition	Pin 14 Condition	Output Function
Open	$2.4\text{ V} \leq V_{OC} \leq V_{REF}$	Normal Push-Pull Operation
$0\text{ V} \leq V_{ST} \leq 0.4\text{ V}$		PWM Output at Q1
$2.4\text{ V} \leq V_{ST} \leq V_{REF}$		PWM Output at Q2

STEERING CONTROL PIN (TL495 only)

Characteristic	Symbol	TL495C			Unit
		Min	Typ	Max	
Low-Level Input Current ($V_{ST} = 0.4\text{ V}$)	I_{STL}	—	—	-200	μA
High-Level Input Current ($V_{ST} = 2.4\text{ V}$)	I_{STH}	—	—	+200	μA

ZENER CHARACTERISTICS (TL495 only)

Characteristic	Symbol	TL495C			Unit
		Min	Typ	Max	
Zener Voltage ($V_{CC} = 42\text{ V}$, $I_{15} = -2.0\text{ mA}$)	V_Z	—	39	—	V
Sink Current, Pin 15 ($V_{CC} = 15\text{ V}$, $V_{15} = 1.0\text{ V}$)	I_{RZ}	—	0.3	—	mA

TOTAL DEVICE

Characteristic	Symbol	TL494C/TL495C			Unit
		Min	Typ	Max	
Standby Power Supply Current	I_{CC}	—	6.0	10	mA

OUTPUT AC CHARACTERISTICS

(Use Recommended Operating Conditions except $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	TL494C/ TL495C			Unit
		Min	Typ	Max	
Rise Time of Output Voltage Common-Emitter Configuration	t_r	—	100	200	ns
Emitter-Follower Configuration		—	100	200	
Fall Time of Output Voltage Common-Emitter Configuration	t_f	—	25	100	ns
Emitter-Follower Configuration		—	40	100	

FIGURE 1 – ERROR AMPLIFIER
TEST CIRCUIT

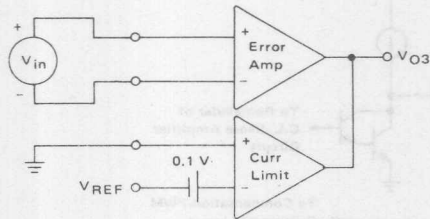


FIGURE 2 – CURRENT LIMIT SENSE
AMPLIFIER TEST CIRCUIT

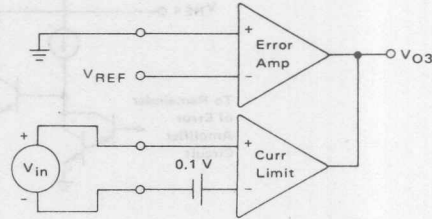


FIGURE 3 – COMMON-EMITTER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

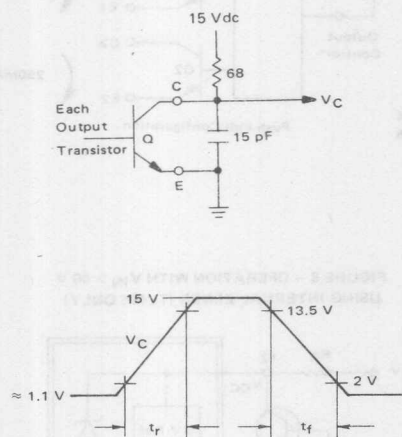


FIGURE 4 – EMITTER-FOLLOWER CONFIGURATION
TEST CIRCUIT AND WAVEFORM

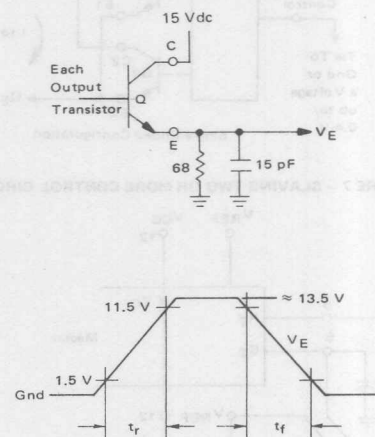


FIGURE 5 – ERROR AMPLIFIER AND CURRENT LIMIT SENSE
AMPLIFIER OUTPUT CIRCUITS

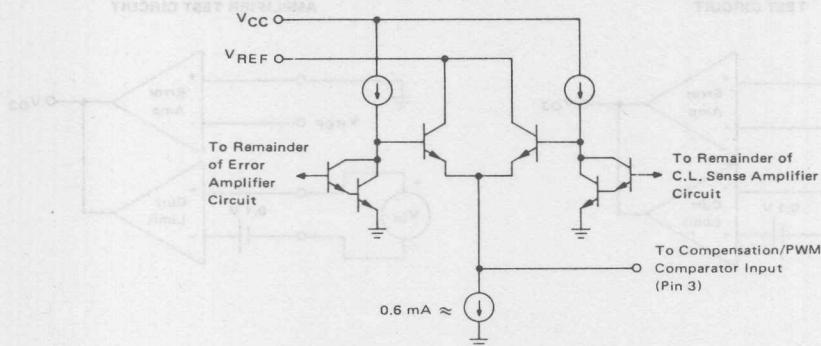


FIGURE 6 – OUTPUT CONNECTIONS FOR SINGLE-ENDED
AND PUSH-PULL CONFIGURATIONS

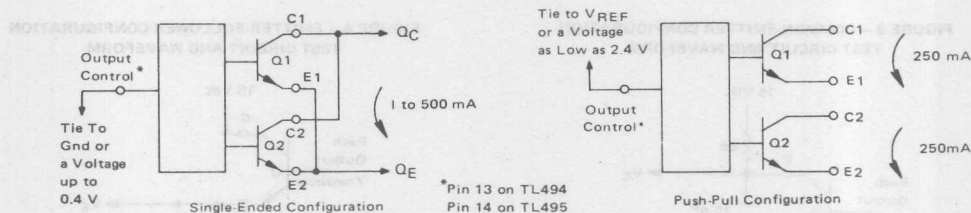


FIGURE 7 – SLAVING TWO OR MORE CONTROL CIRCUITS

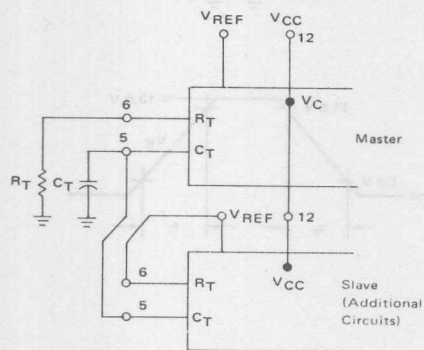


FIGURE 8 – OPERATION WITH $V_{IN} > 40\text{ V}$
USING INTERNAL ZENER (TL495 ONLY)

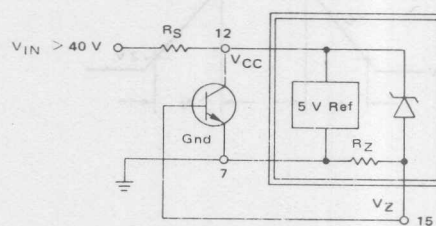
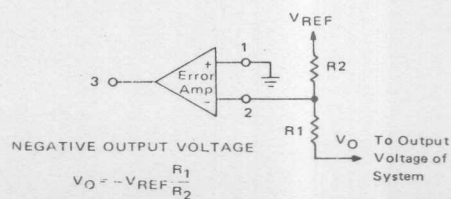
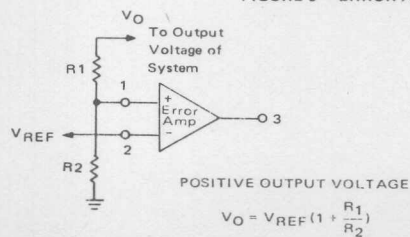


FIGURE 9 – ERROR AMPLIFIER SENSING TECHNIQUES



THERMAL INFORMATION

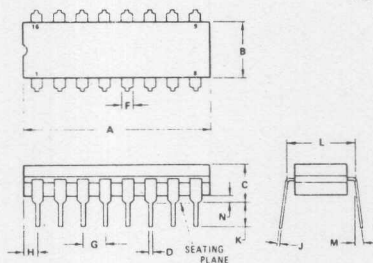
The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_D(T_A) = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)} \geq I_C V_{CC}$$

Where: $P_D(T_A)$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section.
 T_A = Maximum Desired Operating Ambient Temperature
 $R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient
 I_C = Total Sink Current
 V_{CC} = Supply Voltage

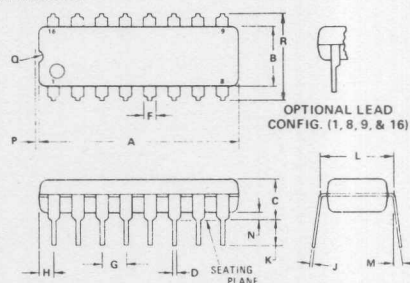
TL494 OUTLINE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	15°		15°	
N	0.51	1.02	0.020	0.040

- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
 - PKG INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
 - DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

J SUFFIX
CERAMIC PACKAGE
CASE 620
 $R_{\theta JA} = 100^{\circ}\text{C/W}$

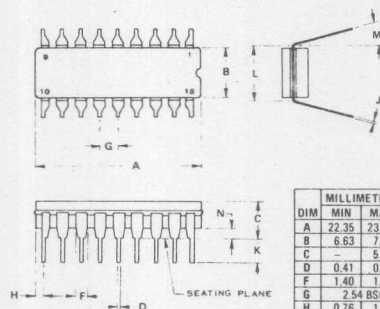


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.10	22.10	0.870	0.870
B	6.10	6.60	0.240	0.260
C	5.08	5.08	0.200	0.200
D	0.38	0.53	0.015	0.021
F	1.72	1.72	0.070	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	2.92	0.115	0.115
L	7.62 BSC		0.300 BSC	
M	15°		15°	
N	0.51	0.51	0.020	0.020
R	8.25	8.25	0.325	0.325

- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIMENSION "B" DOES NOT INCLUDE MOLO FLASH.
 - "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16.
 - DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

N SUFFIX
PLASTIC PACKAGE
CASE 648
(TL494C ONLY)
 $R_{\theta JA} = 100^{\circ}\text{C/W}$

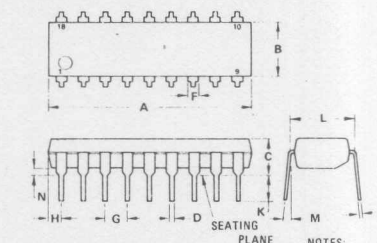
TL495 OUTLINE DIMENSIONS



- NOTES:
- LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 - DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIM "A" & "B" INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.63	7.24	0.261	0.285
C	5.08	5.08	0.200	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.76	1.02	0.030	0.040
J	0.13	0.38	0.005	0.015
K	4.44	4.44	0.175	0.175
L	7.37	8.00	0.290	0.315
M	15°		15°	
N	0.51	0.76	0.020	0.030

J SUFFIX
CERAMIC PACKAGE
CASE 726
 $R_{\theta JA} = 100^{\circ}\text{C/W (Typ)}$

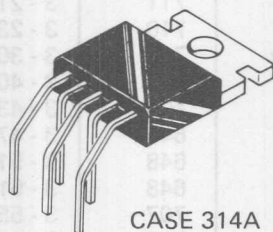


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	15°		15°	
N	0.51	1.02	0.020	0.040

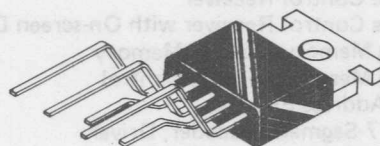
- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
 - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- N SUFFIX
PLASTIC PACKAGE
CASE 701 01
(TL495C ONLY)
 $R_{\theta JA} = 100^{\circ}\text{C/W (Typ)}$

SECTION 3 TV INTEGRATED CIRCUITS

Section 3—Packages



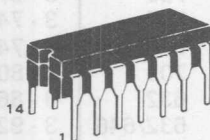
CASE 314A



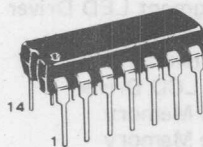
CASE 314B



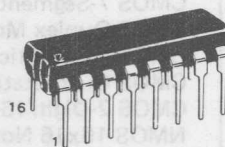
CASE 626



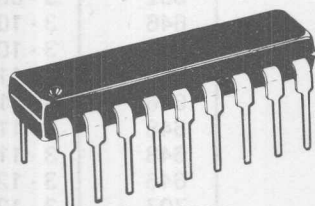
CASE 632 (TO116)



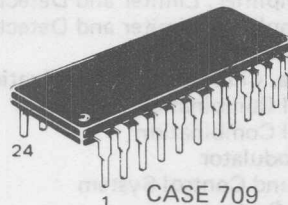
CASE 646 (TO116)



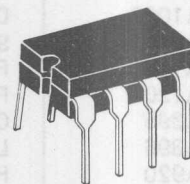
CASE 648



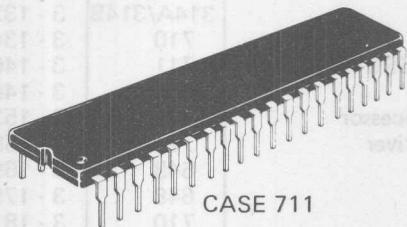
CASE 707



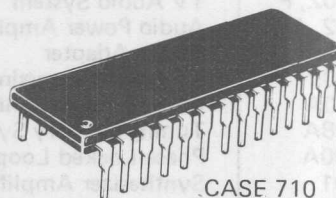
CASE 709



CASE 693



CASE 711



CASE 710



CASE 724



CASE 722A

TV INTEGRATED CIRCUITS

Device	Designation	Package	Page
MC1327A	Dual Doubly Balanced Chroma Demodulator	646	3 - 3
MC1374	TV Modulator Circuit	646	3 - 8
MC1391P	TV Horizontal Processor	626	3 - 12
MC2801P	Linear Control Chip for Frequency Synthesizer System	707	3 - 17
MC6200	TV Synthesizer Controller	711	3 - 21
MC6203	Remote Control Receiver	710	3 - 23
MC6215	Remote Control Receiver with On-screen Display	710	3 - 30
MC14426	Tuning Memory System, Memory	648	3 - 40
MC14429 P-B	Tuning Memory System, Control	707	3 - 43
MC14430	Input Address Encoder	648	3 - 47
MC14493	CMOS 7-Segment Decoder, Driver	648	3 - 51
MC14494	CMOS 7-Segment Decoder, Driver	648	3 - 51
MC14497P	CMOS PCM Remote Control Transmitter	707	3 - 55
MC14499	CMOS 7-Segment LED Display Decoder/Driver	707	3 - 61
MC144100	CMOS Duplex Mode 32-Segment LED Driver	709	3 - 67
MC144110	CMOS Hex Static D/A Converter	707	3 - 74
MC144111	CMOS Quad Static D/A Converter	646	3 - 74
MC144115	CMOS 2-Digit/16-Segment LCD Driver	709	3 - 80
MCM2801	NMOS 16x16 Non Volatile Memory	632	3 - 86
MCM2802	NMOS 32x32 Non Volatile Memory	632/646	3 - 92
MCM144102	CMOS 16-Bit/16-Word Static Ram	626	3 - 98
SAA1006	Diode Matrix Encoder	648	3 - 103
SMA2001	See MCM2801	632	3 - 86
TBA120C	FM/IF Amplifier, Limiter and Detector	646	3 - 105
TBA120D	FM/IF Amplifier, Limiter and Detector	646	3 - 105
TBA395	Chrominance Combination	646	3 - 110
TBA396	Luminance, Chrominance Combination	646	3 - 114
TBA920	Horizontal Combination	648	3 - 118
TBA920S	Horizontal Combination	648	3 - 118
TBA2110	FSK Demodulator	646	3 - 121
TCA5500	Stereo Sound Control System	707	3 - 124
TDA1190Z, P	TV Audio System	722A/648	3 - 128
TDA2002, A	Audio Power Amplifier	314A/314B	3 - 132
TDA3030	Secam Adapter	710	3 - 134
TDA3300B	TV Color Processing System, PAL/NTSC	711	3 - 140
TDA3950A	Chrominance Combination	646	3 - 148
UAA1008A	Tuning Memory System — Linear Processor	724	3 - 152
UAA2000A	Phase-Locked Loop Synthesizer & Driver	724	3 - 158
UAA2001	Synthesizer Amplifier & Driver	648	3 - 169
UAA2010	Synthesizer Amplifier & Driver	648	3 - 175
UAA2011	TV Time Base Processor	710	3 - 181
UAA2022	16-Bit LED Driver / or MPU Interface Circuit	724	3 - 182

MC1327A

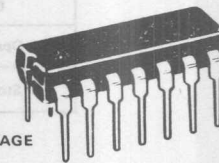
CHROMINANCE DEMODULATOR WITH RGB OUTPUT MATRIX AND PAL SWITCH

MONOLITHIC SILICON
INTEGRATED CIRCUIT

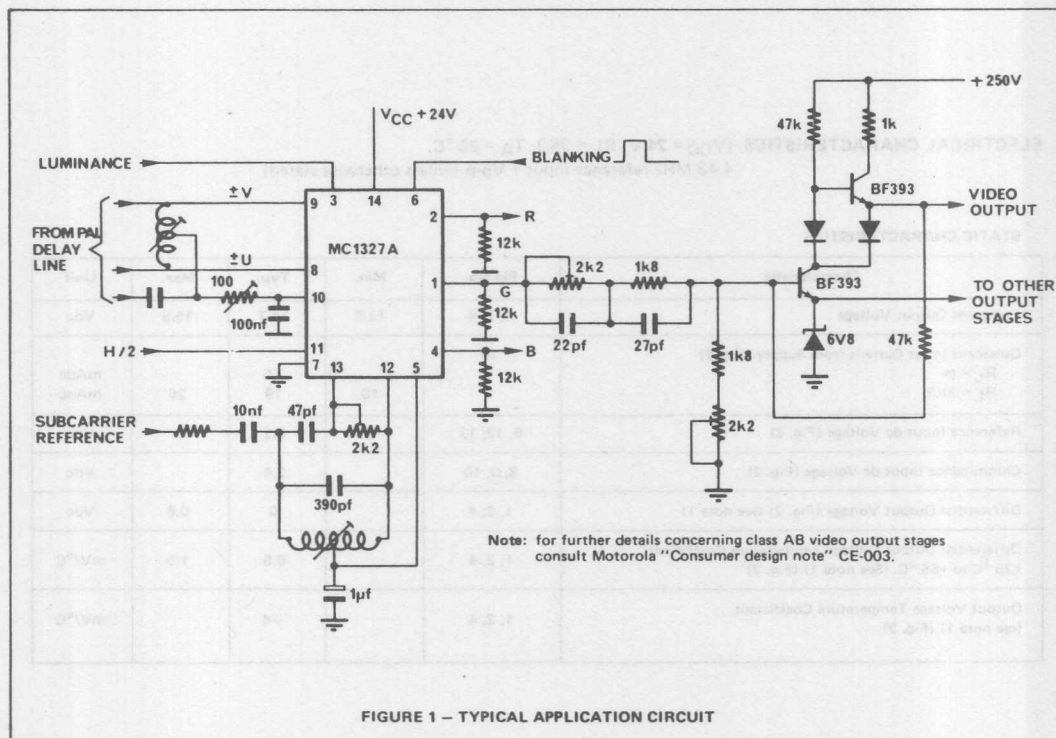
DUAL DOUBLE BALANCED CHROMINANCE DEMODULATOR WITH RGB MATRIX AND PAL SWITCH

... a monolithic device designed for use in PAL colour television decoders.

- Good chrominance sensitivity 0.22 V p-p Input typical for 5 V p-p Output
- Differential DC Temperature Stability 0.5 mV/°C typ.
- High B-Y Output Voltage Swing 10 V p-p
- Blanking Input Provided
- Luminance Bandwidth greater than 5 MHz.



P SUFFIX
PLASTIC PACKAGE
CASE 646



Note: for further details concerning class AB video output stages consult Motorola "Consumer design note" CE-003.

MC1327A

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chrominance Signal Input Voltage	5.0	VpK
Reference Signal Input Voltage	5.0	VpK
Minimum load resistance	3.0	K
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation Derate above 25°C	1000 8	mW mW/ $^\circ\text{C}$
Operating Temperature Range (Ambient)	-20 to $+75$	$^\circ\text{C}$
Storage Temperature Range	-65 to $+150$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24\text{ V}$, $R_L = 3\text{ K}\Omega$, $T_A = 25^\circ\text{C}$, 4.43 MHz reference input 1 Vp-p (unless otherwise stated)

STATIC CHARACTERISTICS

Characteristic	Pin No.	Min.	Typ.	Max.	Unit
Quiescent Output Voltage	1, 2, 4	13.2	14.7	15.8	Vdc
Quiescent Input Current from Supply (Fig. 2) $R_L = \infty$ $R_L = 3\text{ K}\Omega$	14		7.5 19		mAdc mAdc
Reference Input dc Voltage (Fig. 2)	5, 12, 13		6.2		Vdc
Chrominance Input dc Voltage (Fig. 2)	8, 9, 10		3.4		Vdc
Differential Output Voltage (Fig. 2) (see note 1)	1, 2, 4		0	0.6	Vdc
Differential Output Voltage Temperature Coefficient $+25^\circ\text{C}$ to $+65^\circ\text{C}$. (See note 1) (Fig. 2)	1, 2, 4		0.5	1.5	mV/ $^\circ\text{C}$
Output Voltage Temperature Coefficient (see note 1) (Fig. 2)	1, 2, 4		-4		mV/ $^\circ\text{C}$

DYNAMIC CHARACTERISTICS

Characteristic	Pin No.	Min.	Typ.	Max.	Unit
Blue Output Voltage Swing (see note 2) (Fig. 3)	4	8	10		Vp-p
Chrominance Input Voltage at Blue Output = Vp-p (see note 3) (Fig. 3)	8	150	220	350	mVp-p
Luminance Input Resistance	3	100			K Ω
Luminance Gain from pin 3 to Outputs @ dc @ 5.0 MHz referred to 100 KHz	1, 2, 4	0.95	-1.8		db
Differential Luminance Gain RGB Outputs at 5 MHz	1, 2, 4		0.3		db
Blanking Input Resistance (1 Vdc) (0 Vdc)	6		1.1 75		K Ω K Ω
Ratio of colour matrices (see note 3) (Fig. 3)					
B:R	4.2	1.50	1.78	1.96	
(no-b-y input) R:G	2.1	1.76	1.96	2.16	
(no r-y input) B:G	4.1	4.64	5.15	5.67	
PAL Switch Operating Voltage 7.8 KHz square wave	11	0.3			Vp-p
Red Output Offset with PAL switch Operation 7.8 KHz square wave	2			100	mVp-p
Demodulator Unbalance 4.43 MHz residual carrier (normal 4.43 MHz reference signal with no chrominance input)	1, 2, 4		100	200	mVp-p
Residual 4.43 MHz plus harmonics output voltage (with 4.43 MHz reference and chrominance input such that B out = 5 Vp-p	1, 2, 4		0.6	1.0	Vp-p
Reference input resistance chrominance input = 0	12, 13		2		K Ω
Reference input capacitance chrominance input = 0	12, 13		6		pF
Chrominance input resistance	8, 9, 10		2		K Ω
Chrominance input capacitance	8, 9, 10		2		pF

Note:

1. Chrominance input signal voltage = 0 and normal reference input voltage = 1 Vp-p 4.43 MHz.
2. With normal reference input signal voltage adjust chrominance input signal voltage to 1.2 Vp-p.
3. With normal reference signal voltage adjust chrominance input signal voltage until the blue output voltage = 5 Vp-p.



TEST CIRCUITS

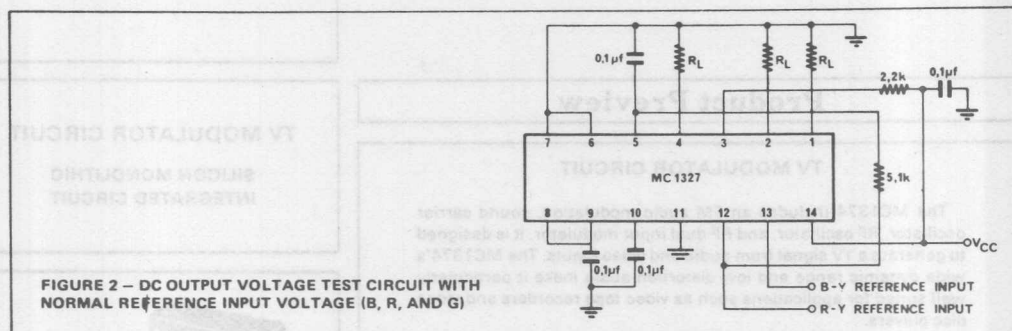


FIGURE 2 — DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

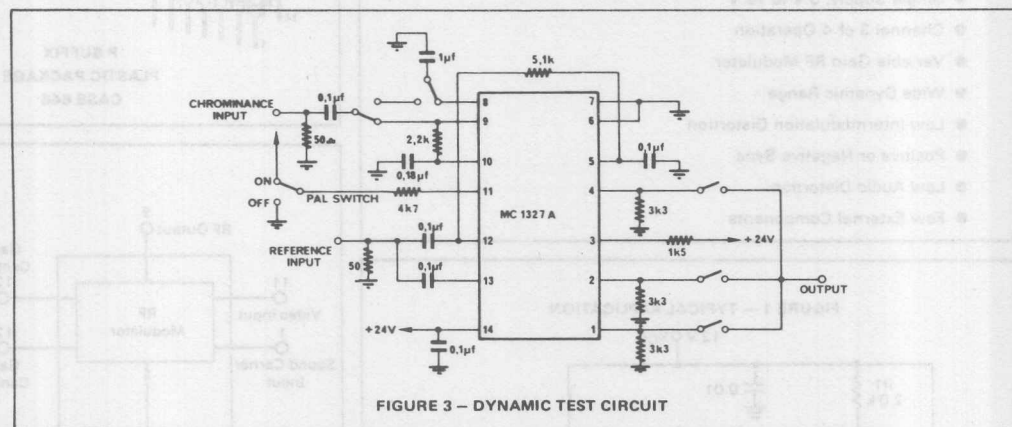
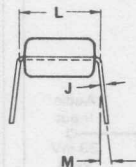
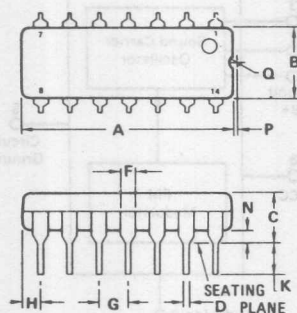


FIGURE 3 — DYNAMIC TEST CIRCUIT

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 646



NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MC1374 TARGET SPECIFICATIONS

Supply Voltage (Pin 8 and Pin 4)	12 V
Sync	Positive or Negative
Video Input Dynamic Range, (Max White to Sync Tips)	2.0 V
RF Output Voltage	15 mV RMS
Carrier Suppression	>40 dB
Linearity Over 30 dB Range	2%
920 kHz Beat	-60 dB
Sound Input for 16 kHz Deviation	<100 mV
4.5 MHz Oscillator Harmonics	-40 dB
Audio Distortion	<0.5%

TYPICAL APPLICATIONS

The RF oscillator in the MC1374 is similar to the oscillator in the MC1372 and the MC1373, and is coupled to the modulator in the same way.

The coil and capacitor connected between Pins 6 and 7 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 μ H shown in Figure 1 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz ($C = 75$ pF, $L = 0.1$ μ H). Resistors R2 and R3 are chosen to provide an adequate amplitude of switching voltage, whereas R1 is used to lower the maximum dc level of switching voltage below V_{CC} , thus preventing saturation within the IC.

For two-channel operation, one side of the tank may be ac grounded by moving C1 to Pin 6 or 7. A capacitor can then be switched in between the hot side of the tank and ground to tune the lower channel.

The video modulator is similar to the MC1496 balanced modulator, where input Pins 1 and 11 correspond to Pins 1 and 4 of the MC1496 and the modulator gain-setting Pins 12 and 13 correspond to Pins 2 and 3 of the MC1496. Only one pair of modulator collectors are brought out on Pin 9. The other pair are returned to V_{CC} .

The dc levels on Pins 1 and 11 are externally determined. The limits of dc plus video are between 2.5 and 1.5 volts below the dc voltage on Pins 6 and 7. This will prevent saturation of any of the modulator transistors.

In a typical application where the composite video information is dc coupled to Pin 11, the bias on Pin 1 is set to give the desired modulation characteristic. The Pin 1 bias may be set either below max white level for positive sync, or above max white for negative sync. As shown in Figure 2 and 3, minimum carrier occurs when the voltage on Pins 1 and 11 are equal.

The gain-setting resistor, R8, between Pins 12 and 13, is picked to give the proper modulation depth for the available composite video amplitude.

The modulated RF signal is presented as a current at the RF output, Pin 9. Since this pin represents a current source, any load impedance may be selected for matching purposes and gain selections as long as the voltage on Pin 9 is high enough to prevent the output devices from reaching saturation. Lowering the dc voltage on Pins 6 and 7 gives increased RF output capability at the expense of video input range.

The sound carrier oscillator and audio modulator have internally set bias. A separate B+ is supplied to the oscillator, via Pin 4, so the oscillation may be easily disabled while tuning the RF tank. The sound carrier frequency is determined by L2 and C3. The oscillator feedback is fed to L2 through dc blocking capacitor C5, and 4.5 MHz appears at the input to the oscillator, Pin 3.

The sound carrier is coupled to the modulator input, Pin 1. R6 is chosen to give the desired sound carrier amplitude.

The value depends upon the Q of L2, R4 and R5 values, and the RF modulator gain as set by R8.

Baseband audio is fed to the audio modulator on Pin 14. The audio directly modulates the sound carrier oscillator for a flat characteristic and very low distortion. The input impedance on Pin 14 is nominally 6.0 k Ω . If the audio available is much greater than necessary for proper deviation, a series resistor can be added to allow a low value for C6.

Where the application calls for tight frequency stability, the sound carrier oscillator may be frequency controlled by supplying a dc current to Pin 14 from a suitable AFC circuit. The nominal voltage at Pin 14 is four diode drops above ground, or approximately 3.0 volts. Supplying current to Pin 14 increases the frequency, and pulling current out of Pin 14 reduces it.

MC1374 TARGET SPECIFICATIONS

FIGURE 2

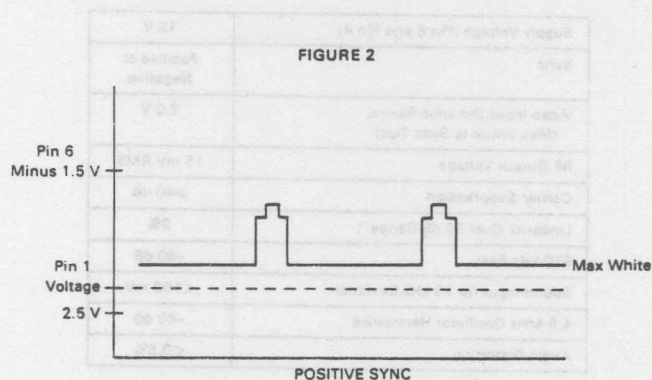
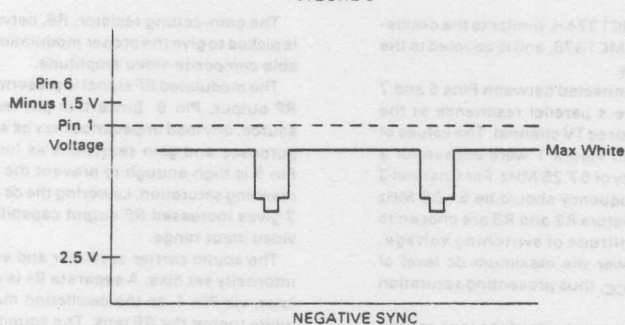


FIGURE 3



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_D(T_A) = \frac{T_J(\max) - T_A}{R_{\theta JA}(\text{typ})}$$

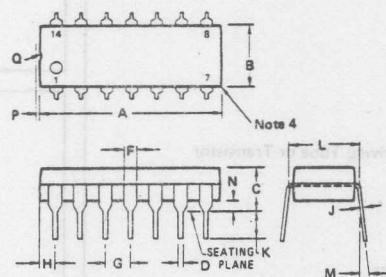
where $P_D(T_A)$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_J(\max)$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(\text{typ})$ = Typical Thermal Resistance Junction to Ambient

OUTLINE DIMENSIONS



NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

CASE 646-05
P SUFFIX
PLASTIC PACKAGE

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1391P	0°C to +75°C	Plastic DIP
MC1394P	0°C to +75°C	Plastic DIP

MC1391P

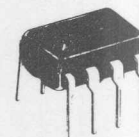
TV HORIZONTAL PROCESSOR

... low-level horizontal sections including phase detector, oscillator and pre-driver — a device designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ± 300 Hz Typical Pull-In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable dc Loop Gain
- MC1391P — Positive Flyback Inputs
- MC1394P — Negative Flyback Inputs

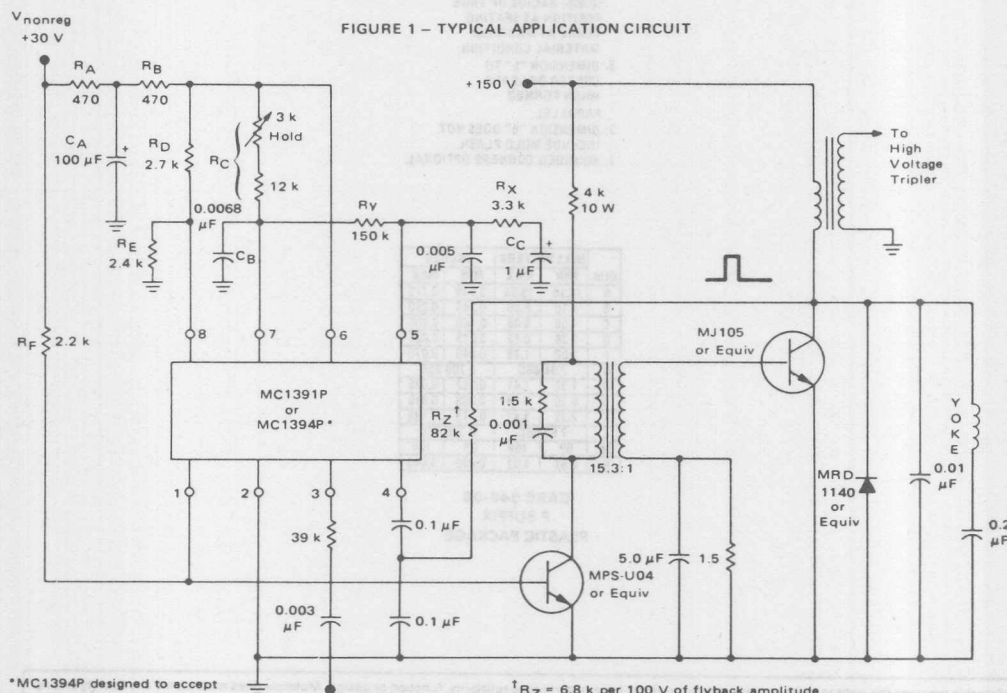
TV HORIZONTAL PROCESSOR

MONOLITHIC SILICON
INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

FIGURE 1 — TYPICAL APPLICATION CIRCUIT



*MC1394P designed to accept reverse polarity sawtooth at Pin 4 if sync pulse not derived from MJ105 collector.

-20 V Sync

This circuit has an oscillator pull-in range of ± 300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mA _{dc}
Output Voltage	40	V _{dc}
Output Current	30	mA _{dc}
Sync Input Voltage (Pin 3)	5.0	V _(p-p)
Flyback Input Voltage (Pin 4)	5.0	V _(p-p)
Power Dissipation (Package Limitation)		
Plastic Package	625	mW
Derate above $T_A = +25^\circ\text{C}$	5.0	mW/ $^\circ\text{C}$
Operating Temperature Range (Ambient)	0 to +75	$^\circ\text{C}$
Storage Temperature Range	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.) (See Test Circuit of Figure 2, all switches in position 1.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.6	9.0	V _{dc}
Supply Current (Pin 6)	—	20	—	mA _{dc}
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Figure 6)				V _{dc}
($I_C = 20\text{ mA}$, Pin 1) V _{dc}	—	0.15	0.25	
Voltage (Pin 4)	—	2.0	—	V _{dc}
Oscillator Pull-in Range (Adjust R_H in Figure 2)	—	± 300	—	Hz
Oscillator Hold-in Range (Adjust R_H in Figure 2)	—	± 900	—	Hz
Static Phase Error ($\Delta f = 300\text{ Hz}$)	—	0.5	—	μs
Free-running Frequency Supply Dependence (S1 in position 2)	—	± 3.0	—	Hz/V _{dc}
Phase Detector Leakage (Pin 5)	—	—	± 1.0	μA
Sync Input Voltage (Pin 3)	2.0	—	5.0	V _(p-p)
Sawtooth Input Voltage (Pin 4)	1.0	—	3.0	V _(p-p)

TYPICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$ unless otherwise noted.)

FIGURE 2 - TEST CIRCUIT

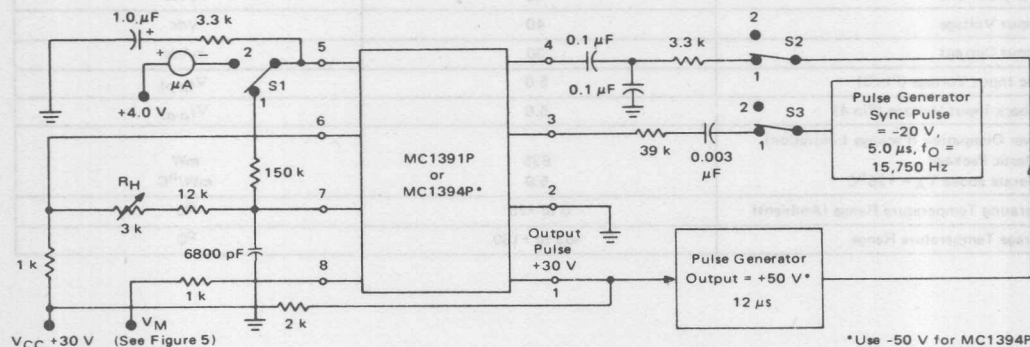


FIGURE 3 - FREQUENCY versus TEMPERATURE

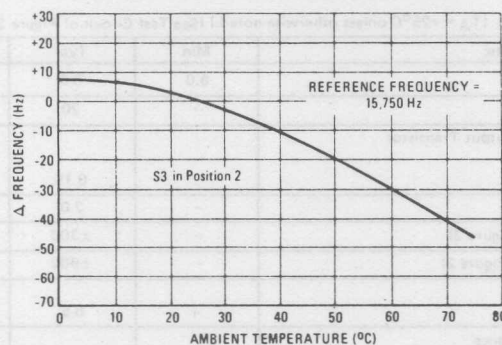


FIGURE 4 - FREQUENCY DRIFT versus WARM-UP TIME

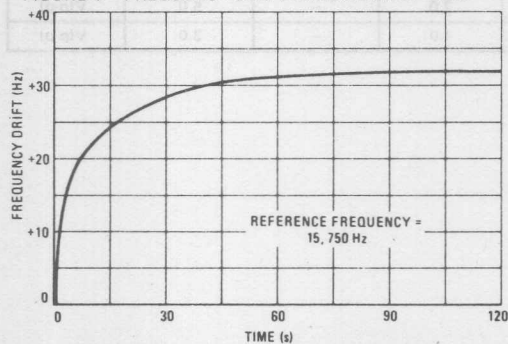


FIGURE 5 - MARK-SPACE RATIO

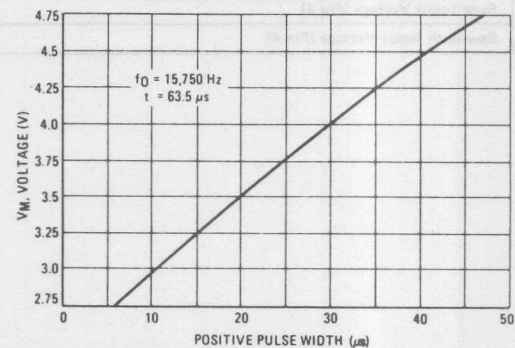
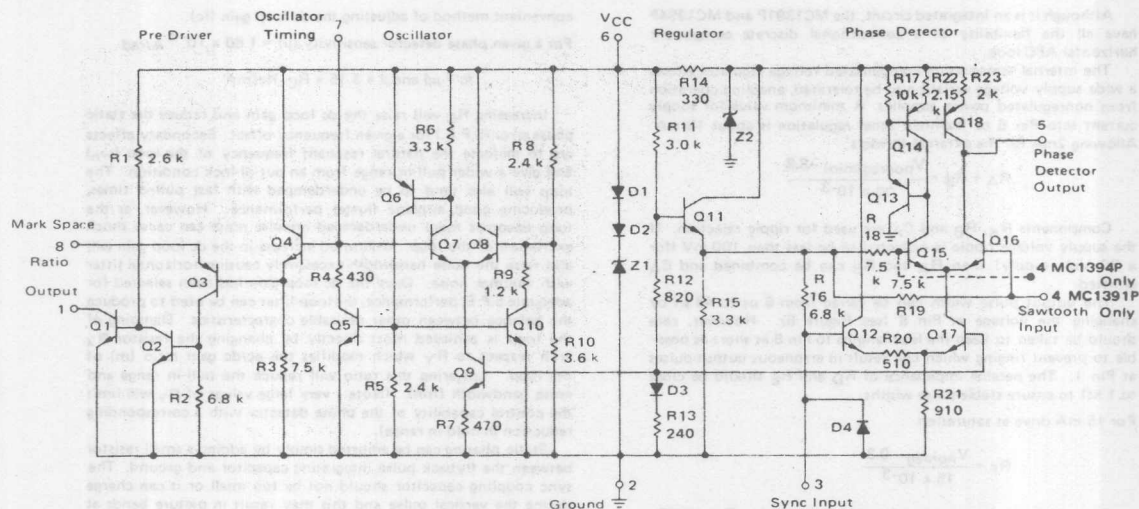


FIGURE 6 - CIRCUIT SCHEMATIC



CIRCUIT OPERATION

The MC1391P and MC1394P contain the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. Then, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either

tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each for half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low-pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P and MC1394P have all the flexibility of a conventional discrete component horizontal APC loop.

The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2mA for the external dividers

$$R_A + R_B = \frac{V_{\text{nonreg(min)}} - 8.8}{20 \times 10^{-3}}$$

Components R_A , R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 Volt supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6 μ s to 48 μ s by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible to prevent ringing which can result in erroneous output pulses at Pin 1. The parallel impedance of R_D and R_E should be close to 1 k Ω to ensure stable pulse widths.

For 15 mA drive at saturation

$$R_F = \frac{V_{\text{nonreg}} - 0.3}{15 \times 10^{-3}}$$

The oscillator free-running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \gg R_{\text{discharge}}$ (R_4 in Figure 6), a useful approximation for the free-running frequency is

$$f_0 = \frac{1}{0.6 R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies — operation at 31.5 kHz for count-down circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free-running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator (β) to control-current from the phase detector is directly dependent on the magnitude of R_C , and this provides a

convenient method of adjusting the dc loop gain (f_c).

For a given phase detector sensitivity (μ) = 1.60×10^{-4} A/rad

$$f_c = \mu \beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing R_C will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull-in range from an out-of-lock condition. The loop will also tend to be underdamped with fast pull-in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate S.P.E. performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the ac/dc gain ratio (m) of the loop. Lowering this ratio will reduce the pull-in range and noise bandwidth (f_{nn}). (Note: very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold-in range).

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

NOTE:

In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 + \chi^2 T \omega_c}{4 \chi T}$$

$$\chi = \frac{R_X}{R_Y}$$

$$\omega_n = \sqrt{\frac{\omega_c}{(1 + \chi) T}}$$

$$\omega_c = 2 \pi f_c$$

$$T = R_Y C_C$$

$$K = \frac{\chi^2 T \omega_c}{4}$$

where:

K = loop damping coefficient

MC2801P

Advance Information

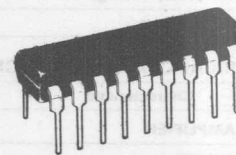
CONTROL CHIP FOR TV FREQUENCY SYNTHESIZER SYSTEM

This linear control chip provides all the necessary interface between an NMOS PLL frequency synthesizer chip and a varicap diode tuner.

- 5-Volt Series Regulator to Support the NMOS LSI and Other Circuits
- 35-Volt Shunt Regulator for Varicap Driver Circuit
- Filter Amplifier to Form Active Filter for PLL Circuit
- Band Decoder to Switch for 3-Band Tuner
- Video Coincidence Circuit to Detect TV Station

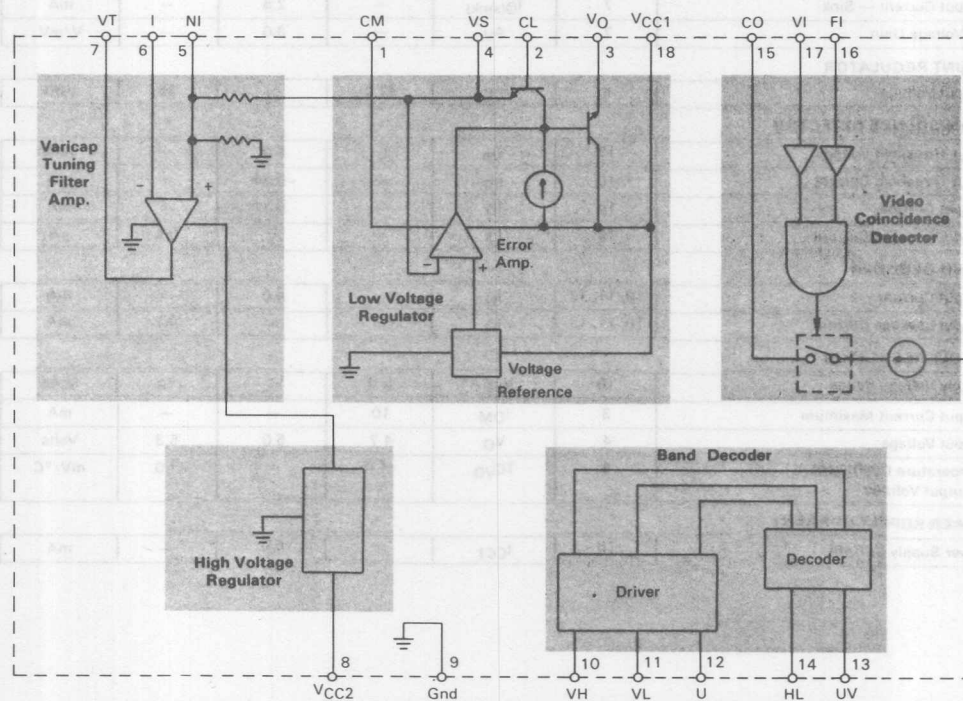
LINEAR CONTROL CHIP FOR TV FREQUENCY SYNTHESIZER SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 707

FIGURE 1 — BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

ADI-580

9168304

CONTROL CHIP FOR TV FREQUENCY

[illegible]

Video Conferencing Circuit to Detect TV Station

—	2.0	—	k Ω
1.20	1.35	1.50	Volts
—	—	2.0	μ A
30	—	—	Volts
—	—	0.5	Volts
—	2.5	—	mA
—	3.0	—	V/mV

[illegible]

22.5		22	14.1
------	--	----	------

32.5	—	38	Volts
------	---	----	-------

—	5.0	—	Volts
—	-0.24	—	mA
—	0.1	—	mA
		0.5	°

	—	—	0.5	μA
--	---	---	-----	---------

—	5.0	—	mA
—	—	0.1	mA

			0.1	III A
--	--	--	-----	-------

9.0	—	15	Volts
10	—	—	mA
4.7	5.0	5.3	Volts
-1.0	—	1.0	mV/°C

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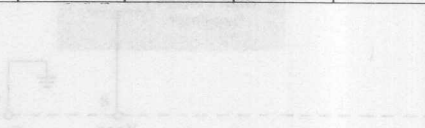
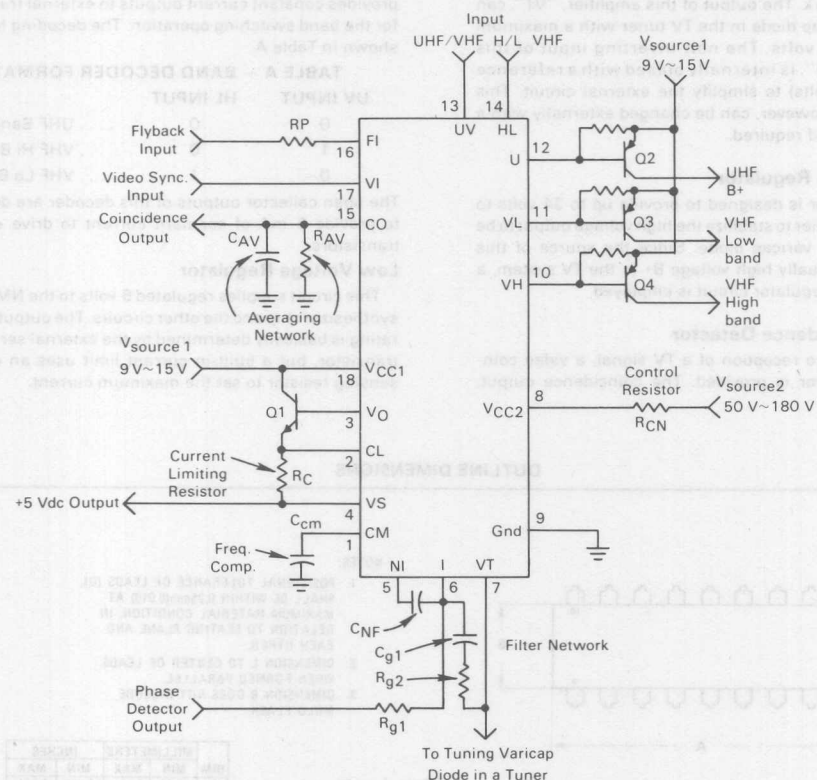


FIGURE 2 — EXTERNAL CONFIGURATION



- Rp — Protection resistor for flyback input
- RAV and CAV — Integrator in the video coincidence circuit
- Q1 — Series pass transistor for the 5 V regulator
- Rc — Sensing resistor for the current limiter
- Ccm — Phase compensation capacitor for the 5 V regulator
- Rg1, Rg2, Cg1 — Filter time constant
- Cnf — Capacitor to improve noise characteristics
- RCN — Control resistor for the high voltage shunt regulator
- Q2, Q3, Q4 — Drivers for the band switch

CIRCUIT DESCRIPTION

This linear control chip is designed to integrate all the control circuits and regulators required in this system on a single chip to minimize the external components.

Filter Amplifier Section

This amplifier is designed to provide an active filter in the PLL network. The output of this amplifier, "VT", can drive the varicap diode in the TV tuner with a maximum voltage of 30 volts. The non-inverting input of this amplifier, "NI", is internally biased with a reference voltage (1.3 volts) to simplify the external circuit. This bias voltage, however, can be changed externally with a single resistor if required.

High Voltage Regulator

The regulator is designed to provide up to 34 volts to the filter amplifier to stabilize the high voltage output to be applied to the varicap diode. Since the source of this regulator is usually high voltage B+ in the TV system, a simple shunt regulator circuit is employed.

Video Coincidence Detector

To assure the reception of a TV signal, a video coincidence detector is provided. The coincidence output,

"CO", of the circuit will go high when the video synchronous signal (video input "VI") and the flyback pulse (flyback input "FI") are synchronous.

Band Decoder

This circuit decodes band-select information and provides constant current outputs to external transistors for the band switching operation. The decoding format is shown in Table A.

TABLE A — BAND DECODER FORMAT

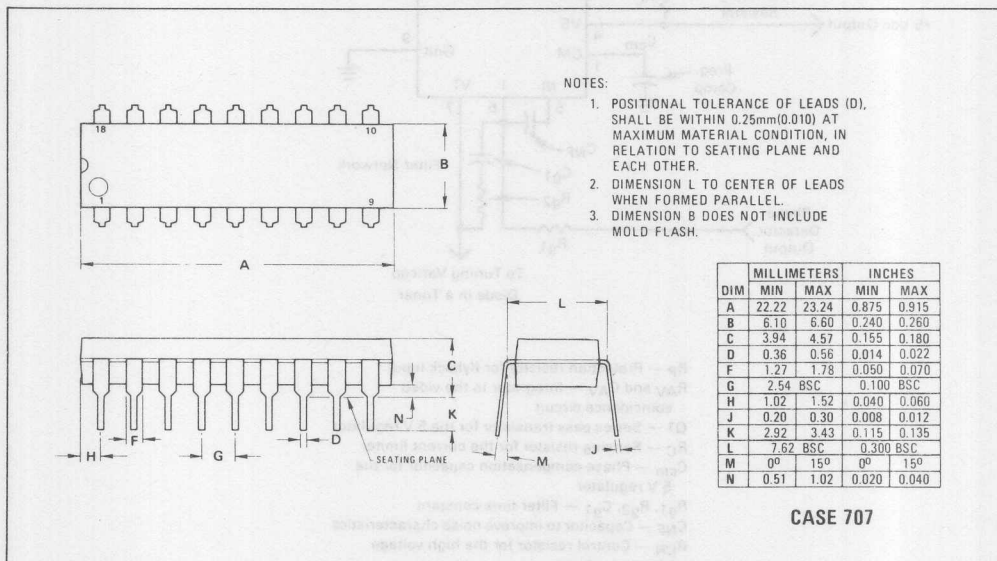
UV INPUT	HL INPUT	
0	0	... UHF Band
1	0	... VHF Hi Band
0	1	... VHF Lo Band

The open collector outputs of this decoder are designed to provide 5 mA of constant current to drive external transistors.

Low Voltage Regulator

This circuit supplies regulated 5 volts to the NMOS PLL synthesizer chip and the other circuits. The output current rating is basically determined by the external series pass transistor, but a built-in current limit uses an external sensing resistor to set the maximum current.

OUTLINE DIMENSIONS



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MC 6200

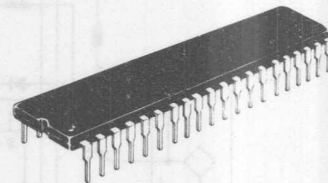
Product Preview

TV SYNTHESIZER CONTROLLER

- Controls 4 peripherals via serial bus :
 - UAA 2000 Synthesizer circuit
 - MC 144102 or SMA 2001 memory circuits
 - MC 14499 LED Driver
 - MC 6215 On-Screen Display
- Up to 30 program standby memory capability
- 100 CCIR channel look up table ROM
- Direct selection of channel or program number
- Both remote and local keyboard control
- Power failure and false entry protection
- Automatic search at 4 channel/sec
- Mute output with 50 ms lead time
- Fine tune at 5 Hz rate and ± 4 MHz max offset (125 KHz resolution)
- Channel and program display control
- Automatic standby switching

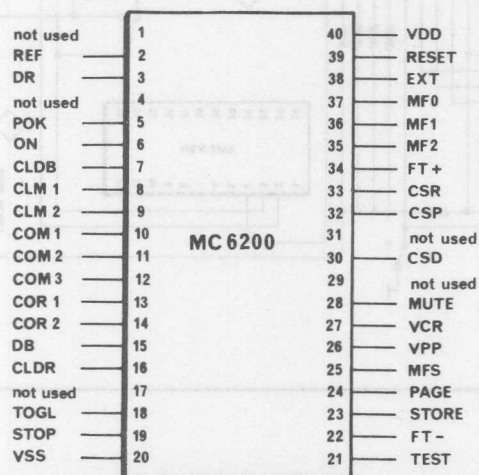
SINGLE-CHIP MICROCONTROLLER

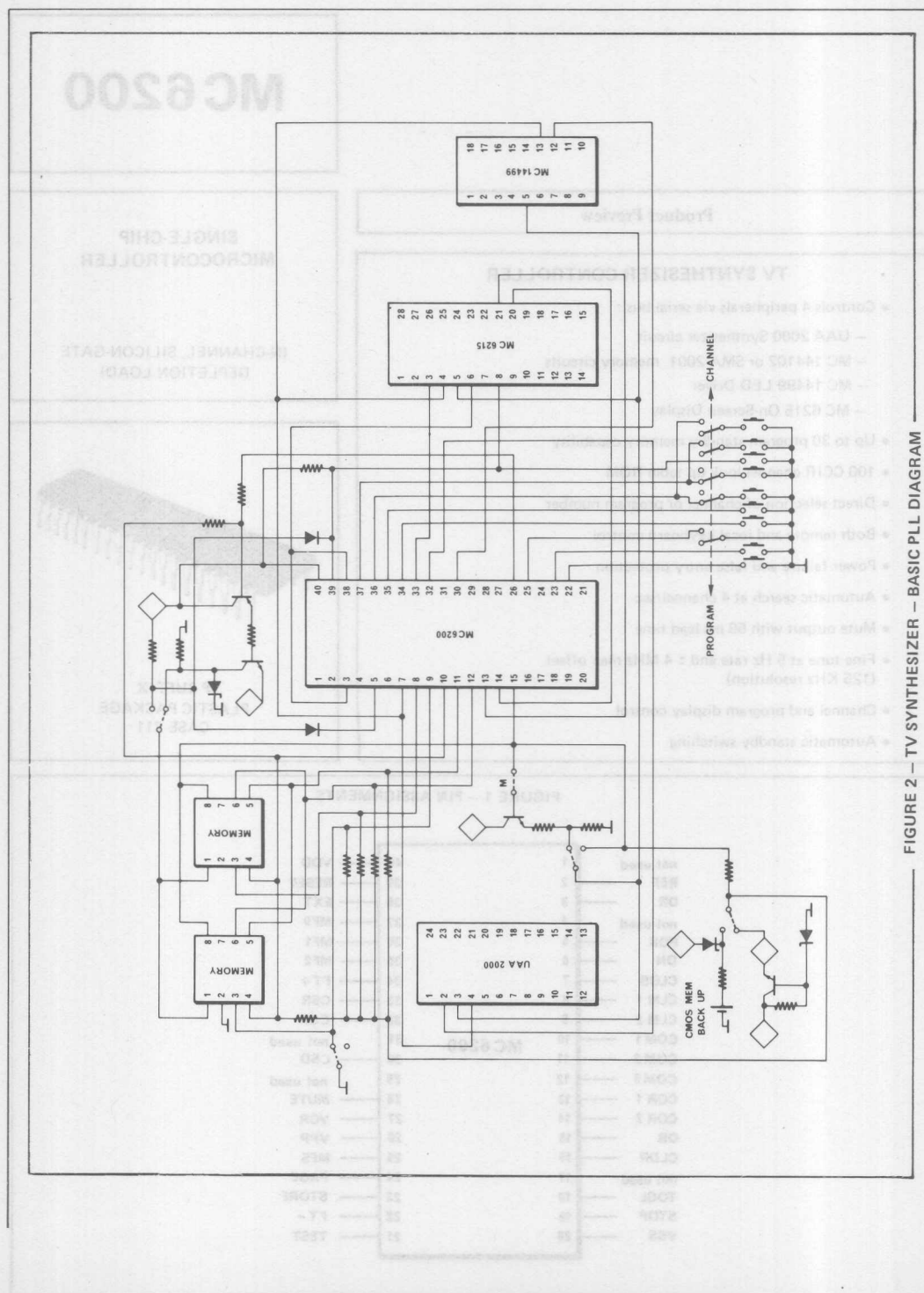
(N-CHANNEL, SILICON-GATE DEPLETION LOAD)



P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1 -- PIN ASSIGNMENTS



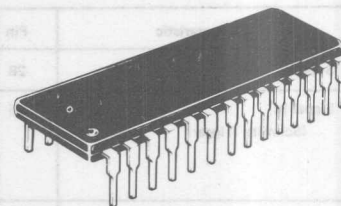


MC 6203

MOS

(N-CHANNEL, SILICON-GATE)

REMOTE CONTROL RECEIVER



PLASTIC PACKAGE
CASE 710-01

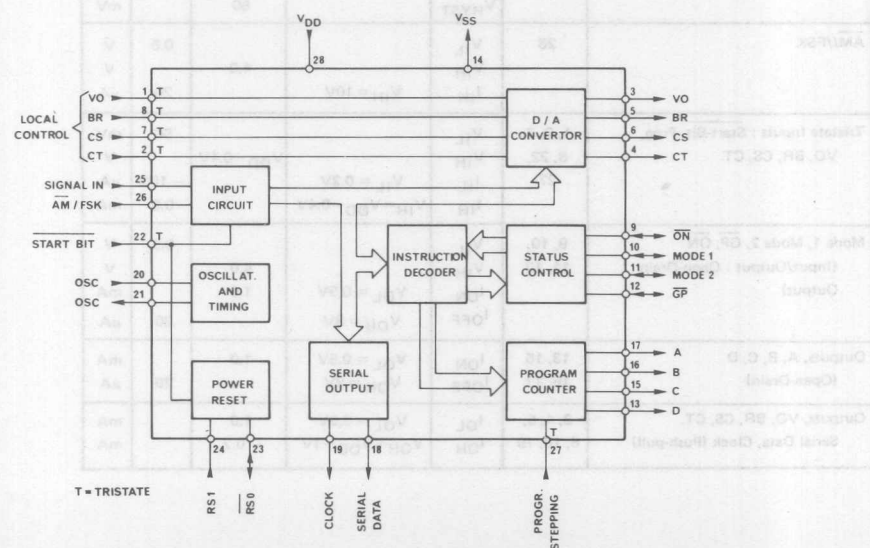
Advance Information

REMOTE CONTROL RECEIVER

The MC 6203 is a PCM remote control receiver realised in NMOS silicon gate technology. It is a comprehensive receiver offering a large number of integrated functions for the full control of TV or Hi-Fi systems. The receiver is designed to be used in conjunction with the MC 14497 transmitter.

- 62 channels over 500 functions
- 3 modes of operation
- AM/FSK pin option
- Start-bit pin option
- 4 analogue functions
- Direct local increment/decrement of analogue functions and TV programmes
- 16 programme parallel output
- Serial data bus output
- 455kHz reference oscillator
- Direct teletext interface

FIGURE 1 — MC 6203 BLOCK DIAGRAM AND PIN ASSIGNMENT



MC6203

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{DD}	-0.3 to 8	Vdc
Input Voltage, pins 8 - 13, 15 - 17, 25 all other pins	V_{in}	0 to 16 0 to 10	Vdc
Operating Temperature Range	T_A	0 to 70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to 150	$^\circ\text{C}$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ELECTRICAL CHARACTERISTICS ($V_{DD} = 5V \pm 0.5V$, $T_A = 0$ to 70°C)

Characteristic	Pin	Symbol	Condition	Min	Max	Unit
Supply Current	28	I_{DD}			50	mA
Signal In (Schmitt Trigger)	25	V_{IL} V_{IH} V_{HYST} I_{IH}	Hysteresis $V_{IH} = 16V$	3.2 50	1.2 20	V V mV μA
RS1	24	V_{IL} V_{IH} V_{HYST} I_{IL}	$V_{IL} = 100\text{mV}$	400 50	50	mV mV mV μA
RS0 (Push-pull Output) (Schmitt Trigger input)	23	I_{OL} I_{OH} V_{IL} V_{IH} V_{HYST}	$V_{OL} = 0.5V$ $V_{OH} = V_{DD} - 1V$	100 -5 400 50	-100 50	μA μA mV mV mV
AM//FSK	26	V_{IL} V_{IH} I_{IH}	$V_{IH} = 10V$	4.0	0.5 20	V V μA
Tristate Inputs : Start-Bit, Prog, VO, BR, CS, CT	1, 2, 7, 8, 22, 27	V_{IL} V_{IH} I_{IL} I_{IH}	$V_{IL} = 0.2V$ $V_{IH} = V_{DD} - 0.4V$	$V_{DD} - 0.4V$	50 -100 0.5	mV V μA mA
Mode 1, Mode 2, \overline{GP} , \overline{ON} (Input/Output : Open-Drain Output)	9, 10, 11, 12	V_{IL} V_{IH} I_{ON} I_{OFF}	$V_{OL} = 0.5V$ $V_{OH} = 8V$	4.0 1.0	0.5	V V mA μA
Outputs, A, B, C, D (Open-Drain)	13, 15 16, 17	I_{ON} I_{OFF}	$V_{OL} = 0.5V$ $V_{OH} = 8V$	1.0	20	mA mA
Outputs, VO, BR, CS, CT, Serial Data, Clock (Push-pull)	3, 4, 5, 6, 18, 19	I_{OL} I_{OH}	$V_{OL} = 0.5V$ $V_{OH} = V_{DD} - 1V$	1.0 -0.2		mA mA

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Pin	Symbol	Condition	Min	Max	Unit
Osc Input	20	I_{IL}	$V_{IL} = 0V$	-1.0	50	μA
		I_{IH}	$V_{IH} = V_{DD}$	1.0	50	μA
Osc Output	21	I_{OL}	$V_{OL} = 0.5V$, $V_{OH} = 4V$	300		μA
		I_{OH}	$V_{OH} = V_{DD} - 1V$, $V_{OL} = 0V$	-50		μA

CIRCUIT OPERATION

The MC 6203 is an integrated circuit PCM remote control receiver designed to receive bi-phase coded PCM transmissions. The receiver is able to receive 62 channels in any of three modes and reception may, optionally, be AM or FSK. There is also a pin option which permits the receiver to recognise two start-bit polarities.

The transmitted information is in the form of a 7-bit word, see figure 4 for format, a start bit and 6 information bits. On reception of a signal the receiver performs a series of tests to achieve the necessary noise immunity and check the validity of the signal:

- The bi-phase code is checked to ensure that there is only one edge during any one time window.
- The word length is checked for the presence of 7 bits.
- The noise level is checked.

The latter test is carried out only in the AM mode.

After reception of an apparently valid word the receiver waits for some 3ms to verify the presence of noise or other transients. Should these be present the word is rejected and not decoded. Should the word, on the other hand, be found to be valid it is moved into a latch, by the signal TRF (see figure 3) and decoded. At the same time it is released on the serial data bus.

The end of transmission is notified by the reception of the "End of Transmission" code, channel 62. In the case of the MC 14497 transmitter this is transmitted automatically when any button is released. This word, too, is available on the serial data bus. In the eventuality of the transmission being interrupted for more than 570ms an internal timer will automatically generate the "End of Transmission" code which will be processed in the normal manner.

While only channels 0 to 31 and 62 are recognised by the internal instruction decoder, all 63 commands are available on the serial data bus; in the TV mode whatever is received at the Signal In pin will be repeated on the bus. In any other mode, i.e. when pins Mode 1 and/or Mode 2 are high the clock line will be disabled after the first signal has been released. The line will be enabled again after receiving an end-of-transmission code (channel 62) or when the time-out counter has timed out.

When power is applied to the circuit the reset circuitry sets up the initial position: $ON = 1$ (standby), Mode 1 and 2 = 0 (TV), $QT = \text{reset}$ and the D/A Converters are at Mid. Depending on the external components the power reset can be either dynamic, using pin RS1 as shown in figure 5, or static using pin RS0.

INPUT/OUTPUT FUNCTIONS

AM/FSK — By means of a suitable voltage level at pin 26 the receiver will decode AM or FSK modulated signals.

AM MODE — In the AM mode, when pin 26 = 0, the receiver is capable of decoding a modulated or demodulated signal, in this mode the SIGNAL IN pin, pin 25, must be high, = 1. When receiving a modulated signal the pulse duration must be at least 4.5µs with a repetition period of at least 70µs if the signal is to be accepted.

FSK MODE — In the FSK mode, when pin 26 = 1, the receiver will only accept a demodulated input signal, at the same time the quiescent level of pin 25 is arbitrary.

ANALOGUE CONTROLS — On reception of the code word for one of the four analogue functions the digital/analogue convertor in the receiver generates an analogue voltage, normally used to control the volume (VO), brightness (BR), colour saturation (CS) or contrast (CT) of a colour TV. The control voltages are obtained by direct RC integration of a variable duty cycle square wave output from the D/A convertor. The total sweep time of the overflow/underflow protected D/A convertor is 6s; derived from a repetition rate of 7.1kHz and a D/A convertor resolution of 60 steps. Operation of the analogue controls is inhibited in the STANDBY mode.

Local control of the four analogue functions is possible by use of the four tristate inputs, pins 1, 2, 7 and 8. For each of these inputs pulling the input high increments the function and vice-versa. The third state will leave control to the remote function. In all cases local control will override remote control.

MID — (Middle Position) This presets all the analogue functions to 50%, with the exception of VO which is set to 33%. It is operative under the following conditions:

- When switching from OFF to ON
- When MID, channel 0, is selected.

MUTE (QT) — This is an internal latch, which when set mutes the sound by pulling the VO line low, = 0. It is a toggle function controlled by channel 1, QT. The mute is applied during a programme change. QT is reset by:

- Channel 0, MID
- Channel 2, STANDBY
- Channel 4/6 Programme +/-
- Channel 8, VO +
- Channels 16 to 31, the programme channels
- Channels 5 and 7, mode changes
- Channel 1, QT

PROGRAMME SELECTION — In order to be able to select up to 16 programme channels a 4-bit binary up/down counter, the program counter, is included on-

chip with its associated outputs A, B, C and D plus the PROG. STEPPING input.

Programme selection is possible by the selection of channels 16 to 31, or the programme channel can be changed by incrementing/decrementing the programme counter remotely, by use of Programme + / Programme -, or by use of the PROG. STEPPING input. Pulling this tristate pin, 27, low will decrement the programme while forcing it high will increment the programme. In its tristate position there is no change and control is a remote function.

SERIAL DATA BUS — The serial data bus releases into the system words which have been received and recognised as valid, thus they will conform to the remote control code and sequence. The format of the serial output data (DATA) and clock (CLOCK) are shown in figure 3.

In the TV mode whatever is received at the SIGNAL IN pin, 25, will be repeated on the serial data bus. However, in any other mode, i.e. when pins MODE 1 and/or MODE 2 = 1, the clock line, CLOCK, will be disabled after the first signal has been released. The line will be enabled again after receiving an end-of-transmission code, channel 62, or when the time-out counter has timed out.

GP — This function, pin 12, is a general purpose toggle function which can be set and reset by calling channel 3. It is also reset by calling channel 2, STANDBY.

MODES OF OPERATION — Four operational modes, or functions, are available which, although their application is unlimited, are identified as shown below:

Function	Pin		
	ON	Mode 1	Mode 2
1* Standby	1	X	X
2* TV	0	0	0
3* Teletext	0	1	0
4* Reserve	0	0	1

X = don't care

* refers to the function number with figure 2

MODE SELECTION

STANDBY — Selected by channel 2, STANDBY. At this time pin 9, ON, is high.

TV — This is the prime active mode and is selected by channel 6, 4 or any programme channel, 16 to 31.

TELETEXT — Selected by channel 5, MODE 1, at this time the MODE 1 pin, 10, will be high. As channel 5 is a toggle function, reselection of this channel will return the receiver to the TV mode.

INPUT/OUTPUT FUNCTIONS (continued)

RESERVE — Selected by channel 7, MODE 2, which will cause pin 11, MODE 2, to go high. This channel, too, is a toggle function and recalling channel 7 will restore the receiver to the TV mode.

A further mode of operation is available, by locally forcing both MODE 1 and MODE 2 = 1. However, this function is not available remotely.

As can be seen the mode selection is a typewriter-like shifted key function. The differences between the modes can be summarised as follows :

TV — All instructions can be used. All data are available on the serial data bus.

Teletext — All analogue functions, plus MID and MUTE are available. Remote programme change is not possible, but they can be locally incremented/decremented by use of pin 27, PROG. STEPPING.

Reserve — All analogue functions are inhibited, although the sound is muted when incrementing/decrementing the programme counter. All remote programme changes are inhibited, but the programme counter may be locally incremented/decremented by use of PROG. STEPPING.

START BIT — The MC 6203 recognises two start-bit polarities, high and low. The start-bit pin, 22, is a tristate input which in its high state, = 1, primes the receiver to recognise a test function. When pin 22 = 0 the receiver will recognise a high start-bit and when the pin is tristate, i.e. floating, the receiver will recognise a low start-bit.

FIGURE 2 — TABLE OF INSTRUCTIONS

Ch	Command	Function 1* 2* 3* 4*	Code Word F E D C B A	Ch	Word F E D C B A
0	MID/QT reset	— X X —	0 0 0 0 0 0	32	1 0 0 0 0 0
1	MUTE (QT)	— X X —	0 0 1	33	1 0 0 0 0 1
2	Standby/QT reset	X X X X	0 1 0	34	1 0 0 0 1 0
3	Clock (CLK) GP	— X — —	0 1 1	35	1 0 0 0 1 1
4	Programme +/-ON/QT reset	X X — —	1 0 0	36	1 0 0 1 0 0
5	Mode 1/ON/QT reset	— X X X	1 0 1	37	1 0 0 1 0 1
6	ON/QT reset/programme —	X X — —	1 1 0	38	1 0 0 1 1 0
7	Mode 2/ON/QT reset	— X X X	1 1 1	39	1 0 0 1 1 1
8	Volume +/-QT reset	— X X —	0 0 1 0 0 0	40	1 0 1 0 0 0
9	Volume —	— X X —	0 0 1	41	1 0 1 0 0 1
10	Brightness +	— X X —	0 1 0	42	1 0 1 0 1 0
11	Brightness —	— X X —	0 1 1	43	1 0 1 0 1 1
12	Colour saturation +	— X X —	1 0 0	44	1 0 1 1 0 0
13	Colour saturation —	— X X —	1 0 1	45	1 0 1 1 0 1
14	Contrast +	— X X —	1 1 0	46	1 0 1 1 1 0
15	Contrast —	— X X —	1 1 1	47	1 0 1 1 1 1
16	ON/QT reset/programme preset	X X — —	0 1 0 0 0 0	48	1 1 0 0 0 0
17	ON/QT reset/programme preset	X X — —	0 0 1	49	1 1 0 0 0 1
18	ON/QT reset/programme preset	X X — —	0 1 0	50	1 1 0 0 1 0
19	ON/QT reset/programme preset	X X — —	0 1 1	51	1 1 0 0 1 1
20	ON/QT reset/programme preset	X X — —	1 0 0	52	1 1 0 1 0 0
21	ON/QT reset/programme preset	X X — —	1 0 1	53	1 1 0 1 0 1
22	ON/QT reset/programme preset	X X — —	1 1 0	54	1 1 0 1 1 0
23	ON/QT reset/programme preset	X X — —	1 1 1	55	1 1 0 1 1 1
24	ON/QT reset/programme preset	X X — —	0 1 1 0 0 0	56	1 1 1 0 0 0
25	ON/QT reset/programme preset	X X — —	0 0 1	57	1 1 1 0 0 1
26	ON/QT reset/programme preset	X X — —	0 1 0	58	1 1 1 0 1 0
27	ON/QT reset/programme preset	X X — —	0 1 1	59	1 1 1 0 1 1
28	ON/QT reset/programme preset	X X — —	1 0 0	60	1 1 1 1 0 0
29	ON/QT reset/programme preset	X X — —	1 0 1	61	1 1 1 1 0 1
30	ON/QT reset/programme preset	X X — —	1 1 0	62	1 1 1 1 1 0 (EOT)
31	ON/QT reset/programme preset	X X — —	0 1 1 1 1 1		

X = commands available within each functional mode
* refers to the table on page 11.

FIGURE 3 — THE RECEIVER TIMING DIAGRAM

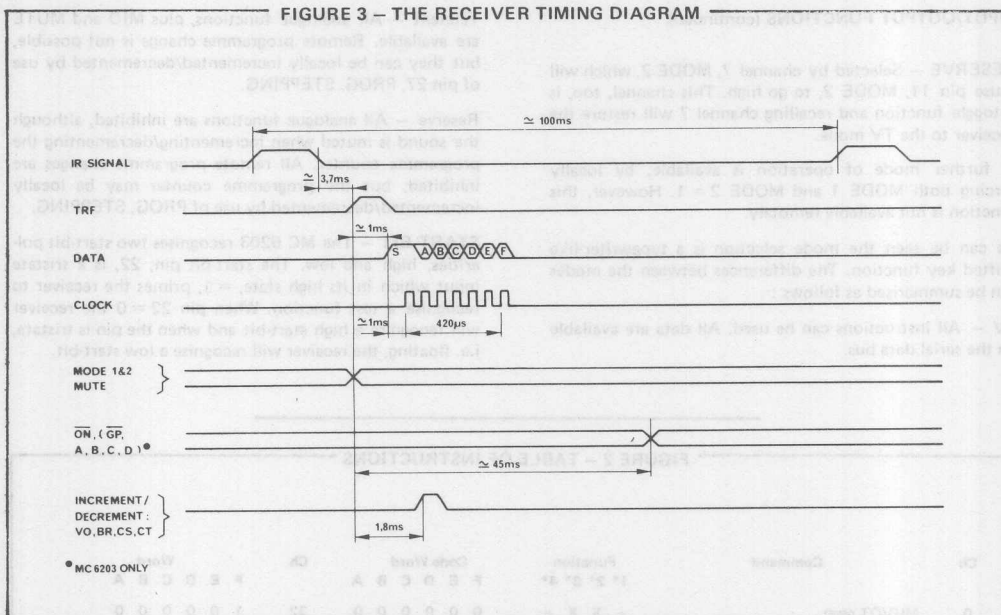


FIGURE 4 — THE TRANSMITTED SIGNAL

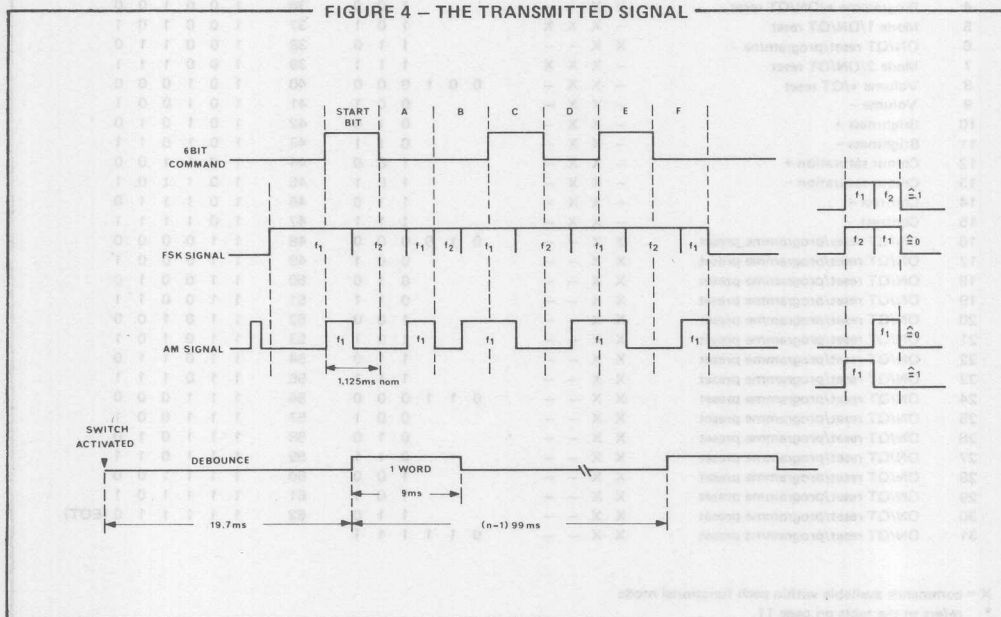
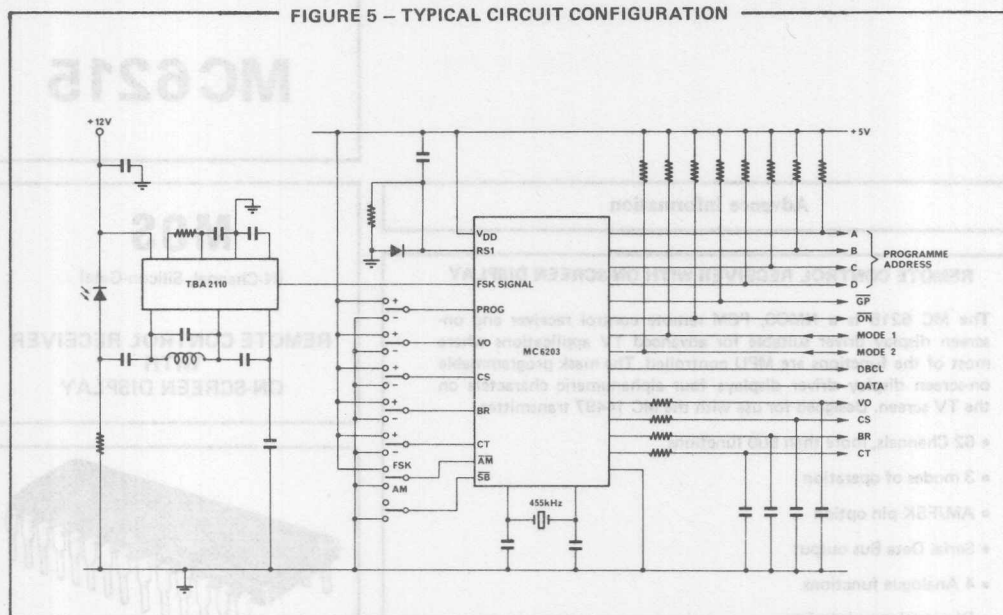
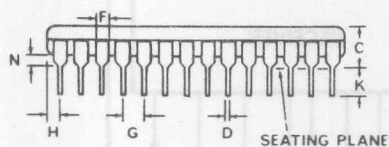
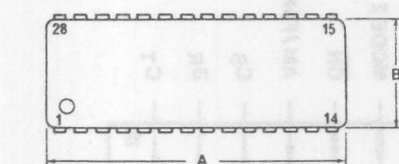


FIGURE 5 - TYPICAL CIRCUIT CONFIGURATION



PACKAGE DIMENSIONS

PLASTIC PACKAGE
CASE 710-01

NOTES

- 1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION
- 2 DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW PACKAGE BASE)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.41	2.57	0.095	0.105
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MC6215

Advance Information

REMOTE CONTROL RECEIVER WITH ON-SCREEN DISPLAY

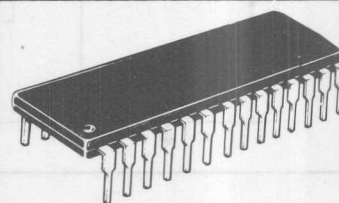
The MC 6215 is a NMOS, PCM remote control receiver and on-screen display driver suitable for advanced TV applications where most of the functions are MPU controlled. The mask programmable on-screen display driver displays four alphanumeric characters on the TV screen. Designed for use with the MC 14497 transmitter.

- 62 Channels, more than 500 functions
- 3 modes of operation
- AM/FSK pin option
- Serial Data Bus output
- 4 Analogue functions
- Direct teletext interface
- Mask programmable character set of 16 characters
- Suitable for 625 line/50Hz TV systems

MOS

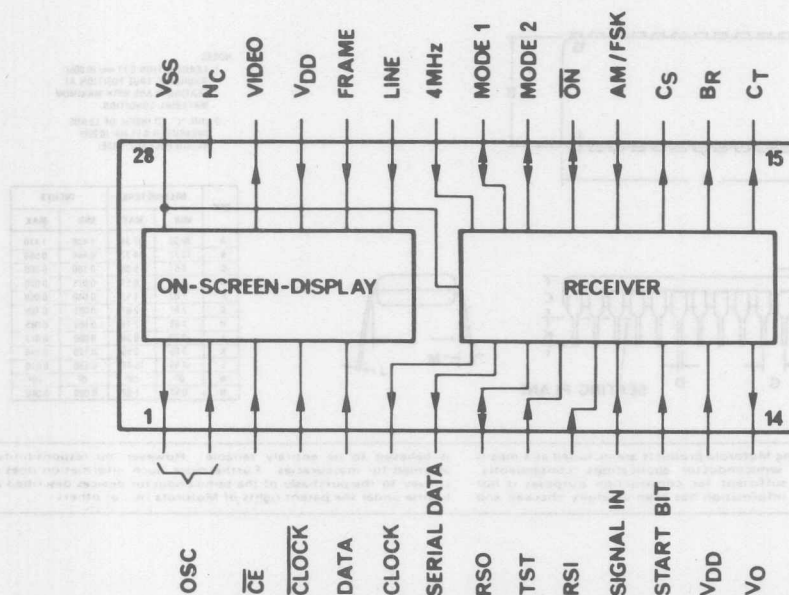
(N-Channel, Silicon-Gate)

REMOTE CONTROL RECEIVER WITH ON-SCREEN DISPLAY



PLASTIC PACKAGE
CASE 710-01

FIGURE 1 — MC 6215 PIN ASSIGNMENT



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +8	Vdc
Voltage on any pin	$V_{i/o}$	-0.3 to +8	Vdc
Storage Temperature	T_{STG}	-55 to +150	$^\circ\text{C}$
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ELECTRICAL CHARACTERISTICS ($V_{DD} = +5.0\text{V}$, $V_{SS} \text{ Gnd}$, $T_A = 25^\circ\text{C}$ unless otherwise noted) Receiver Section

Characteristic	Pin	Condition	Symbol	Min	Typ	Max	Unit
Supply Current	13		I_{DD}			50	mA
Input (Schmitt Trigger) Signal In	11	Hysteresis $V_{IH} = 16\text{V}$	V_{IL} V_{IH} V_{HYST} I_{IH}	3.2 50		1.8 V mV 20	V V mV μA
Input (TST, $\overline{\text{AM}}$ /FSK)	9, 18	$V_{IH} = 16\text{V}$	V_{IL} V_{IH} I_{IH}	4.0		0.5 V 20	V V μA
Input (Schmitt Trigger) RSI	10	$V_{IL} = 100\text{mV}$	V_{IL} V_{IH} V_{HYST}	400 50		50 mV mV -20	mV mV mV μA
Input/Output (Open Drain) $\overline{\text{ON}}$, Mode 1, Mode 2	19 20 21	$V_{OL} = 0.5\text{V}$ $V_{OH} = 8\text{V}$	V_{IL} V_{IH} ON OFF	4 1.0		0.5 V mA 20	V V mA μA
Output (push-pull) VO, BR, CS, CT	14, 15	$V_{OL} = 0.5\text{V}$	I_{OL}	1.0			mA
Output, Clock, Serial Data	16, 17 6, 7	$V_{OH} = V_{DD} - 1\text{V}$	I_{OH} I_{OL} I_{OH}	-0.2 2.0 -0.2			mA mA mA
Input/Output (Push-pull) RSO	8	$V_{OL} = 0.5\text{V}$ $V_{OH} = V_{DD} - 1\text{V}$ V_{IL} V_{IH} V_{HYST}	I_{OL} I_{OH}	100 -10 400 50		-100 50 mV mV	μA μA mV mV
Input f_{REF} (4MHz)	22	$V_{IH} = 16\text{V}$	V_{IL} V_{IH}	3.3		0.8 V 20	V V μA

ELECTRICAL CHARACTERISTICS (continued)

ON-SCREEN DISPLAY SECTION

Characteristic	Pin	Condition	Symbol	Min	Typ	Max	Unit
Supply Current (Output Open)	25	$V_{DD} = 5.5V$ $T = 0^\circ C$				25	mA
Inputs (Schmitt Trigger) Line, Frame, Clock, \overline{CE}	23		V_{IL}			0.8	V
	24		V_{IH}	2.6			V
	3, 4		V_{HYST}	0.1			V
Input Data	5		V_{IL}			0.8	V
			V_{IH}	4.0			V
Video Output	26	$V_{VL} = 0.8V$	I_{VL}	1.6			mA
		$V_{VH} = 2.4V$	I_{VH1}	-0.2			mA
		$V_{VH} = 2.0V$	I_{VH2}	-0.7			mA

SWITCHING CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_A = 0$ to $70^\circ C$)

Characteristic	Pin	Condition	Symbol	Min	Typ	Max	Unit
Chip select to clock lead time			t_{CSL}	0.4			μS
Chip deselect to clock lead time			t_{CSG}	0.4			μS
Data to clock lead time			t_{DL}	0.1			μS
Clock to chip deselect time			t_{CLCS}	50			nS
Clock LOW time			t_{CLL}	0.8		12.0	μS
Clock period			t_C	4.0			μS
Video rise time		$V_{VH} = 2V$	t_{VR}			120	nS
Video fall time		$V_{VL} = 0.3V$ $CL = 30pF$	t_{VF}			120	nS
Oscillator period			t_{OSC}	-5 %	404	+5 %	nS
Line high time		$V_{IHY} = 2V$ $V_{ILY} = 0.8V$	t_{FB}	1.5		14	μS
Frame high time		$V_{IHY} = 2V$ $V_{ILY} = 0.8V$	t_{FR}	$t_{FB} + 10t_{OSC}$			
Line to 1st field lead time			t_{FLD}	6.5			t_{OSC}

INPUT/OUTPUT FUNCTIONS

AM/FSK — By means of a suitable voltage level at pin 18 the receiver will decode AM or FSK modulated signals.

AM MODE — In the AM mode, when pin 18 = 0, the receiver is capable of decoding a modulated or demodulated signal, in this mode the SIGNAL IN pin (pin 11) has to be high, = 1. When receiving a modulated signal the pulse duration must be at least $4.5\mu\text{s}$ with a repetition period of at least $70\mu\text{s}$ if the signal is to be accepted.

FSK MODE — In the FSK mode, when pin 18 = 1, the receiver will accept only a demodulated input signal, at the same time the quiescent level of pin 11 is arbitrary.

ANALOGUE CONTROLS — On reception of a code word for one of the four analogue functions the digital/analogue (D/A) convertor in the receiver generates an analogue voltage, normally used to control the volume (VO), brightness (BR), colour saturation (CS) or contrast (CT) of a colour TV receiver. The control voltages are obtained by direct RC integration of a variable duty cycle square wave output from the D/A convertor. The total sweep time of the overflow/underflow protected D/A convertor is 6s; derived from a repetition rate of 7.1kHz and a D/A convertor resolution of 60 steps. Operation of the analogue controls is inhibited in the STANDBY mode.

MID — (Middle Position) This presets all the analogue functions to 50 %, with the exception of VO which is set to 33 %. It is operative under the following conditions :

- When switching from OFF to ON
- When MID, channel 0, is selected.

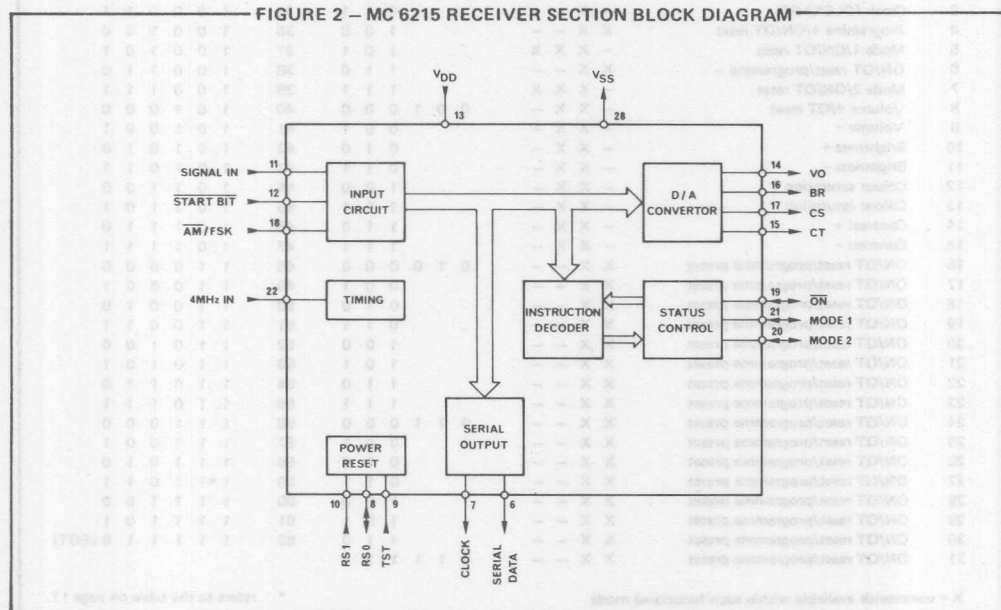
MUTE (QT) — This is an internal latch, which when set mutes the sound by pulling the VO line low, = 0. It is a toggle function controlled by channel 1, QT.

QT is reset by :

- Channel 0, MID
- Channel 2, STANDBY
- Channel 8, VO+
- Channels 16 to 25, programme channels
- Channels 5 and 7, mode changes
- Channel 1, QT

SERIAL DATA BUS — The serial data bus releases into the system words which have been received and recognised as valid, thus they will conform to the remote control code and sequence. The format of the serial output data (DATA) and clock (CLOCK) are shown in figure 4.

FIGURE 2 — MC 6215 RECEIVER SECTION BLOCK DIAGRAM



MODES OF OPERATION — Four operational modes, or functions, are available which, although their application is unlimited, are identified as shown below :

Function	Pin		
	ON	Mode 1	Mode 2
1* Standby	1	X	X
2* TV	0	0	0
3* Teletext	0	1	0
4* Reserve	0	0	1

* refers to the function number with figure 3. X = do not care

MODE SELECTION

Standby — selected by channel 2, STANDBY. At this time pin ON is high.

TV — This is the prime active mode and is selected by channel 6, ON or any programme channel, 16 to 25.

Teletext — Selected by channel 5, MODE 1, at this time the MODE 1 pin will be high. As channel 5 is a toggle function, reselection of this channel will return the receiver to the TV mode.

Reserve — Selected by channel 7, MODE 2, which will be high. This channel, too, is a toggle function and recalling channel 7 will restore the receiver to the TV mode.

A further mode of operation is available, by locally forcing both MODE 1 and MODE 2 = 1. However, this function is not available remotely.

As can be seen the mode selection is a typewriter-like shifted key function. The differences between the modes can be summarised as follows :

TV — All instructions can be used.

All data are available on the serial data bus.

Teletext — All analogue functions, plus MID and MUTE are available.

Remote programme change is not possible.

Reserve — All remote programme changes are inhibited.

FIGURE 3 — TABLE OF INSTRUCTIONS

FIGURE 3 – TABLE OF INSTRUCTIONS															
Ch	Command	Function 1* 2* 3* 4*	Code Word					Ch	Word						
			F	E	D	C	B		A	F	E	D	C	B	A
0	MID/QT reset	— X X —	0	0	0	0	0	0	32	1	0	0	0	0	0
1	MUTE (QT)	— X X —				0	0	1	33	1	0	0	0	0	1
2	Standby/QT reset	X X X X				0	1	0	34	1	0	0	0	1	0
3	Clock (CLCK) GP	— X — —				0	1	1	35	1	0	0	0	1	1
4	Programme +/ON/QT reset	X X — —				1	0	0	36	1	0	0	1	0	0
5	Mode 1/ON/QT reset	— X X X				1	0	1	37	1	0	0	1	0	1
6	ON/QT reset/programme —	X X — —				1	1	0	38	1	0	0	1	1	0
7	Mode 2/ON/QT reset	— X X X				1	1	1	39	1	0	0	1	1	1
8	Volume +/QT reset	— X X —	0	0	1	0	0	0	40	1	0	1	0	0	0
9	Volume —	— X X —				0	0	1	41	1	0	1	0	0	1
10	Brightness +	— X X —				0	1	0	42	1	0	1	0	1	0
11	Brightness —	— X X —				0	1	1	43	1	0	1	0	1	1
12	Colour saturation +	— X X —				1	0	0	44	1	0	1	1	0	0
13	Colour saturation —	— X X —				1	0	1	45	1	0	1	1	0	1
14	Contrast +	— X X —				1	1	0	46	1	0	1	1	1	0
15	Contrast —	— X X —				1	1	1	47	1	0	1	1	1	1
16	ON/QT reset/programme preset	X X — —	0	1	0	0	0	0	48	1	1	0	0	0	0
17	ON/QT reset/programme preset	X X — —				0	0	1	49	1	1	0	0	0	1
18	ON/QT reset/programme preset	X X — —				0	1	0	50	1	1	0	0	1	0
19	ON/QT reset/programme preset	X X — —				0	1	1	51	1	1	0	0	1	1
20	ON/QT reset/programme preset	X X — —				1	0	0	52	1	1	0	1	0	0
21	ON/QT reset/programme preset	X X — —				1	0	1	53	1	1	0	1	0	1
22	ON/QT reset/programme preset	X X — —				1	1	0	54	1	1	0	1	1	0
23	ON/QT reset/programme preset	X X — —				1	1	1	55	1	1	0	1	1	1
24	ON/QT reset/programme preset	X X — —	0	1	1	0	0	0	56	1	1	1	0	0	0
25	ON/QT reset/programme preset	X X — —				0	0	1	57	1	1	1	0	0	1
26	ON/QT reset/programme preset	X X — —				0	1	0	58	1	1	1	0	1	0
27	ON/QT reset/programme preset	X X — —				0	1	1	59	1	1	1	0	1	1
28	ON/QT reset/programme preset	X X — —				1	0	0	60	1	1	1	1	0	0
29	ON/QT reset/programme preset	X X — —				1	0	1	61	1	1	1	1	0	1
30	ON/QT reset/programme preset	X X — —				1	1	0	62	1	1	1	1	1	0 (EOT)
31	ON/QT reset/programme preset	X X — —	0	1	1	1	1	1							

X = commands available within each functional mode

* refers to the table on page 11.

X = commands available within each functional mode

* refers to the table on page 11.

CIRCUIT OPERATION

The MC 6215 is an integrated circuit bi-phase coded PCM remote control receiver able to receive 62 channels in any of 3 modes. Reception may, optionally, be AM or FSK.

The transmitted information is in the form of a 7-bit word, see figure 10 for format, a start bit and 6 information bits. On reception of a signal the receiver performs a series of tests to achieve the necessary noise immunity and check the validity of the signal :

- The bi-phase code is checked to ensure that there is only one edge during any one time window.
- The word length is checked for the presence of 7 bits.
- The noise level is checked.

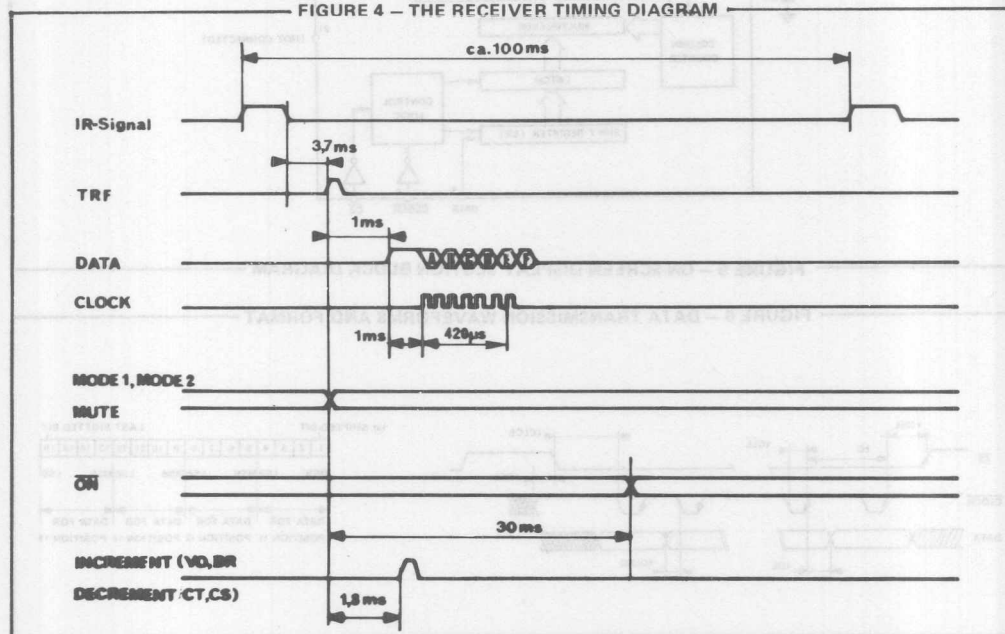
The latter test is carried out only in the AM mode. After reception of an apparently valid word the receiver waits for some 3ms to verify the presence of noise or other transients. Should these be present the word is rejected and not decoded. Should the word, on the other hand, be found to be valid it is moved into a latch, by the signal TRF (see figure 4) and decoded. At the same time it is released on the serial data bus.

The end of transmission is notified by the reception of the "End of Transmission" code, channel 62. In the case of the MC 14497 transmitter this is transmitted automatically when any button is released. This word, too, is available on the serial data bus. In the eventuality of the transmission being interrupted for more than 570ms an internal timer will automatically generate the "End of Transmission" code which will be processed in the normal manner.

While only channels 0 to 25 and 62 are recognised by the internal instruction decoder, all 62 commands are available on the serial data bus; in the TV mode whatever is received at the Signal In pin will be repeated on the bus. In any other mode, i.e. when pins Mode 1 and/or Mode 2 are high the clock line will be disabled after the first signal has been released. The line will be enabled again after receiving an end-of-transmission code (channel 62) or when the time-out counter has timed out.

When power is applied to the circuit the reset circuitry sets up the initial position : $\overline{ON} = 1$ (standby), Mode 1 and 2 = 0 (TV), QT = reset and the D/A Convertors are at Mid. Depending on the external components the power reset can be either dynamic, using pin RS1 as shown in figure 11, or static using pin RSO. Normally the test input, TST, is held at 0V.

FIGURE 4 — THE RECEIVER TIMING DIAGRAM



CIRCUIT OPERATION (continued)

REFERENCE FREQUENCY – The reference frequency for the receiver is the 4MHz used by the MPU.

\overline{SB} – This pin, 12, is the start bit input. When $\overline{SB} = 1$ the receiver will recognise a low start bit. Conversely, when $\overline{SB} = 0$, the receiver will recognise a high start bit. This facility is confined to AM operation.

THE ON-SCREEN DISPLAY SECTION

The general operation of the On-Screen Display circuit can be followed by referring to figures 5 to 9.

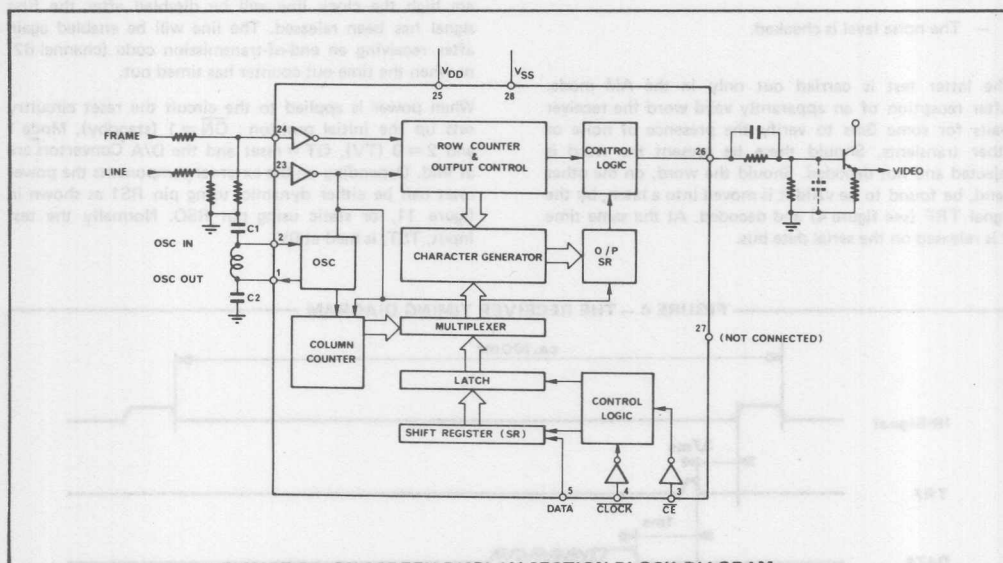
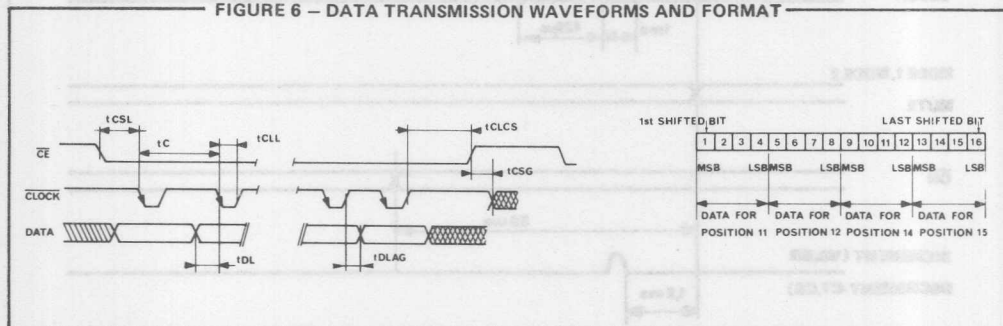
The character information is transmitted serially from

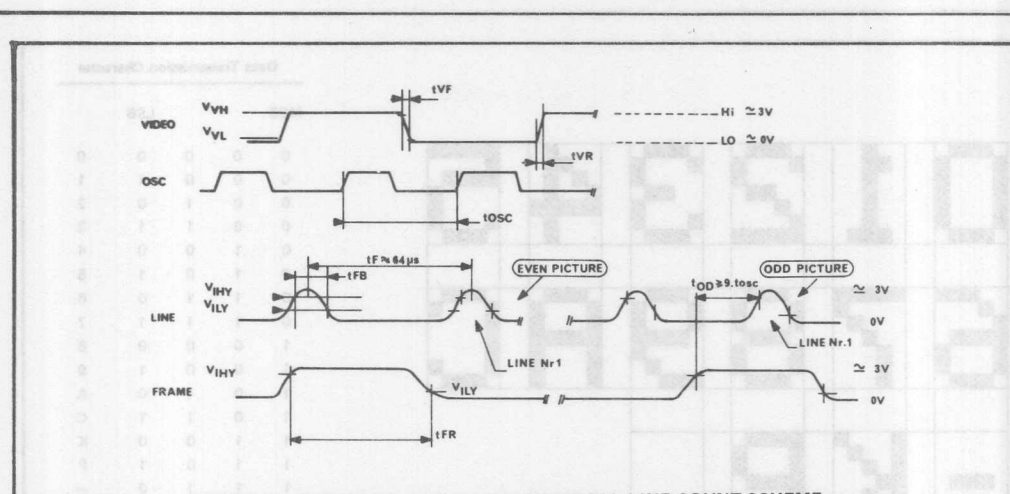
the MPU to the MC 6215 in the form of a 16-bit code and is in fact clocked in to the shift register by 16 clock pulses while $CE = 0$. All clock pulses are ignored while $CE = 1$, as can be seen from figure 6.

While CE , the chip select, = 0 the input latches are disconnected from the shift register. Data are samples during the high-low transition of the **CLOCK** input.

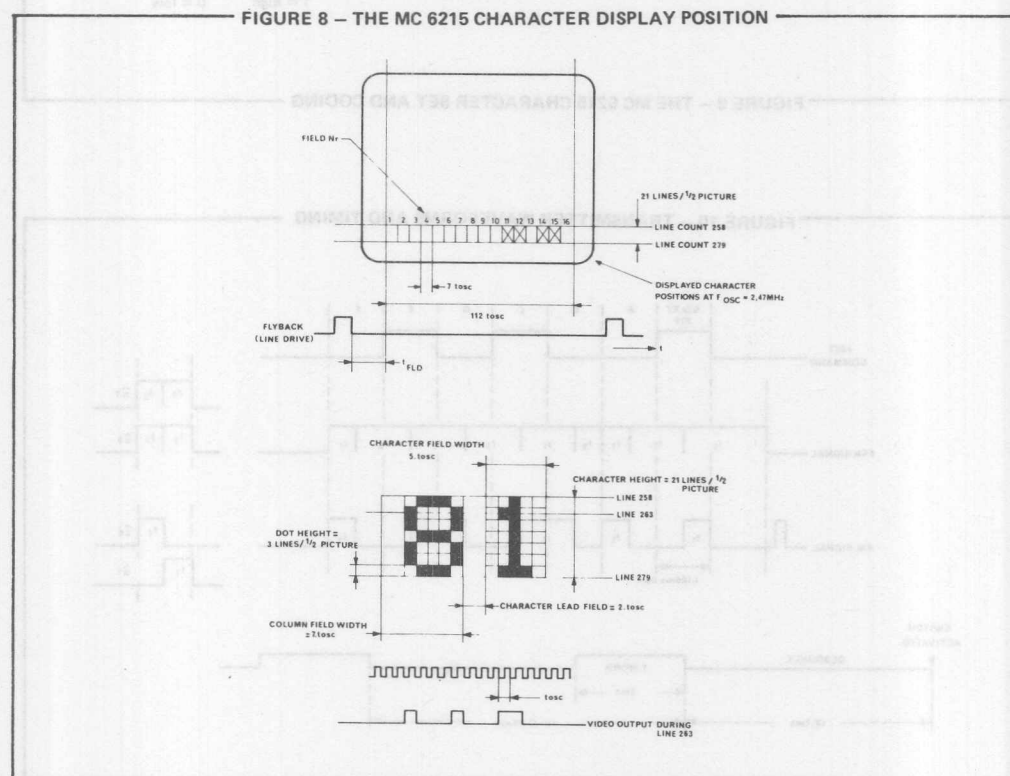
The mask programmable characters are formed on a 5 X 7 matrix, shown in figure 8, with a dot height of 3 lines per half picture and a dot width of one cycle of the stop-start oscillator, with a nominal frequency of 2.4MHz.

As can be seen from figure 8 the characters are displayed in positions 11, 12, 14 and 15 between lines 258 and 279.

**FIGURE 5 – ON-SCREEN DISPLAY SECTION BLOCK DIAGRAM****FIGURE 6 – DATA TRANSMISSION WAVEFORMS AND FORMAT**



- FIGURE 7 – THE VIDEO SIGNAL AND VERTICAL LINE COUNT SCHEME



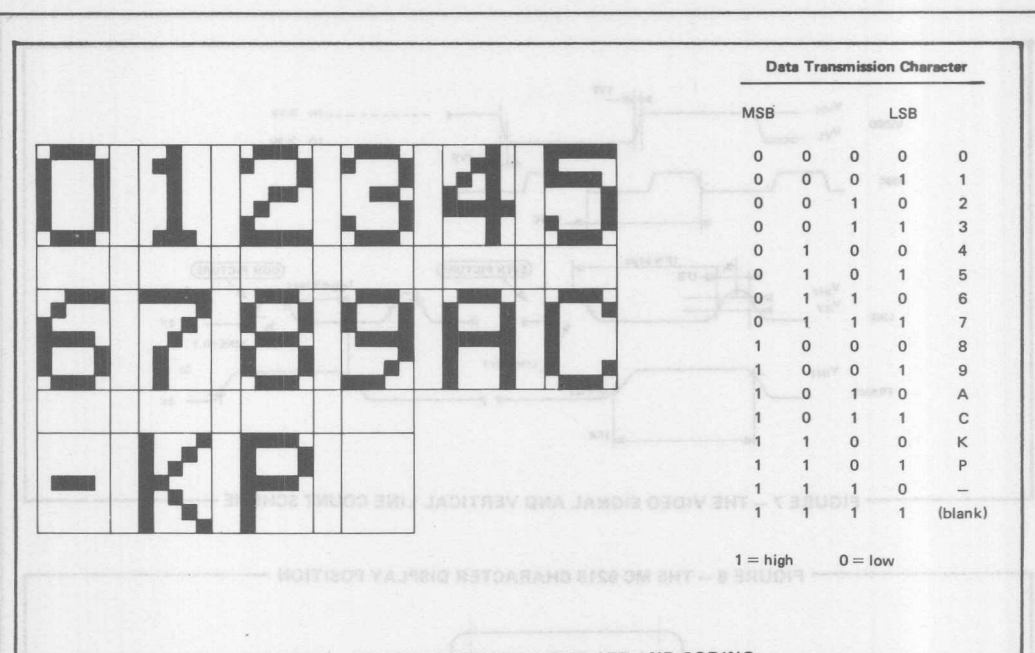


FIGURE 9 — THE MC 6215 CHARACTER SET AND CODING

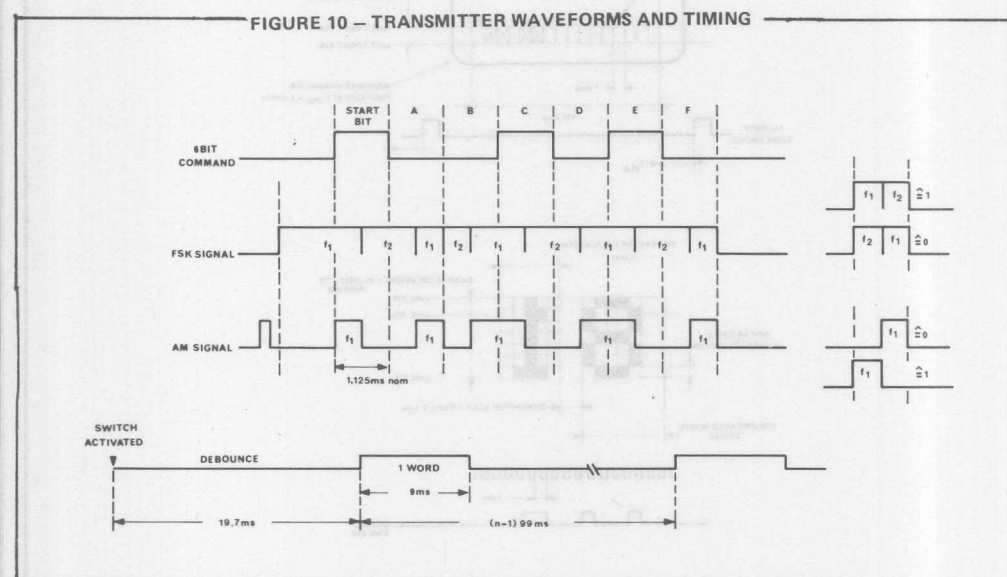


FIGURE 10 — TRANSMITTER WAVEFORMS AND TIMING

MC6215

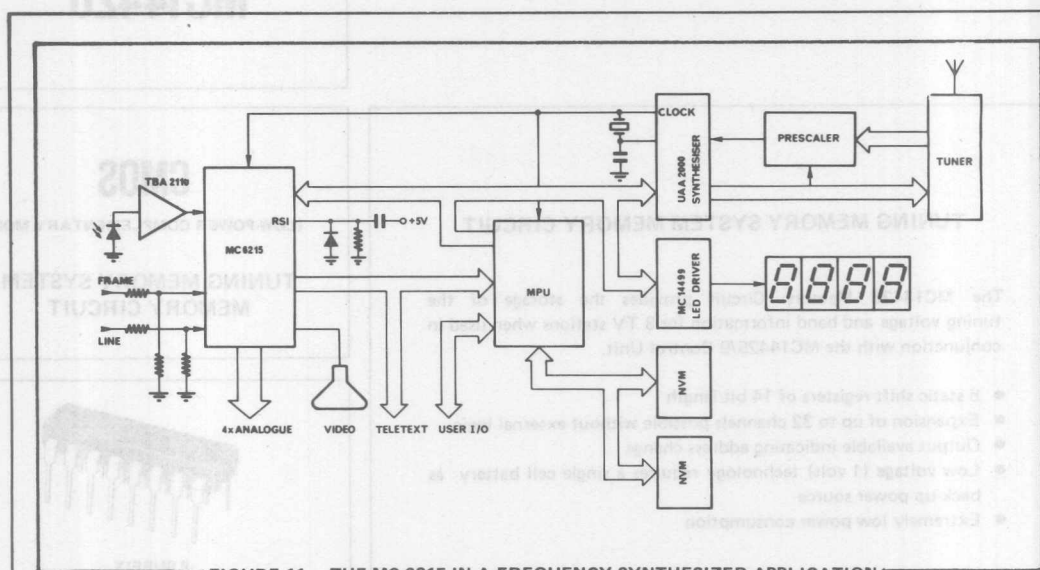
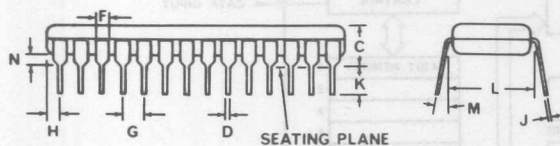
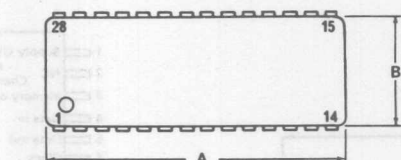


FIGURE 11 — THE MC 6215 IN A FREQUENCY SYNTHESIZER APPLICATION

PACKAGE DIMENSIONS

PLASTIC PACKAGE
CASE 710-01



- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION
 - DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW PACKAGE BASE).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.32	37.34	1.430	1.470
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.38	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.41	2.67	0.095	0.105
G	1.65	2.16	0.065	0.085
H	0.20	0.30	0.008	0.012
I	3.05	3.56	0.120	0.140
J	14.99	15.49	0.590	0.610
K	0°	10°	0°	10°
L	0.51	1.02	0.020	0.040

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MC14426

CMOS

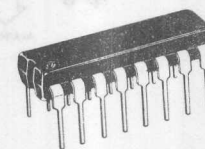
(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM MEMORY CIRCUIT

TUNING MEMORY SYSTEM MEMORY CIRCUIT

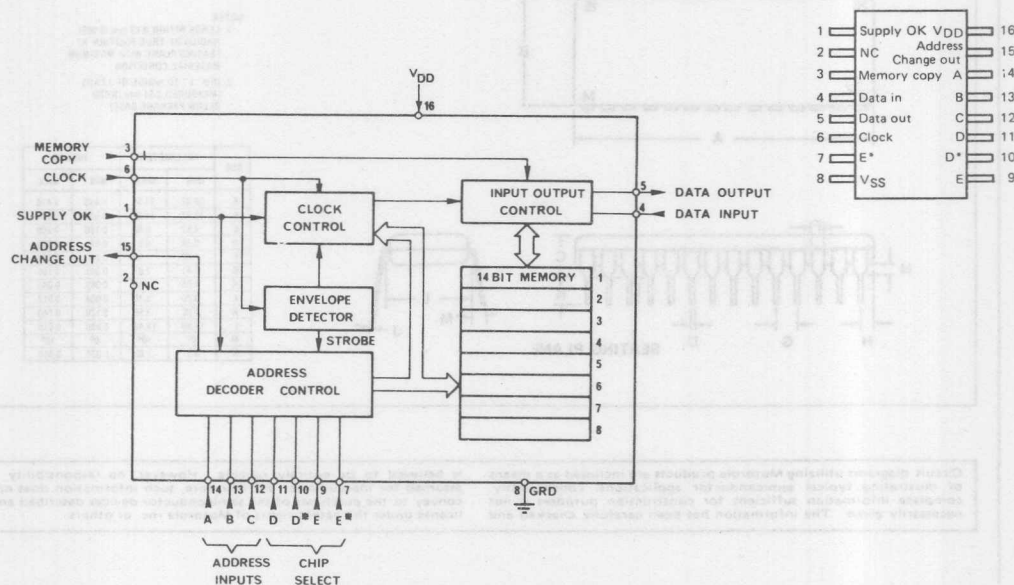
The MC14426 Memory Circuit provides the storage of the tuning voltage and band information for 8 TV stations when used in conjunction with the MC14425/9 Control Unit.

- 8 static shift registers of 14 bit length
- Expansion of up to 32 channels possible without external logic
- Output available indicating address change
- Low voltage (1 volt) technology requires a single cell battery as back up power source
- Extremely low power consumption



P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 - MC14426 BLOCK DIAGRAM AND PIN-OUT



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6 to -0.5	Vdc
Input Voltage, All inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current drain per pin	I	10	mA
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C) Voltages referenced to V_{SS} , pin 8

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage	V_{DD}	4.0	5.2	6.0	Vdc
Standby Supply Voltage ¹	V_{DD}	1.2	1.5	6.0	Vdc
Quiescent Current ($V_{DD} = 1.5\text{ V}$) ($V_{DD} = 5\text{ V}$)	I_{DD}		0.008 0.5	2.0 15.0	μA dc
Input Voltage ($V_{DD} = 5\text{ V}$)	V_{IL} V_{IH}	4.5		0.5	Vdc
Input Voltage ($V_{DD} = 5\text{ V}$)	V_{IL} V_{IH}	4.0		1.0	Vdc
Input Current all Inputs Except Pin 3. ($V_{DD} = 5\text{ V}$)	I_{IN}		10		pA
Input Current ² ($V_{DD} = 5\text{ V}$)	I_{IN}	-1.5	-3.0	-6.0	μA
Input Capacitance all Inputs ($V_{IN} = 0\text{ V}$)	C_{IN}		5.0	12.0	pF
Output Current all Outputs (sinking) ($V_{OL} = 0.4\text{ V}$)	I_{OL}	0.4			mA
Three State Output Leakage Current (sinking) ($V_{DD} = 5\text{ V}$)	I_{TL}	± 0.001	± 0.001	± 5.0	μA
Clock Input Frequency ($V_{DD} = 5\text{ V}$)	$f_{max.}$ $f_{min.}$	400	700 25	100	kHz

¹ Standby mode is obtained by lowering Supply OK input to V_{SS} during a few read/write cycles. V_{DD} can then be lowered to its standby value, Pin 1 staying low.

In Standby mode no read/write operation can be performed.

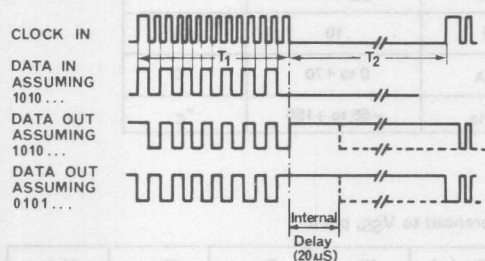
² An internal pull-up resistor is present on pin 3.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

INPUT/OUTPUT FUNCTIONS

DATA IN/OUT — The input/output control section provides the interface between the memory and the control circuit MC14425/9 via pins 5 and 4. The output network is active only when the chip is selected and supply OK (pin 1) is at 1. The relationship between clock and input/output signals is shown below:



It should be noted that the memory copy information on pin 3 input is inserted into the serial data transfer line which goes to the control circuit during period T_2 .

MEMORY COPY — This input is controlled by connecting pin 3 to V_{SS} (ground), which in turn holds down the memory output signal during period T_2 . This function allows to transfer the content of the 14 bit shift register of the control circuit MC14425/9 into any memory location as long as this command is present. Its utilisation is two-fold:

- To resume search for a TV station starting from the last selected station rather than from a random tuning voltage.
- To copy the content of a shift register into a different location. This permits to change the order of TV programs according to the user wish.

SUPPLY OK — In case of power failure this input (pin 1) is used to deactivate all functions of the chip so that no data is lost, provided that V_{DD} is held at 1 volt minimum. (See note 1.)

The supply OK signal is enabled in such a way that deactivation during transfer of information is prevented.

ADDRESS INPUTS — To select the 8 memory words only three A, B, C address bits are required. (pins 14, 13, 12.)

Channel	A	B	C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1

CHIP SELECT — To facilitate the parallel connection of several MC14426 memory circuits, four additional inputs D, D*, E, E* are provided for chip select.

The truth table of chip select inputs is given below.

Chip Selected	Channel	D	D*	E	E*
1	1 to 8	0	0	0	0
2	9 to 16	1	1	0	0
3	17 to 24	0	0	1	1
4	24 to 32	1	1	1	1
None	—	Any other combination			

D* and E* are programming inputs of the chip select network and are normally connected to V_{SS} or V_{DD} .

The logic levels on these inputs specify the levels of the D and E inputs for chip selection.

The chip is selected if $D = D^*$ and $E = E^*$.

As shown in the above truth table up to four circuits (32 channels) can be connected in parallel without external decoding.

CLOCK IN — (pin 6) See MC14425/9 data sheet.

ADDRESS CHANGE — An additional function (pin 15) is available to mute the sound section of the TV set during each address change. The 400msec. one-shot on the control circuit (MC14425/9) provides this feature. This one-shot is triggered by the address change signal supplied by the memory circuit. If the address is changed, the AC signal appears on the leading edge of the internal strobe pulse and lasts one ($T_1 + T_2$) cycle.

MC14429P-B

ADVANCE INFORMATION

TUNING MEMORY SYSTEM CONTROL CIRCUIT

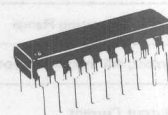
The MC14429B control circuit will perform the following functions when used as part of the Motorola Tuning Memory.

- LC Clock generator
- Underflow protected UP/DOWN Counter providing information for memory
- Rate multiplier for D/A conversion
- Shift register for memory data access and storage of new data
- 2,3 or 4 TV band counter with automatic or manual switching
- Control section for automatic or manual TV station search
- Automatic volume muting control during each search and programme change

CMOS

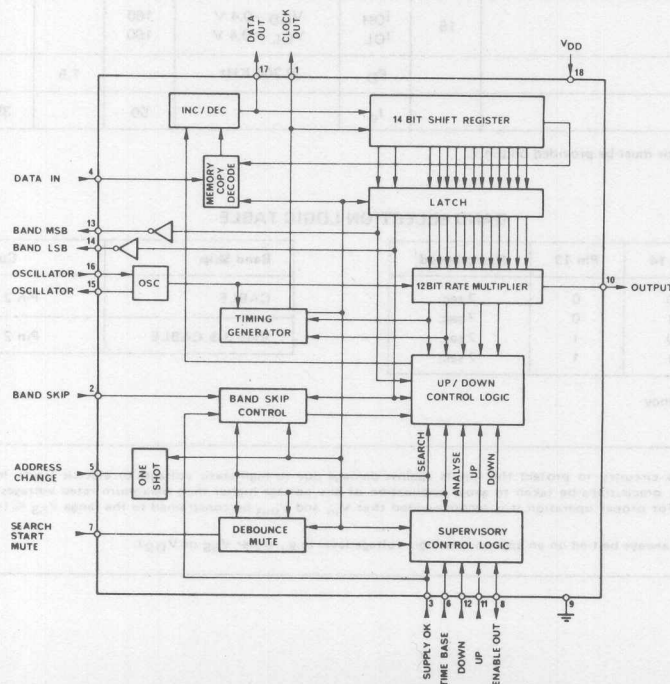
(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM CONTROL CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 707

FIGURE 1 — MC14429B BLOCK DIAGRAM AND PIN-OUT



This is advance information on a new introduction and specifications are subject to change without notice.

MC14429P—B

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6 to -0.5	Vdc
Input Voltage, All inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C) Voltages referenced to V_{SS} , pin 9

Characteristics	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Operating Range	18	V_{DD}		4.95	5.2	6	Vdc
Input Current, All inputs (except pins 5, 7)		I_{in}		—	10	—	pAdc
Enable Output Current	8	I_{OH} I_{OL}	$V_{DD} - 0.4\text{ V}$ 0.4 V	280 280			μAdc μAdc
Band Switching Output Current	13, 14	I_{OH} I_{OL}	$V_{DD} - 0.4\text{ V}$ 0.4 V	280 280			μAdc μAdc
Other Output Currents	1 10, 17	I_{OH} I_{OL}	$V_{DD} - 0.4\text{ V}$ $V_{OL} = 0.4\text{ V}$	280 280			μAdc μAdc
One Shot Output, Search & Mute (see ¹)	5, 7	I_{OL}	$V_{OL} = 0.4$	280			μA
Oscillator	15	I_{OH} I_{OL}	$V_{DD} - 0.4\text{ V}$ $V_{OL} = 0.4\text{ V}$	160 160			μA μA
Power Dissipation		P_D	@ 300 KHz		7.5		mW
Oscillator Frequency		f_o		50		350	KHz

¹ An external pull-up resistor must be provided on pin 7.

BAND SELECTION LOGIC TABLE

Band	Pin 14	Pin 13	Ramp Speed ¹
UHF	0	0	7 sec.
VHF 1	1	0	7 sec.
VHF 3	0	1	7 sec.
CABLE	1	1	7 sec.

Band Skip	Connect
CABLE	Pin 2 to Pin 13
VHF 3 & CABLE	Pin 2 to Pin 14

¹ At 300 KHz Clock frequency

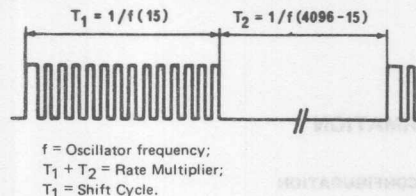
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

INPUT/OUTPUT FUNCTIONS

CLOCK OUT — Clock pulses (PIN 1) control the transfer of data between the MC14429B control chip and the memory chip via pins 4 and 17. For best system performance the oscillator circuit should generate a pulse train of approximately 300kHz, however the frequency value is not critical.

The clock out signal timing is shown below.



BRM OUTPUT — The binary rate multiplier output is available on pin 10.

The binary word cycle is approximately 13 msec for a clock frequency of 300 KHz (3.3 μ sec pulse width). The output provides pulses symmetrically spaced to facilitate the filtering when doing D/A conversion.

In the block diagram of Figure 1, the least significant bit is to the right. Bits 13 and 14 represent band information, therefore overflow of the rate multiplier control word automatically increments band information.

SEARCH & MUTE — Search mode is initiated by presenting a 0 on pin 7. For trouble free operation the signal on pin 7 is debounced internally on both edges for 13 msec. As soon as search is initiated and the debounce cycle is terminated this pin becomes an output for the mute signal which is available during the whole cycle. The search cycle ends when a valid station is found and the one shot (R/C on pin 5) has timed out. The mute signal is available also at address change and during any other time the one shot is active. Each time the oneshot is reset the mute output will momentarily go to high and back to low for less than 13 msec. It is therefore recommended to introduce a proper time constant on this line to smooth out the mute function.

Mute is also provided when supply OK input (pin 3) is VSS.

Two ramp modes are present:

1. Search mode, with a rate of change of 8 steps per clock cycle and a scan time of 7 seconds.
2. Tracking mode, used for manual search or normal locked on conditions, with a rate of change of 1 step per clock cycle and a scan time of 56 seconds.

Search mode is terminated by the simultaneous presence of a 1 on both inputs UP (pin 11) and DOWN (pin 12).

SUPPLY OK — An input (pin 3) is provided to ensure that during power failures, flash-overs, low supply voltages, etc., no memory information can be modified or lost. In operating conditions it should receive a 1 from the

linear processors UAA1008A/C. When at 0 the Search FF, analyse FF and Band skip FF are all reset. The UP/DOWN control logic is not inhibited and a 1 on the UP or DOWN inputs still could modify the content of the shift register.

However, due to the fact that the memory circuit does not send any information when Supply OK is at 0, no data can be modified.

TIME BASE — This input (pin 6) receives a 1 whenever coincidence between fly-back and video sync signals has been detected by the linear processors UAA1008A/C. In the search mode the presence of a 1 on pin 6 is checked by the analyse flip-flop set by the one shot. If time base information is present before the one shot is timed out (usually 400 msec. from ramp stop) the analyse FF is reset, search/mute ends and a stable situation reached. Should time base be 0 when the one shot times out, search will resume.

If in Memory/Normal mode, the presence of a 1 on pin 6 will force Enable Out to low, if at 0 Enable Out will go to the tristate condition.

ENABLE OUT — This output (pin 8) is used to control the AFC OUT gate and UP/DOWN overlap in the linear processor circuit UAA1008A/C.

Its truth-table is the following:

Search FF (internal)	Analyse FF (internal)	Time Base IN (PIN 6)	Enable OUT (PIN 8)
0	0	0	Tristate
0	0	1	0
0	1	0	0
0	1	1	0
1	X	X	1
0	0	X	Tristate

X : Don't care

- The first line of the truth table indicates that the system is in its memory mode and that no TV station is received.
- The second line indicates that a valid TV station is received and system is in its normal memory mode.
- The third line shows the states during the "oneshot" period, e.g. the search function has been interrupted temporarily and waits for Time Base signal.
- The fourth line is as above but Time Base is present.
- The fifth line represents Search mode, the search FF is set and enable out is forced to 1.
- The sixth line represents Address Change, enable out goes tristate during the on time of the one shot.

UP & DOWN — These two inputs (pin 11 & 12) have two modes of operation.

When the system is in search, only the simultaneous presence of an UP and a DOWN signal, both of them at 1,

will interact with the system by stopping the search ramp. A 1 on only one of the two inputs does not stop search nor reduce search speed. Logic has been included to improve the "Stop process" by making it independent of the up and down width when both at 1.

When the circuit is not in search, a 1 on the UP or DOWN inputs results in adding or subtracting a one to or from the content of the 14 bit shift register during each rate multiplier cycle. Built-in underflow protection prevents a band change if the digital word is zero and a DOWN command is initiated.

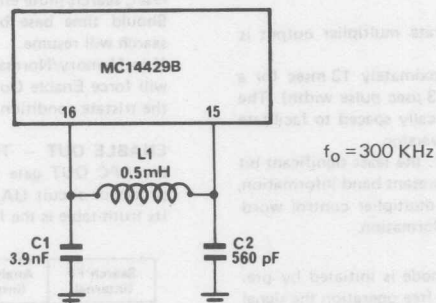
BAND CODE — Refer to band selection logic table for output code. (pin 13 MSB, pin 14 LSB).

A maximum of four bands are available. Three or two bands only can be obtained by connecting pin 2 to pin 13 or 14 as per band selection logic table.

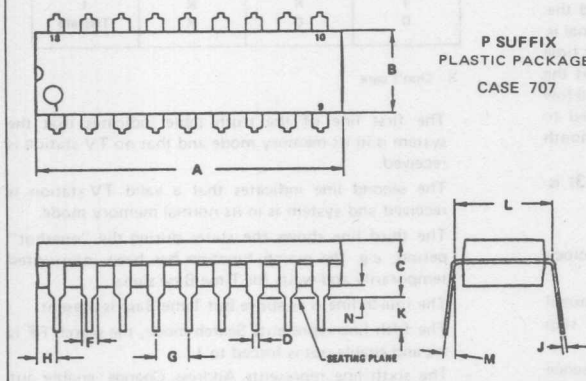
Note that no debounce network is included on pin 2 input. Therefore, if manual band skip is required, provision for a bounce-free input signal has to be made.

APPLICATION INFORMATION

RECOMMENDED OSCILLATOR CONFIGURATION



OUTLINE DIMENSIONS



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54	8SC	0.100	8SC
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62	8SC	0.300	8SC
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLO FLASH.

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MC14430

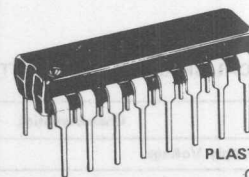
CMOS

INPUT ADDRESS ENCODER

INPUT ADDRESS ENCODER

The MC14430 is an integrated circuit designed for program selection address in TV and radio receivers by means of push button switches.

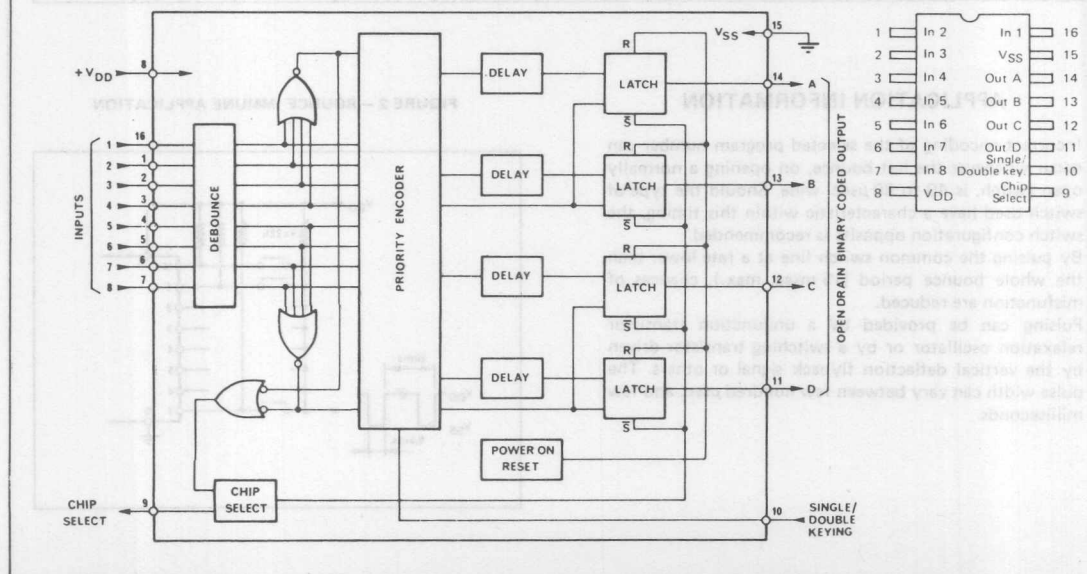
- 8 program inputs
- Binary coded open drain latched output
- Push button type keyboard allows for electrical isolation in live chassis applications
- Single or double keying operation possible
- Up to four circuits can be cascaded
- Normally closed or normally open switches can be used.



PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

FIGURE 1 — MC14430 BLOCK DIAGRAM & PIN-OUT



MC14430

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+10 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage	V_{DD}	4	5.2	6	Vdc
Quiescent Current per Package (Pins 16,1,2, 3,4,5,6,7 open or grounded)	I_{DD}	—	0.068	10	μAdc
Input Voltage	"O" Level "I" Level	V_{IL} V_{IH}	2.25 2.75	1.5 —	Vdc
Input Current	$V_{DD} = 5\text{ V}$ $V_{in} = 1\text{ V}$ $V_{in} = 2\text{ V}$ $V_{in} = 5\text{ V}$	I_{in}	— 2.1 2.6 2.6	— — — 6.0	μAdc
Output Drive Current ($V_{OL} = 0.5\text{ V}$)	$V_{DD} = 5\text{ V}$	I_{OL}	2.5	6.2	mAdc
Output Drive Current ($V_{OL} = 0.5\text{ V}$)	$V_{DD} = 5\text{ V}$	I_{OL}	0.9	2.25	mAdc

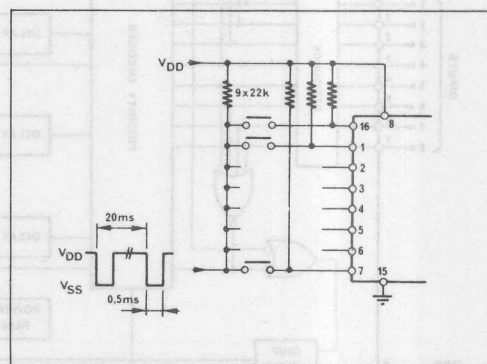
APPLICATION INFORMATION

Incorrect encoding of the selected program number can occur whenever the last bounce, on opening a normally open switch, is 40 to 60 $\mu\text{sec.}$ wide. Should the type of switch used have a characteristic within this timing, the switch configuration opposite is recommended.

By pulsing the common switch line at a rate lower than the whole bounce period (15 msec. max.), chances of misfunction are reduced.

Pulsing can be provided by a unijunction transistor relaxation oscillator or by a switching transistor driven by the vertical deflection flyback signal or others. The pulse width can vary between few hundred $\mu\text{sec.}$ and few milliseconds.

FIGURE 2 — BOUNCE IMMUNE APPLICATION



APPLICATION INFORMATION

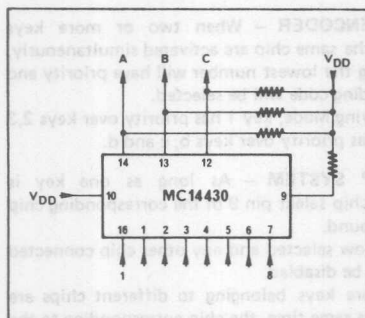


FIGURE 3 — 8 CHANNELS SINGLE KEYING

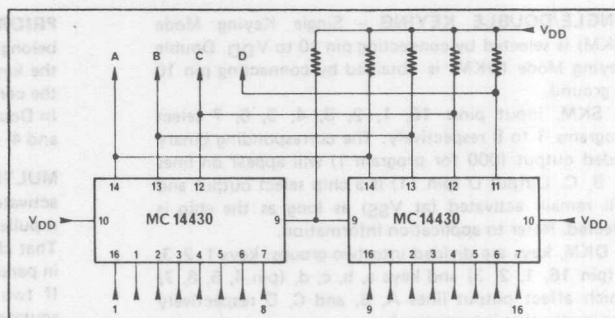


FIGURE 4 — 16 CHANNELS SINGLE KEYING

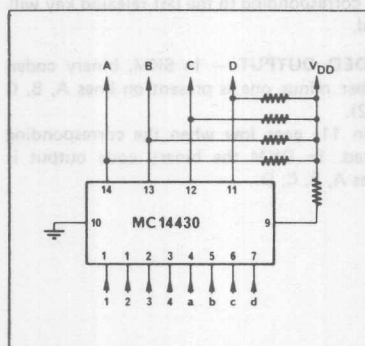


FIGURE 5 — 16 CHANNELS DOUBLE KEYING

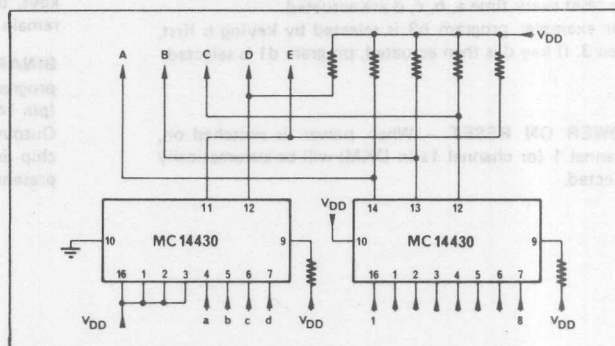


FIGURE 6 — 32 CHANNELS DOUBLE KEYING

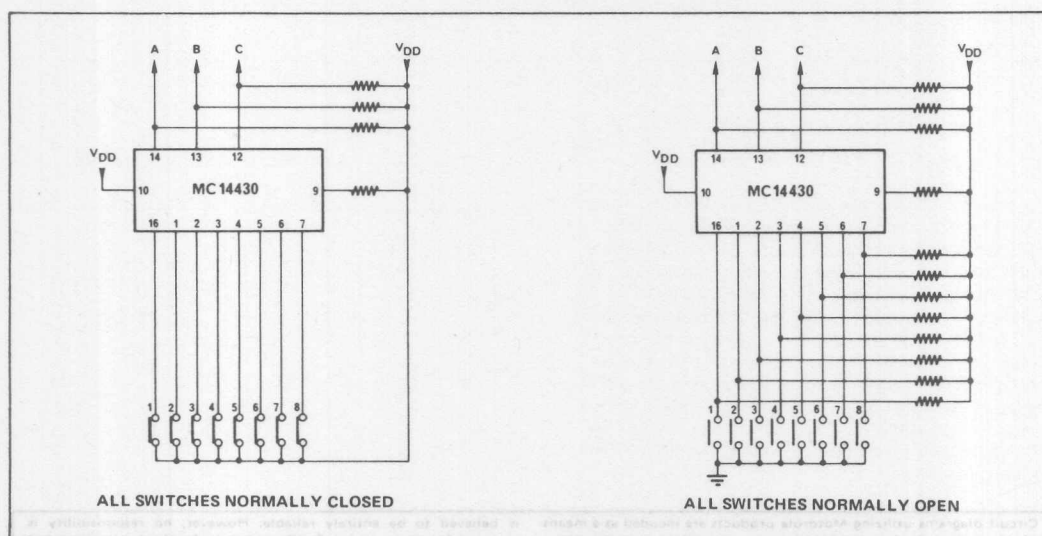


FIGURE 7 — PUSH BUTTON ELECTRICAL DIAGRAM

INPUT/OUTPUT FUNCTIONS

SINGLE/DOUBLE KEYING — Single Keying Mode (SKM) is selected by connecting pin 10 to V_{DD} . Double Keying Mode (DKM) is obtained by connecting pin 10 to ground.

In SKM, input pins: 16, 1, 2, 3, 4, 5, 6, 7 select programs 1 to 8 respectively. The corresponding binary coded output (000 for program 1) will appear on lines A, B, C. Output D (pin 11) is a chip select output and will remain activated (at V_{SS}) as long as the chip is selected. Refer to application information.

In DKM, keys are divided into two groups: keys 1, 2, 3, 4 (pin 16, 1, 2, 3) and keys a, b, c, d, (pin 4, 5, 6, 7) which affect output lines A, B, and C, D respectively (see application information).

Keying sequence is important since output lines A and B are reset every time a, b, c, d are actuated.

For example: program b3 is selected by keying b first, then 3. If key d is then actuated, program d1 is selected.

POWER ON RESET — When power is switched on, channel 1 (or channel 1a in DKM) will be automatically selected.

PRIORITY ENCODER — When two or more keys belonging to the same chip are activated simultaneously, the key having the lowest number will have priority and the corresponding code will be selected.

In Double Keying Mode, key 1 has priority over keys 2, 3 and 4, key a has priority over keys b, c and d.

MULTI CHIP SYSTEM — As long as one key is activated the chip select pin 9 of the corresponding chip is pulled to ground.

That chip is now selected and any other chip connected in parallel will be disabled.

If two or more keys belonging to different chips are actuated at the same time, the chip corresponding to the first actuated key will be selected. When releasing the keys, the chip corresponding to the last released key will remain selected.

BINARY CODED OUTPUT — In SKM, binary coded program number minus one is present on lines A, B, C (pin 14, 13, 12).

Output D (pin 11) goes low when the corresponding chip is selected. In DKM the binary code output is present on lines A, B, C, D.

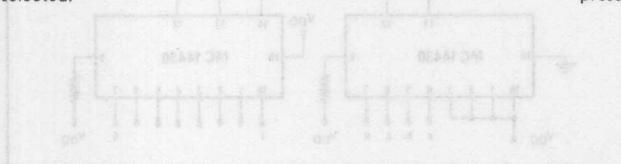


FIGURE 2 - 32 CHANNELS DOUBLE KEYING



FIGURE 3 - 16 CHANNELS DOUBLE KEYING

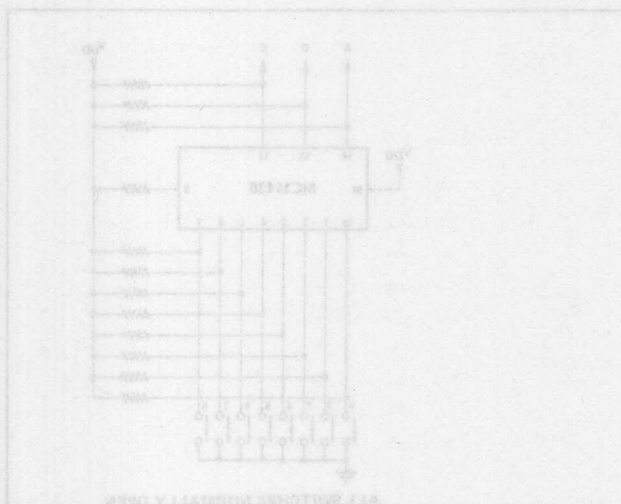


FIGURE 4 - 16 CHANNELS SINGLE KEYING

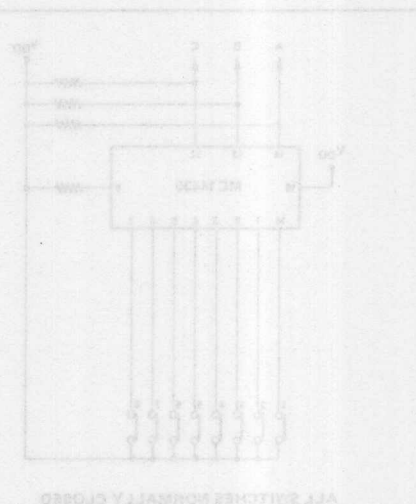


FIGURE 5 - 32 CHANNELS SINGLE KEYING

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is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MC14493 MC14494

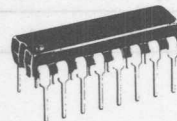
BINARY TO SEVEN SEGMENT LATCH/DECODER/DRIVER FOR 1½ DIGITS

The MC14493 and the MC14494 are 1½ digit 7 segment decoder and driver circuits designed for TV program number display or general purpose applications.

- The MC14493 provides binary plus one decoding
- The MC14494 provides binary decoding
- Designed to drive common cathode LED displays
- VCR output is activated whenever program 16 is displayed
- High current sourcing outputs with internal limiting resistance
- Internal input Level shift.

CMOS

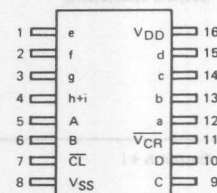
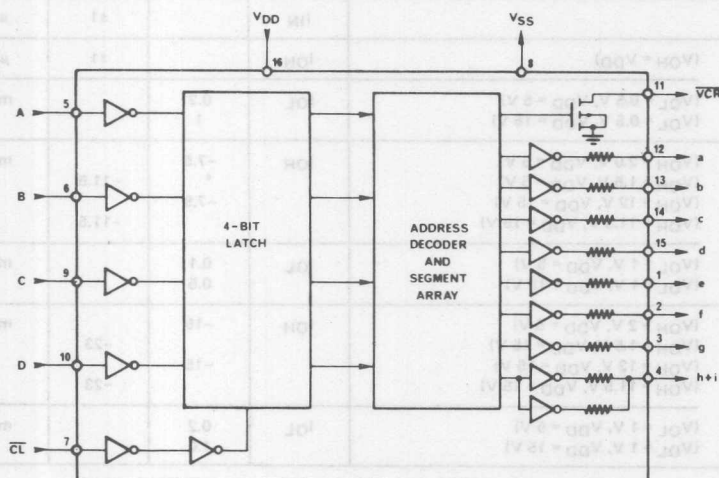
SEVEN SEGMENT DECODER/DRIVER



CASE 648
PLASTIC PACKAGE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated, voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

FIGURE 1 — BLOCK DIAGRAM & PIN ASSIGNMENT



MC14493 MC14494

MAXIMUM RATING ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 V to +18	V_{dC}
Input Voltage, all Inputs	V_{IN}	-0.5 V to $V_{DD} + 0.5$	V_{dC}
DC Current Drain per Input	I	10	mA
Dissipation per Output Driver Pins 1, 2, 3, 12, 13, 14, 15 Pin 4	P_{OH}	50 100	mW
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (All voltages referenced to $V_{SS} = 0$, $T_A = 0$ to 70°C)

Characteristics	Symbol	Min.	Max.	Unit
DC Supply Voltage	V_{DD}	4.5	16	V
Input Voltage	V_{IL}		0.8	V
	V_{IH}	4 3.5		V
Input Current	I_{IN}		± 1	μA
VCR, Output, open drain	I_{OH}		± 1	μA
	I_{OL}	0.2 1		mA
Outputs a,b,c,d,e,f,g	I_{OH}	-7.5 -7.5	-11.5 -11.5	mA
	I_{OL}	0.1 0.5		mA
Output h + i	I_{OH}	-15 -15	-23 -23	mA
	I_{OL}	0.2 1.0		mA

INPUT/OUTPUT FUNCTIONS

SEGMENT DRIVER (a, b, c, d, e, f, g, h, i; Pins 1, 2, 3, 4, 12, 13, 14, 15).

The segment drivers are emitter-follower NPN-transistors. To limit the output current, a resistor typically 290 ohms is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of $V_{DD} = 5.0$ volts.

OUTPUT \overline{VCR} (Pin 11)

This output is activated (goes to low) whenever the address corresponding to program 16 is selected. Otherwise the output is open. See the truth table.

INPUT LATCH (A, B, C, D; Pins 5, 6, 8, 10)

The block diagram is shown on page 1. The inputs A, B, C and D are fed to a 4-bit latch which is controlled by clock (CL). Two modes of operation are available.

CLOCK (CL; Pin 7)

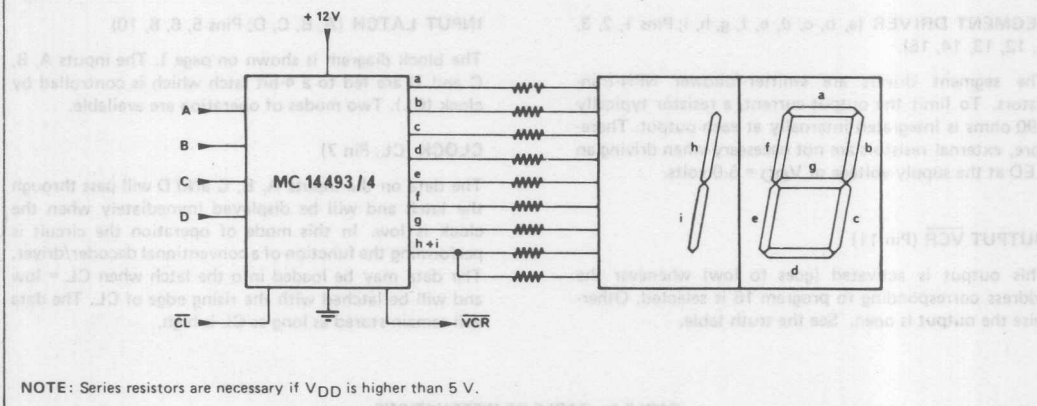
The data on the inputs A, B, C and D will pass through the latch and will be displayed immediately when the clock is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when CL = low and will be latched with the rising edge of CL. The data will remain stored as long as CL is high.

TABLE 1 — TABLE OF INSTRUCTIONS

14493 TRUTH TABLE											
A	B	C	D	a	b	c	d	e	f	g	h+i
0	0	0	0	0	1	1	0	0	0	0	0
1	0	0	0	1	1	0	1	1	0	1	0
0	1	0	0	1	1	1	1	0	0	1	0
1	1	0	0	0	1	1	0	0	1	1	0
0	0	1	0	1	0	1	1	0	1	1	0
1	0	1	0	1	0	1	1	1	1	1	0
0	1	1	0	1	1	1	0	0	0	0	0
1	1	1	0	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	0	1	1	0	1
1	0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	0	1	1	0	0	0	0	1
1	1	0	1	1	1	0	1	1	0	1	1
0	0	1	1	1	1	1	0	0	1	1	1
1	0	1	1	0	1	1	0	0	1	1	1
0	1	1	1	1	0	1	1	0	1	1	1
1	1	1	1	1	0	1	1	1	1	1	1

14494 TRUTH TABLE											
A	B	C	D	a	b	c	d	e	f	g	h+i
0	0	0	0	1	0	1	1	1	1	1	1
1	0	0	0	0	1	1	0	0	0	0	0
0	1	0	0	1	1	0	1	1	0	1	0
1	1	0	0	1	1	1	1	0	0	1	0
0	0	1	0	0	1	1	0	0	1	1	0
1	0	1	0	1	0	1	1	0	1	1	0
0	1	1	0	1	0	1	1	1	1	1	0
1	1	1	0	1	1	1	0	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	0
1	0	0	1	1	1	1	0	1	1	0	1
0	1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	0	1	1	0	0	0	0	1
0	0	1	1	1	1	0	1	1	0	1	1
1	0	1	1	1	1	1	1	0	0	1	1
0	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	1	0	1	1	0	1	1	1

FIGURE 2 — TYPICAL CONFIGURATION



TRUTH TABLE									
A	B	C	D	CL	VCR	Display	Output	Output	Output
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0

TRUTH TABLE									
A	B	C	D	CL	VCR	Display	Output	Output	Output
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0

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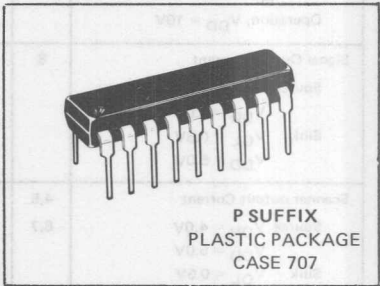
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MC 14497P

CMOS

PCM REMOTE CONTROL TRANSMITTER

**P SUFFIX
PLASTIC PACKAGE
CASE 707**



PCM REMOTE CONTROL TRANSMITTER

The MC 14497 is a PCM remote control transmitter realised in CMOS technology. Using a dual-single (AM/FSK) frequency biphasic modulation the transmitter is designed to work with the MC 6203 and MC 6215 receivers.

- Both AM/FSK modulation selectable
- 62 channels — up to 62 keys
- 500kHz reference oscillator controlled by inexpensive ceramic resonator
- Very low duty cycle
- Very low standby current
- Infrared transmission
- Selectable Start-Bit polarity (AM only)
- Shifted key mode available

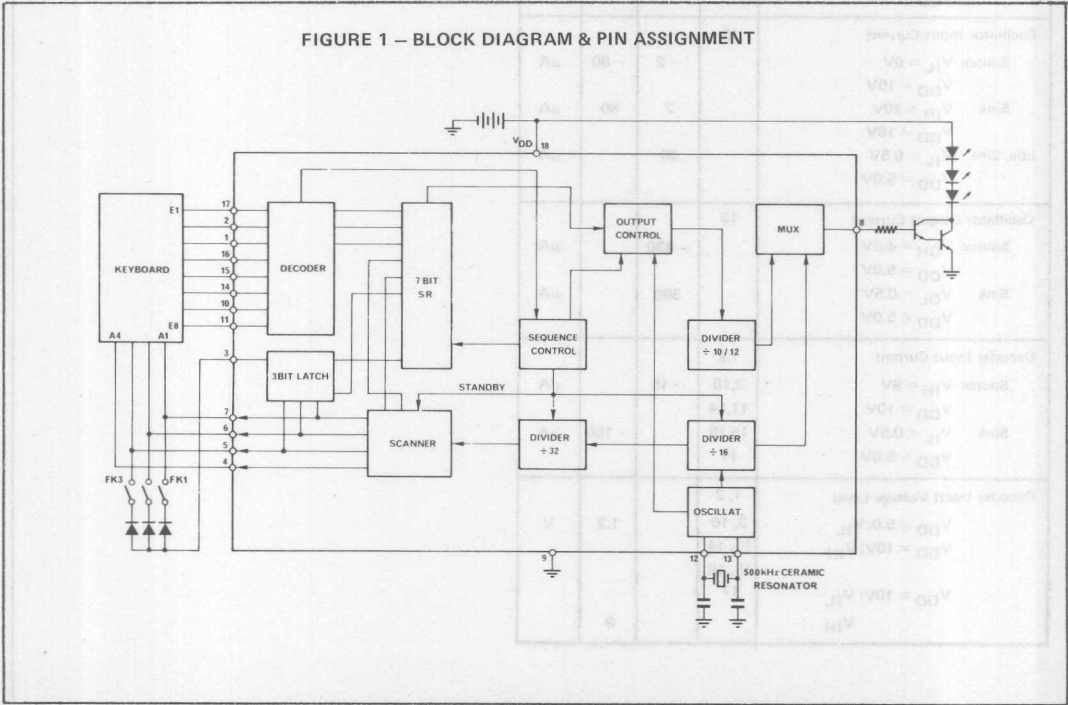
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- Both AM/FSK modulation selectable
 - 62 channels — up to 62 keys
 - 500kHz reference oscillator controlled by inexpensive ceramic resonator
 - Very low duty cycle
 - Very low standby current
 - Infrared transmission
 - Selectable Start-Bit polarity (AM only)
 - Shifted key mode available

FIGURE 1 — BLOCK DIAGRAM & PIN ASSIGNMENT



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+15 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

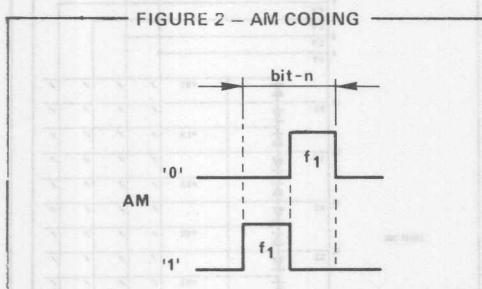
ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C)

Characteristics	Pin	Min	Max	Unit
Supply voltage	18	5.0	10.0	V DC
Supply Current	18			
Idle, $V_{dd} = 10\text{V}$			50	μA
Operation, $V_{DD} = 10\text{V}$			5	mA
Signal Output Current	8			
Source $V_{OH} = 4.0\text{V}$ $V_{DD} = 5.0\text{V}$		-1.0		mA
Sink $V_{OL} = 0.5\text{V}$ $V_{DD} = 5.0\text{V}$			200	μA
Scanner output Current	4,5 6,7			
Source $V_{OH} = 4.0\text{V}$ $V_{DD} = 5.0\text{V}$		-50		μA
Sink $V_{OL} = 0.5\text{V}$ $V_{DD} = 5.0\text{V}$			380	μA
Oscillator Input Current	12			
Source $V_{IL} = 0\text{V}$ $V_{DD} = 10\text{V}$		-2	-80	μA
Sink $V_{IH} = 10\text{V}$ $V_{DD} = 10\text{V}$		2	80	μA
Idle, Sink $V_{IL} = 0.5\text{V}$ $V_{DD} = 5.0\text{V}$			30	μA
Oscillator Output Current	13			
Source $V_{OH} = 4.0\text{V}$ $V_{DD} = 5.0\text{V}$		-430		μA
Sink $V_{OL} = 0.5\text{V}$ $V_{DD} = 5.0\text{V}$			380	μA
Decoder Input Current	1,2 3,10 11,14 15,16 17			
Source $V_{IH} = 9\text{V}$ $V_{DD} = 10\text{V}$		-15		μA
Sink $V_{IL} = 0.5\text{V}$ $V_{DD} = 5.0\text{V}$			-150	μA
Decoder Input Voltage Level	1,2 3,10 11,14 15,16 17			
$V_{DD} = 5.0\text{V}; V_{IL}$			1.2	V
$V_{DD} = 10\text{V}; V_{IH}$				
$V_{DD} = 10\text{V}; V_{IL}$ V_{IH}			9	

CIRCUIT OPERATION

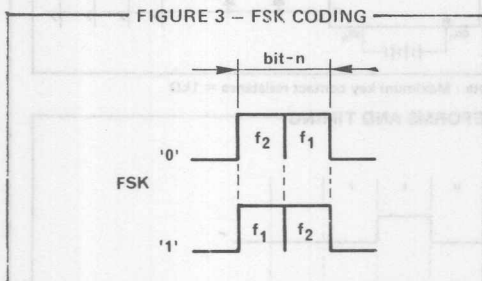
The transmitter emits a 6-bit, labelled A(LSB) to F(MSB), binary code giving a total of 64 possible combinations or code words. All of these are user selectable, except the last two - where channel 63 is not sent while channel 62 is automatically sent by the transmitter at the end of each transmission as an "End of Transmission" code.

In either mode, AM or FSK, the transmitted signal is in the form of a biphase pulse code modulation (PCM) signal. The AM coding is shown in figure 1.



Where f_1 is a train of pulses at the modulating frequency of 31.25 kHz for a reference frequency of 500 kHz.

In the FSK mode two modulating frequencies are used as shown in figure 3.



Where f_1 is 50 kHz and f_2 is 41.66 kHz for a reference frequency of 500 kHz.

The keyboard can be a simple switch matrix using no external diodes, connected between the four scanner outputs, A1 to A4, and the eight row inputs, E1 to E8. Under these conditions only the first 32 code words are available, bit-F is always at logical "0". However, a simple two-pole, changeover switch, in the manner of a typewriter "shift" key (switch FK3 in figure 1) can be used to change the polarity of bit-F to give access to the next full set of 32 instructions.

An alternative method of accessing more than 32 instructions is by the use of external diodes between the address

inputs, see figure 4. These have the effect of producing "phantom" address inputs by pulling two inputs low at the same time, which causes bit-F to go high, that is to logical "1". By interconnecting only certain address inputs it is possible to make an intermediate keyboard with between 32 and 64 keys.

The other two switches in figure 1, FK1 and FK2, change the modulation mode, a closure changes the modulation from FSK to AM, and the start-bit polarity, a closure changes the start-bit to a logical "0", respectively.

The full range of options available is illustrated in the table below:

	Start-bit	Modulation	bit-F	Channels
E9 - open	1	FSK	0	0 - 31
E9 - A1 (FK1)	1	AM	0	0 - 31
E9 - A2 (FK2)	0	FSK	0	0 - 31*
E9 - A3 (FK3)	1	FSK	1	32 - 61
E9 - A1 + A2	0	AM	0	0 - 31
E9 - A1 + A3	1	AM	1	32 - 61
E9 - A2 + A3	0	FSK	1	32 - 61*
E9 - A1 + A2 + A3	0	AM	1	32 - 61

* = Not allowed.

One of the transmitter's major features is its low power consumption - in the order of $10\mu\text{A}$ in the idle state. For this reason the battery is perpetually in circuit. It has in fact been found that a light discharge current is beneficial to battery life.

In its active state the transmitter efficiency is increased by the use of a low duty cycle, less than 2.5% for the modulating pulse trains.

While no key is pressed the circuit is in its idle state, the reference oscillator is topped and the eight address input lines are held high through internal pull-up resistors.

As soon as a key is pressed this takes the appropriate address line low, signalling to the circuit that a key has been selected. The oscillator is now enabled. If the key is released before the code word has been sent the circuit returns to its idle state. To account for accidental activation of the transmitter the circuit has a built-in reaction time of some 20ms, which also overcomes contact bounce. After this delay the code word will be sent and repeated at 90ms intervals for as long as the key is pressed. As soon as the key is released the circuit automatically sends channel 62, the "End of Transmission" (EOT) code. The transmitter then returns to its idle state.

The differences between the two modulation modes are illustrated in figure 5. However it should be noted that:

In the AM mode each transmitted word is preceded by a burst of pulses lasting $512\mu\text{s}$. This is used to set up the AGC loop in the receiver's preamp. In the FSK mode the first frequency of the first bit is extended by 1.5ms and the AGC burst is suppressed. In either mode it is assumed that the normal start-bit is present.

INPUT/OUTPUT FUNCTIONS

Row Inputs E1 to E8 (Pins 1, 2, 10, 11, 14, 16 & 17). Under idle conditions these inputs are held high, by internal pull-up resistors. As soon as a key is pressed a logical "0" on that particular line signals to the circuit that a key has been selected. After a delay of 20ms the internal register is loaded with the code word for the key selected.

Row Input E9 (Pin 3). This is a special programming input and when connected to the appropriate scanner output, via a diode, it will modify the transmitted output according to the table in the previous section.

In that table the figures in brackets, FK1 etc. refer to the switches shown in figures 1 and 4. If only one option is required the diode may be omitted. The connections shown in the table may be made in any combination.

Although E9 is a row input forcing this line low will not activate the circuit.

Scanner Outputs A1 to A4 (Pins 4, 5, 6 & 7). Under idle condition these outputs are held low, logical "0". When oscillator will start and release the outputs.

Oscillator (Pins 12 & 13). This is designed to operate with a 500kHz ceramic resonator or a tuned LC circuit.

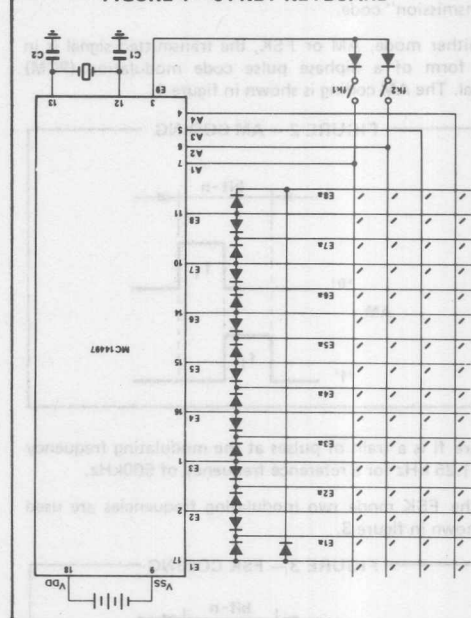
It is important that a ceramic resonator and *not* a filter is used here as the oscillator frequency can not be guaranteed if a ceramic filter is used.

Signal Out (Pin 8). This output provides the modulating signal ready to drive the modulation amplifier.

If required the transmitter can be used as a keyboard encoder for direct use with a receiver. In this case the

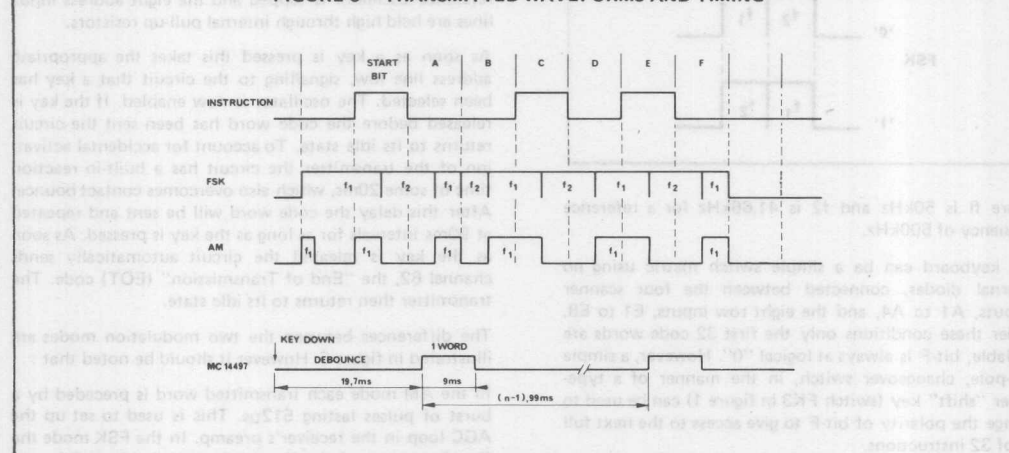
AM option is selected, the output inverted and fed directly to the receiver's signal input pin.

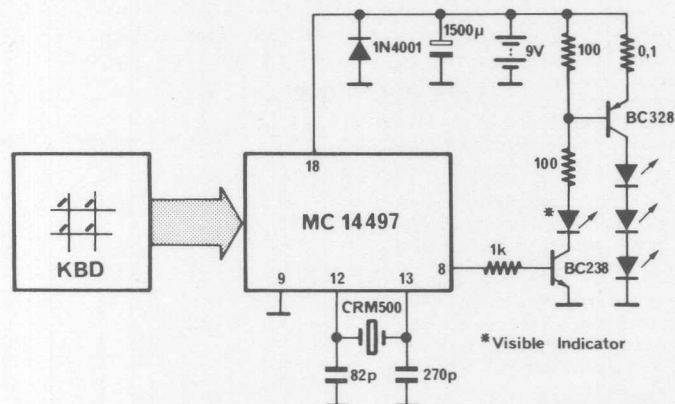
FIGURE 4 - 64-KEY KEYBOARD



Note : Maximum key contact resistance = 1k Ω

FIGURE 5 - TRANSMITTED WAVEFORMS AND TIMING



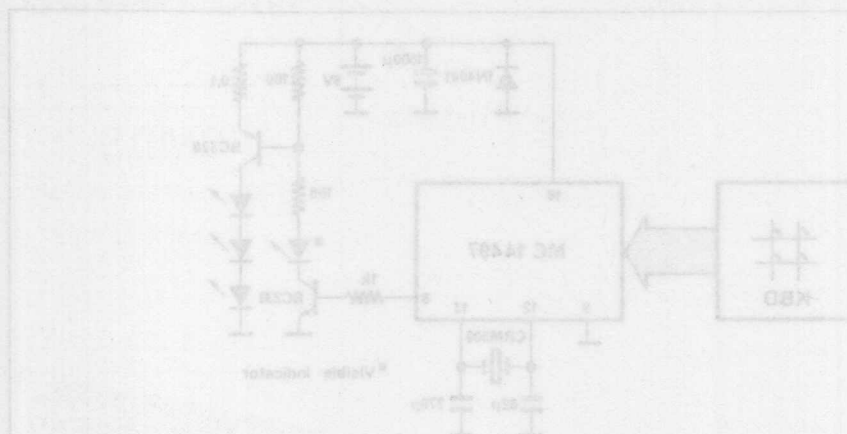


TYPICAL APPLICATION CIRCUIT

TABLE 1 – TRANSMITTED CODES

Channel	Code word					Keyboard		Channel	Code word					Keyboard	
	F	E	D	C	B	A	In Out		F	E	D	C	B	A	In Out
0	0	0	0	0	0	0	E8 A4	32	1	0	0	0	0	0	E8a A4
1		0	0	1			E1 A4	33		0	0	1			E1a A4
2			0	1	0		E2 A4	34			0	1	0		E2a A4
3			0	1	1		E3 A4	35			0	1	1		E3a A4
4			1	0	0		E4 A4	36			1	0	0		E4a A4
5			1	0	1		E5 A4	37			1	0	1		E5a A4
6			1	1	0		E6 A4	38			1	1	0		E6a A4
7			1	1	1		E7 A4	39			1	1	1		E7a A4
8	0	0	1	0	0	0	E8 A1	40	1	0	1	0	0	0	E8a A1
9		0	0	1			E1 A1	41		0	0	1			E1a A1
10		0	1	0			E2 A1	42		0	1	0			E2a A1
11		0	1	1			E3 A1	43		0	1	1			E3a A1
12		1	0	0			E4 A1	44		1	0	0			E4a A1
13		1	0	1			E5 A1	45		1	0	1			E5a A1
14		1	1	0			E6 A1	46		1	1	0			E6a A1
15		1	1	1			E7 A1	47		1	1	1			E7a A1
16	0	1	0	0	0	0	E8 A3	48	1	1	0	0	0	0	E8a A3
17		0	0	1			E1 A3	49		0	0	1			E1a A3
18		0	1	0			E2 A3	50		0	1	0			E2a A3
19		0	1	1			E3 A3	51		0	1	1			E3a A3
20		1	0	0			E4 A3	52		1	0	0			E4a A3
21		1	0	1			E5 A3	53		1	0	1			E5a A3
22		1	1	0			E6 A3	54		1	1	0			E6a A3
23		1	1	1			E7 A3	55		1	1	1			E7a A3
24	0	1	1	0	0	0	E8 A2	56	1	1	1	0	0	0	E8a A2
25		0	0	1			E1 A2	57		0	0	1			E1a A2
26		0	1	0			E2 A2	58		0	1	0			E2a A2
27		0	1	1			E3 A2	59		0	1	1			E3a A2
28		1	0	0			E4 A2	60		1	0	0			E4a A2
29		1	0	1			E5 A2	61		1	0	1			E5a A2
30		1	1	0			E6 A2	62 (EOT)		1	1	0			E6a A2
31	0	1	1	1	1	1	E7 A2	Not transmitted	1	1	1	1	1	1	E7a A2

NOTE: Although the 'a' suffix applies to a 'phantom' input when using a keyboard with up to 64 keys the coding for a shifted key, up to 32 keys, model, with FK3 closed, is identical.

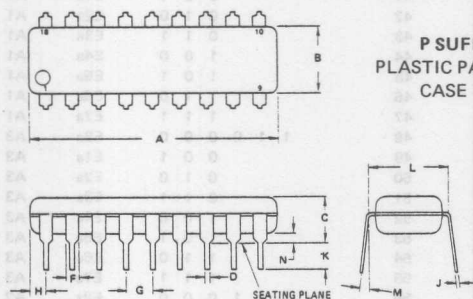


TYPICAL APPLICATION CIRCUIT

TABLE 1 - TRANSMITTED CODES

Channel	Code word	Keycode	Channel	Code word	Keycode
1	2	3	4	5	6
1	0 0 0 0 0	00	16	0 0 1 0 0	00
2	0 0 1 0 0	01	17	0 0 1 0 1	01
3	0 1 0 0 0	02	18	0 1 0 0 1	02
4	0 1 1 0 0	03	19	0 1 1 0 1	03
5	1 0 0 0 0	04	20	1 0 0 0 1	04
6	1 0 1 0 0	05	21	1 0 1 0 1	05
7	1 0 1 0 1	06	22	1 0 1 1 0	06
8	1 1 0 0 0	07	23	1 1 0 0 1	07
9	1 1 0 0 1	08	24	1 1 0 1 0	08
10	1 1 1 0 0	09	25	1 1 1 0 1	09
11	1 1 1 0 1	10	26	1 1 1 1 0	10
12	1 1 1 1 0	11	27	1 1 1 1 1	11
13	1 1 1 1 1	12	28	1 1 1 1 1	12
14	1 1 1 1 1	13	29	1 1 1 1 1	13
15	1 1 1 1 1	14	30	1 1 1 1 1	14

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 707

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.60	7.11	0.260	0.280
C	4.06	4.57	0.160	0.180
D	0.35	0.51	0.014	0.020
E	1.02	1.52	0.040	0.060
F	2.41	2.67	0.095	0.105
G	1.14	1.40	0.045	0.055
H	0.20	0.20	0.008	0.012
J	3.05	3.56	0.120	0.140
K	7.37	7.87	0.290	0.310
L	0.0	10.0	0.0	10.0
M	0.51	1.02	0.020	0.040
N	0.51	1.02	0.020	0.040

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MC 14499

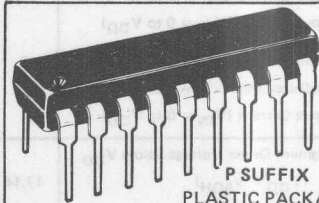
CMOS

7-SEGMENT LED DISPLAY DECODER/DRIVER

7-SEGMENT LED DISPLAY DECODER/DRIVER

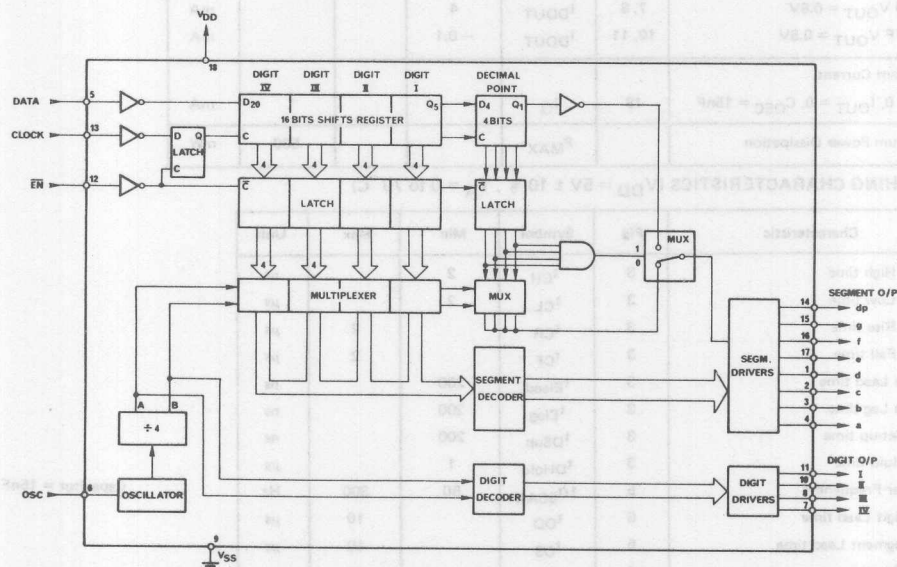
The MC 14499 is a 7-segment alphanumeric LED decoder/driver for use in conjunction with microprocessor (MPU) systems. It is able to drive directly 4 digit displays.

- High current segment drivers on-chip
- MPU compatible input levels
- Very few external components required



P SUFFIX
PLASTIC PACKAGE
CASE 707

FIGURE 1 – BLOCK DIAGRAM AND PINOUT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +7.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	18	V_{DD}	4.5		6.5	Vdc
Input Level - low	5, 13	V_{IL}			$0.3XV_{DD}$	Vdc
Input Level - high	12	V_{IH}	$0.7XV_{DD}$			Vdc
Input Current ($V_{IN} = 0$ to V_{DD})		I_{in}			1	μA
Oscillator Input - High Level	6	V_{ILO}			$0.2V_{DD}$	Vdc
Oscillator Input - Low Level		V_{IHO}	$0.8V_{DD}$			Vdc
Input Current ($V_{IN} = 0$ to V_{DD})		I_{INO}	-100		100	μA
Segment Driver Voltage below V_{DD} ($V_{DD} - V_{SOH}$)	17, 14					
$I_{OUT} = 50\text{mA}$	1, 2,				1.0	Vdc
$I_{OUT} = 10\text{mA}$	3, 4				0.8	Vdc
Leakage $V_{OUT} = 0$	15, 16	I_{OFF}			0.5	mA
Digit Drivers						
ON $V_{OUT} = 0.8\text{V}$	7, 8	I_{DOUT}	4			mA
OFF $V_{OUT} = 0.5\text{V}$	10, 11	I_{DOUT}	-0.1			mA
Quiescent Current $V_{IN} = 0$, $I_{OUT} = 0$, $C_{OSC} = 15\text{nF}$	18	I_Q			1	mA
Maximum Power Dissipation		P_{MAX}			500	mW

SWITCHING CHARACTERISTICS ($V_{DD} = 5\text{V} \pm 10\%$, $T_A = 0$ to 70°C)

Characteristic	Fig	Symbol	Min	Max	Unit
Clock High time	3	t_{CH}	2		μs
Clock Low time	3	t_{CL}	2		μs
Clock Rise time	3	t_{CR}		2	μs
Clock Fall time	3	t_{CF}		2	μs
Enable Lead time	3	t_{Elead}	200		ns
Enable Lag time	3	t_{Elag}	200		ns
Data Set-up time	3	t_{DSup}	200		ns
Data Hold time	3	t_{DHold}	1		μs
Scanner Frequency ¹	5	$1/t_{SCAN}$	50	300	Hz
Osc/Digit Lead time	5	t_{OD}		10	μs
Osc/Segment Lead time	5	t_{OS}		10	μs
Digit Overlap	5	t_{OV}		5	μs

Capacitor = 15nF

CIRCUIT OPERATION

The circuit accepts a 20-bit input, 16-bits for the four digit display plus 4-bits for the decimal point — these latter four-bits are optional.

The input sequence is the decimal point code followed by the four digits, as shown in figure 2.

In order to enter data the enable input, \overline{EN} , must be low, = 0. The sample and shift are accomplished on the falling clock edge, see figure 3. Data are loaded from the shift register to the latches when \overline{EN} goes high, = 1. While the shift register is being loaded the previous data are stored in the latches.

If the decimal point is used the system requires 20 clock pulses to load data, otherwise only 16 are required.

Cascading

The circuit may be cascaded in the following manner.

If a 1111 word is loaded into the decimal point latch, the output of the shift register is switched to the decimal point driver, see figure 4. Therefore, to cascade n four digit display drivers a set-up is used which will firstly load the 1111 cascading word :

- 1 $\overline{EN} = 0$
- 2 Load 20-bits, the first four bits being 1, with 20 clock pulses.
- 3 $\overline{EN} = 1$, to load the latch
- 4 Repeat steps 1 to 3 (n-1) times
- 5 (nX20)-bits can be loaded into n circuits, with 1111 as decimal point word to continue the cascading.

Scanner

The scanner frequency is determined by an on-chip oscillator, which requires an external frequency determining capacitor. The capacitor voltage varies between two trigger levels at the oscillator frequency.

An external oscillator signal can be used, within the recommended operating range of 200 to 800Hz — to avoid flicker and digit overlap. For test purposes this frequency can be increased up to 10kHz.

A divide by four counter provides four non-overlapping scanner waveforms corresponding to the four digits — see figure 5.

Segment decoder

The code used in this matrix decoder is shown in figure 6, other codes can be used with a single mask change.

Output drivers

There are two different drivers :

The segment and decimal point drivers; these are NPN emitter followers with no current limiting devices.

The digit output buffers; These are short circuit protected NPN devices.

A typical application circuit is shown in figure 7.

FIGURE 2 — INPUT SEQUENCE

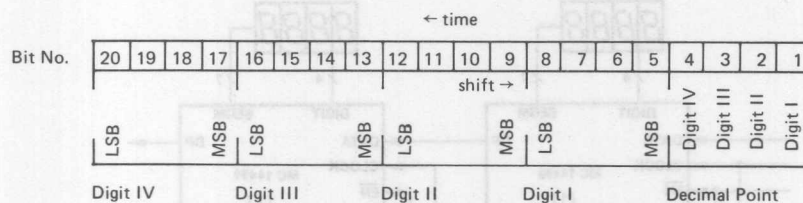


FIGURE 3a — SERIAL INPUT, POSITIVE CLOCK

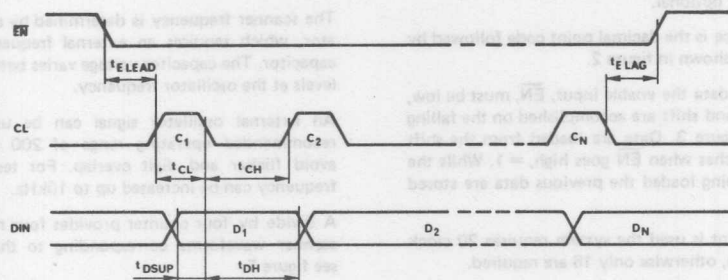


FIGURE 3b — SERIAL INPUT, NEGATIVE CLOCK

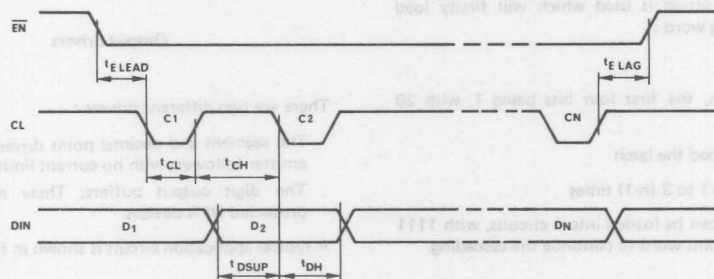


FIGURE 4 — CASCADING MC 14499s

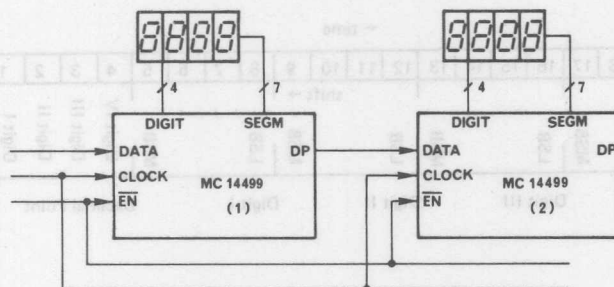


FIGURE 5 — SCANNER WAVEFORMS

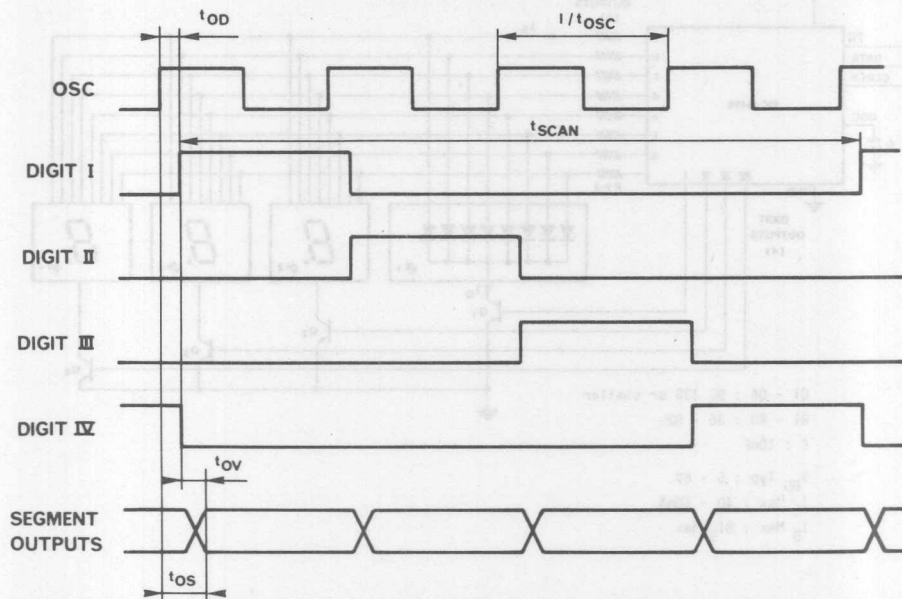
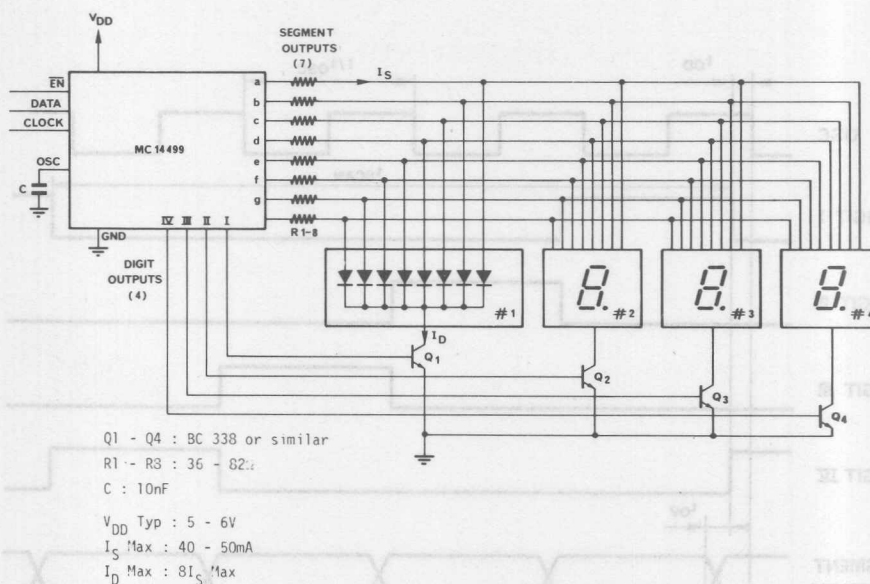


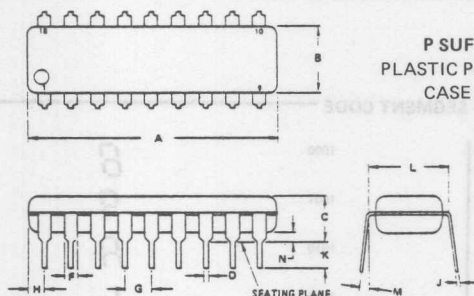
FIGURE 6 — SEGMENT CODE

0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	I
0100	4	1100	11
0101	5	1101	U
0110	6	1110	dash
0111	7	1111	blank

FIGURE 7 — APPLICATION EXAMPLE



OUTLINE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.74	0.875	0.915
B	5.50	7.11	0.260	0.280
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.014	0.020
F	1.01	1.52	0.040	0.060
G	2.41	2.57	0.095	0.105
H	1.14	1.40	0.045	0.055
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	1.27	1.57	0.050	0.060
M	0.51	0.60	0.020	0.024
N	0.51	0.60	0.020	0.024

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MC144100

ADVANCE INFORMATION

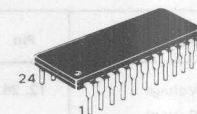
DUPLEX MODE 32-SEGMENT LED DRIVER

The MC144100 is a 32-bit serial data input to 32-segment LED driver realised in CMOS technology, designed for use in AC mains powered applications. The use of the 50/60Hz mains to provide the two phase multiplexing ensures minimal radio frequency interference (RFI).

- Minimal RFI from two phase sine wave multiplex driver
- Suitable for radio/clock applications
- Cascadable
- On-chip bipolar NPN drivers
- No on-chip decoder—for greater flexibility

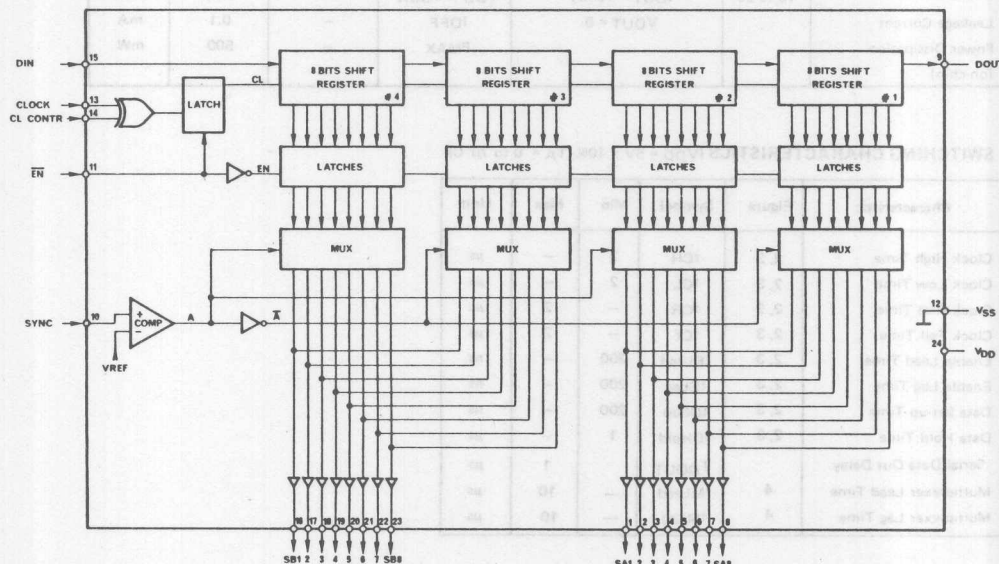
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

DUPLEX MODE
32-SEGMENT LED DRIVER



P SUFFIX
PLASTIC PACKAGE
CASE 709

FIGURE 1 — MC144100 BLOCK DIAGRAM AND PINOUT



MC144100

MAXIMUM RATINGS (Voltages referred to VSS, pin 12)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to 6.5	V DC
Input Voltage, All Inputs	VIN	-0.5 to VDD + 0.5	V DC
DC Current Drain per Input Pin	I	10	mA
DC Current Drain per Output Pin	I	50	mA
Output Voltage, Segment Output	VSOFF	VSS - 0.5 to VDD + 0.5	V DC
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	TSTG	-65 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \leq V_{IN}$ or $V_{OUT} \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

ELECTRICAL CHARACTERISTICS (TA = 0 to 70°C)

Characteristic	Pin	Condition	Symbol	Min	Max	Unit
Supply Voltage	12, 24		VDD	3.0	6.0	V DC
Supply Current			IDD	—	1.0	mA
Input Voltage High	15, 13	VIN = 0, IOUT = 0	VIH	0.7 X VDD	—	V DC
Input Voltage Low	14, 11		VIL	—	0.3 X VDD	V DC
Input Current		VIN = 0 to VDD	IIN	—	1	μA
Input Voltage High	10		VIHS	VDD - 0.5	—	V DC
Input Voltage Low			VILS	—	VDD - 2	V DC
Input Current		VIN = 0 to VDD	IINS	—	10	μA
Output Drive Capability	9	VOL = 0.5V VOH = VDD - 0.5V	IOL IOH	200 -200	— —	μA μA
Voltage Drop	1 to 8 16 to 23	IOUT = 30mA, VDD ≥ 5V IOUT = 10mA	VDD - VSOH VDD - VSOH	— —	1.2 0.75	V DC V DC
Leakage Current		VOUT = 0	IOFF	—	0.1	mA
Power Dissipation (on-chip)			PMAX	—	500	mW

SWITCHING CHARACTERISTICS (VDD = 5V ± 10%, TA = 0 to 70°C)

Characteristic	Figure	Symbol	Min	Max	Unit
Clock High Time	2, 3	tCH	2	—	μs
Clock Low Time	2, 3	tCL	2	—	μs
Clock Rise Time	2, 3	tCR	—	2	μs
Clock Fall Time	2, 3	tCF	—	2	μs
Enable Lead Time	2, 3	tELead	200	—	ns
Enable Lag Time	2, 3	tELag	200	—	ns
Data Set-up Time	2, 3	tDSup	200	—	ns
Data Hold Time	2, 3	tDHold	1	—	μs
Serial Data Out Delay		TDOUT		1	μs
Multiplexer Lead Time	4	tMLead	—	10	μs
Multiplexer Lag Time	4	tMLag	—	10	μs

CIRCUIT OPERATION

The circuit operation can be followed by reference to the block diagram Figure 1.

Data are fed serially into the circuit via the data input pin DIN, which is controlled by the CLOCK and chip enable, \overline{EN} , pins—this latter enables the circuit when it is low i.e. at logical '0'. When \overline{EN} goes high, to logical '1', the clock idle state is stored in a latch; thus permitting the use of a positive or negative going clock.

Four 8-bit words are loaded into a 32-bit shift register, made up of four 8-bit registers, when \overline{EN} is low. At the next rising edge of \overline{EN} the data in the shift register are loaded into latches.

The shift in the register takes place on the falling edge of the clock when the clock control input, CLCONTR, is low, logical '0'. Conversely, when CLCONTR is high, logical '1', the shift takes place on the clock's rising edge. See Figures 2 and 3.

Word number 1 is the first shifted and number 4 the last.

The output DOUT serves as a cascading output.

Multiplexing is controlled by the SYNC input whose switching threshold occurs just before the LED segments are turned on. A current limiting resistor is necessary for this input if the control signal swings outside the limits of $V_{DD} + 0.5V$ to $V_{SS} - 0.5V$.

The relationship between the SYNC input and the displayed word is shown in the table below:

TABLE 1

Segments	SYNC	Word
SA1 – SA8	low	1
SA1 – SA8	high	2
SB1 – SB8	low	3
SB1 – SB8	high	4

Because decoding is a function of an external circuit, for example the microprocessor in a radio synthesizer application, there is no decoding circuitry in this device.

INPUT/OUTPUT FUNCTIONS

DIN — (pin 15) This is the serial data input pin.

DOUT — (pin 9) This is the cascading output. If desired this pin can be tied directly to the DIN pin (pin 15) of a further MC144100 for cascading purposes.

CLOCK — (pin 13) This is the clock input and is able to accept a clock frequency of up to 250kHz.

CLCONTR — (pin 14) The state of this pin determines whether the data are shifted on the rising edge, CLCONTR = logical '1', or on the falling edge, CLCONTR = logical '0', of the clock signal.

\overline{EN} — (pin 11) This is the chip enable pin and is active

when low, logical '0'. When high it causes the clock idle state, at the time of the positive going transition, to be stored in a latch.

SYNC — (pin 10) The status of this input determines which of the four input words are displayed. See Table 1. If the control signal applied to this pin goes more positive than $V_{DD} + 0.5V$ or more negative than $V_{SS} - 0.5V$ an external current limiting resistor will be necessary.

OUTPUT DRIVERS — (pins 1 to 8 & 16 to 23) These are on-chip NPN emitter followers each requiring an external current limiting resistor. In the off state they are protected against voltages down to $V_{SS} - 6V$.

FIGURE 2 – TIMING DIAGRAM—CLCONTR HIGH

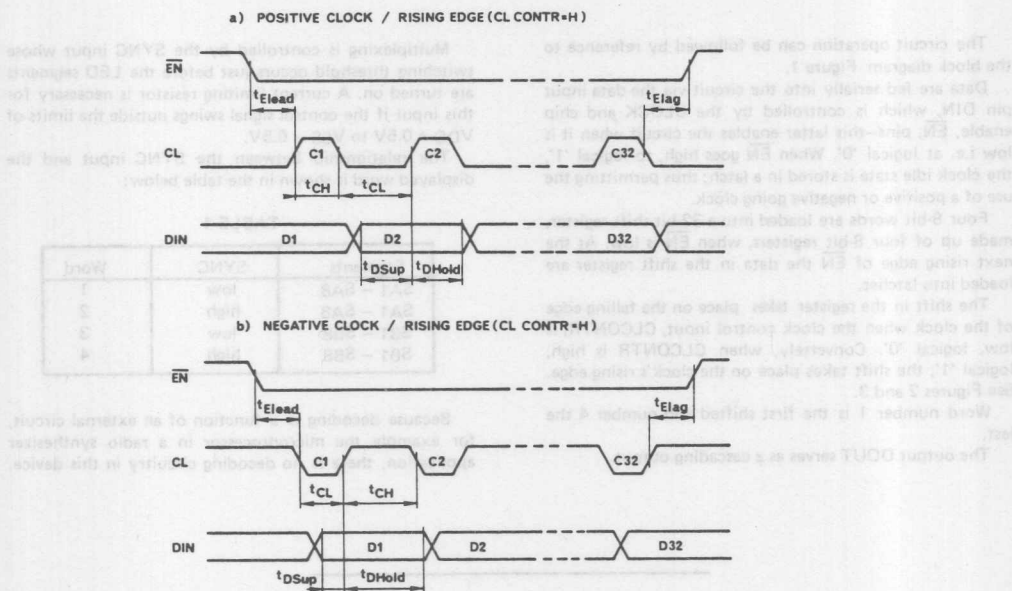


FIGURE 3 – TIMING DIAGRAM—CLCONTR LOW

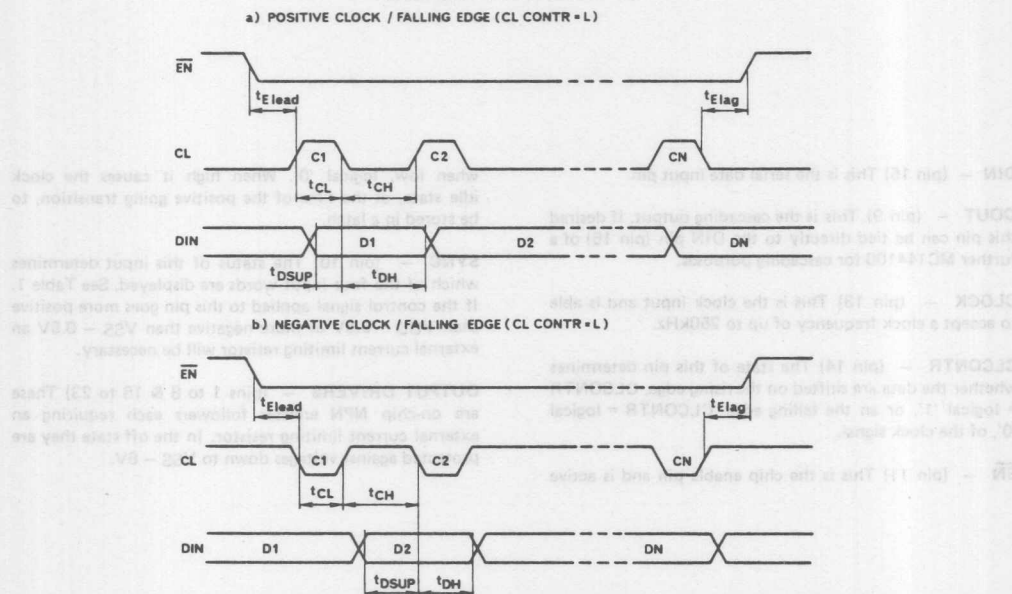


FIGURE 4 – SEGMENT CHANGE DELAY

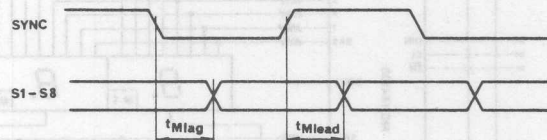


FIGURE 5 – SEGMENT TURN-ON/TURN-OFF

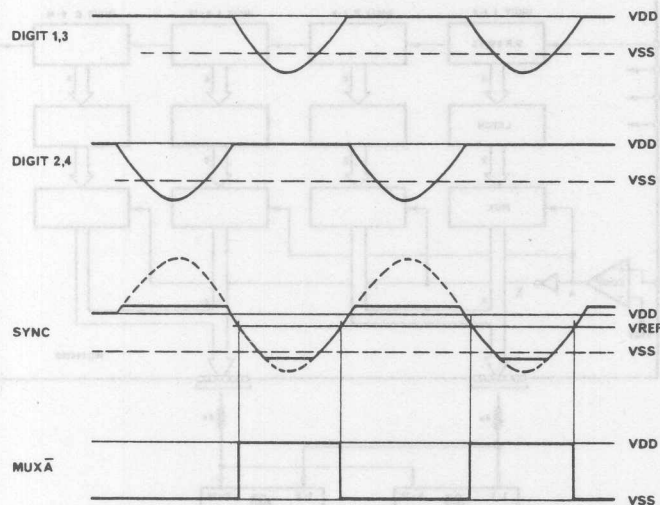
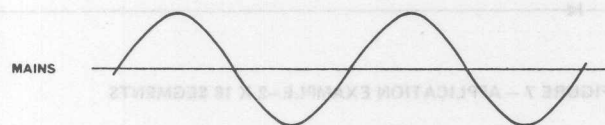


FIGURE 6 – APPLICATION EXAMPLE—4 X 8 SEGMENTS

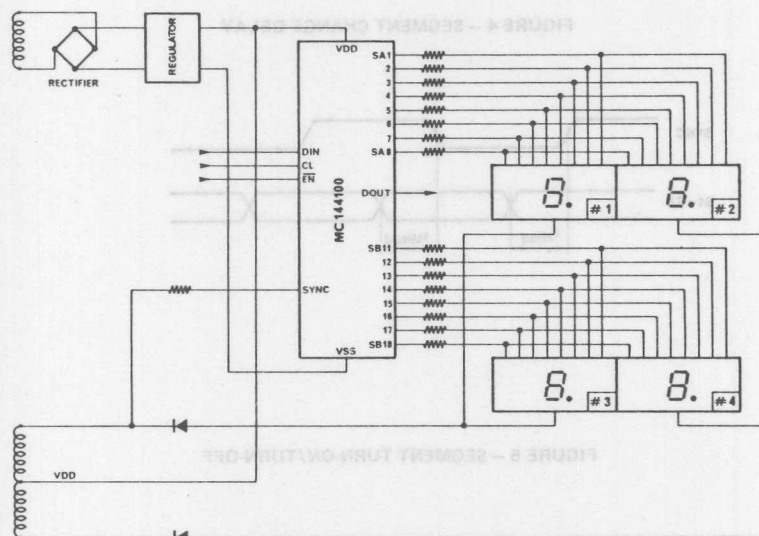
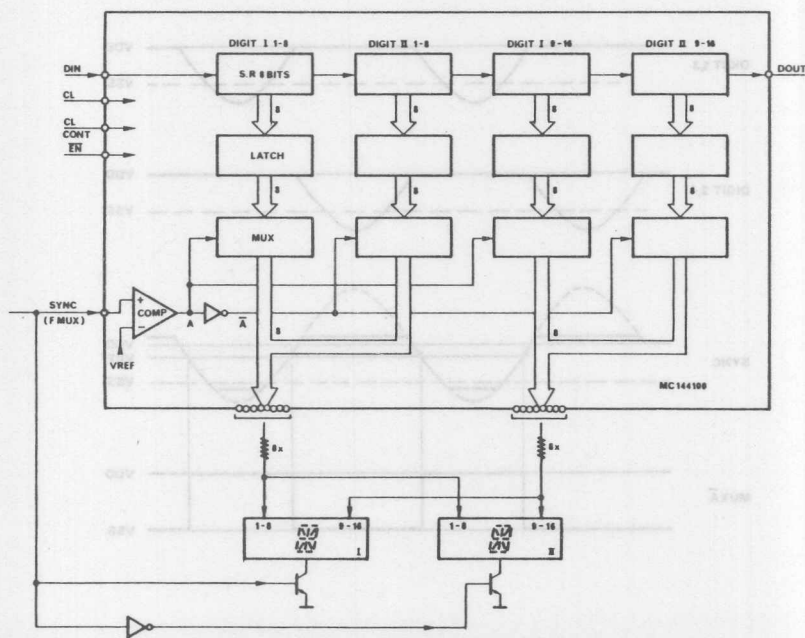


FIGURE 7 – APPLICATION EXAMPLE—2 X 16 SEGMENTS

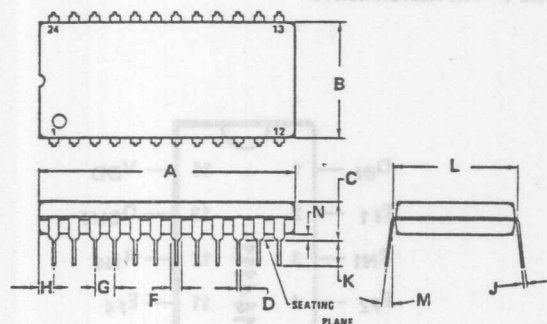


MECHANICAL OUTLINES

CASE 709-02

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. 709-01 OBSOLETE, NEW STD 709-02.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24	BSC	0.600	BSC
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

MC144110/1

Advance Information

QUAD & HEX D/A CONVERTERS

The MC 144110 and MC 144111 are hex and quad static, D/A converters realised in CMOS technology. Each converter, featuring 6-bit resolution, consists of a 6-bit shift register, 6-bit latch and a static D/A converter.

- 4/6 direct R-2R network outputs
- 4/6 emitter follower outputs
- MPU compatible input levels
- Serial data input
- Data cascade output
- Wide operating voltage range of 4.5 to 15 Vdc

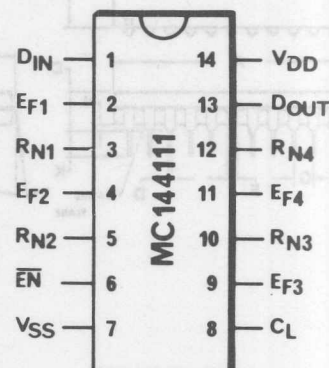
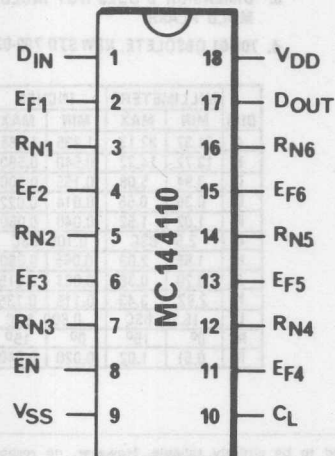
CMOS

QUAD & HEX D/A CONVERTERS

MC 144110
P SUFFIX
PLASTIC PACKAGE
CASE 707-02

MC 144111
PLASTIC PACKAGE
CASE 646 (TO-116)

FIGURE 1 – PIN ASSIGNMENTS



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
Input Current, All Inputs	I_{in}	10	mA
Operating Temperature Range	T_A	0 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

SWITCHING CHARACTERISTICS ($T_A = 0 \dots 85^\circ\text{C}$)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Clock high time	$V_{DD} = 5\text{V}$	t_{CH}	2	0.2		μs
	$V_{DD} = 10\text{V}$		1.5			μs
	$V_{DD} = 15\text{V}$		1	0.1		μs
Clock low time	$V_{DD} = 5\text{V}$	t_{CL}	5	1.5		μs
	$V_{DD} = 10\text{V}$		3.5			μs
	$V_{DD} = 15\text{V}$		2	0.5		μs
Enable lead time	$V_{DD} = 5\text{V}$	t_{Elead}	5	1.5		μs
	$V_{DD} = 10\text{V}$		3.5			μs
	$V_{DD} = 15\text{V}$		2	0.5		μs
Enable lag time	$V_{DD} = 5\text{V}$	t_{Elag}	5	1.5		μs
	$V_{DD} = 10\text{V}$		3.5			μs
	$V_{DD} = 15\text{V}$		2	0.5		μs
Data Set-up time	$V_{DD} = 5\text{V}$	t_{Dsup}	1	0.1		μs
	$V_{DD} = 10\text{V}$		0.75			μs
	$V_{DD} = 15\text{V}$		0.5	0		μs
Data Hold time	$V_{DD} = 5\text{V}$	t_{Dhold}	5	1.5		μs
	$V_{DD} = 10\text{V}$		3.5			μs
	$V_{DD} = 15\text{V}$		2	0.5		μs
Clock rise time		t_{Crise}			2	μs
Clock fall time		t_{Cfall}			2	μs

ELECTRICAL CHARACTERISTICS ($T_A = 0 - 85^\circ\text{C}$, $V_{DD} = 4.5 - 15\text{V}$)

Characteristic	Pin ¹	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	18	V_{DD}	4.5		15	V DC
DC Supply Current	MC 144110 MC 144111	I_{DD}			12 8	mA DC mA DC
Input low level	1	D_{IN}			0.8	V
High level	(1)		3.0			V
			3.5			V
			4.0			V
Current		I_{IN}			1	μA
Output Sink	$V_{OL} = 0.5\text{V}$	I_{OL}	200			μA
Source	$V_{OH} = V_{DD} - 0.5\text{V}$	I_{OH}	-200			μA
D/A Characteristics						
Network Resistance		R	7	10	15	k Ω
Precision	3, 5, 7, 12					
(w.c. at $V_{RN} = V_{DD}/2$)	$V_{DD} = 5\text{V}$	V_{NONL}		20	100	mV
	$V_{DD} = 10\text{V}$				200	mV
	$V_{DD} = 15\text{V}$			120	300	mV
Step Size			-75 %	$V_{DD}/64$	+75 %	
MC 144110						
NPN Emitter Follower Current Gain						
$I_E = 0.1 - 10\text{mA}$	2, 4, 6,	h_{fe}	40	100		
Emitter leakage Current $V_{RN} = 0\text{V}$	11, 13				10	μA
V_{BE} at $I_E = 1\text{mA}$		V_{BE}	0.4		0.7	V
Max Dissipation	15					
per output	$T_{Amax} = 85^\circ\text{C}$	P_E			10	mW
all 4 outputs		P_{Etot}			25	mW
per output	$T_{Amax} = 70^\circ\text{C}$	P_E			30	mW
all 4 outputs		P_{Etot}			100	mW
MC 144111						
NPN Emitter Follower Current Gain	2, 4, 9,					
$I_E = 0.1 - 10\text{mA}$	11	h_{fe}	40	100		
Emitter Leakage Current $V_{RN} = 0\text{V}$					10	μA
V_{BE} at $I_E = 1\text{mA}$		V_{BE}	0.4		0.7	V
Max Dissipation						
per output	$T_{Amax} = 85^\circ\text{C}$	P_E			20	mW
all 4 outputs		P_{Etot}			50	mW
per output	$T_{Amax} = 70^\circ\text{C}$	P_E			50	mW
all 4 outputs		P_{Etot}			150	mW

¹ Pin numbers in brackets () refer to MC 144111

FIGURE 2a – SERIAL INPUT, POSITIVE CLOCK

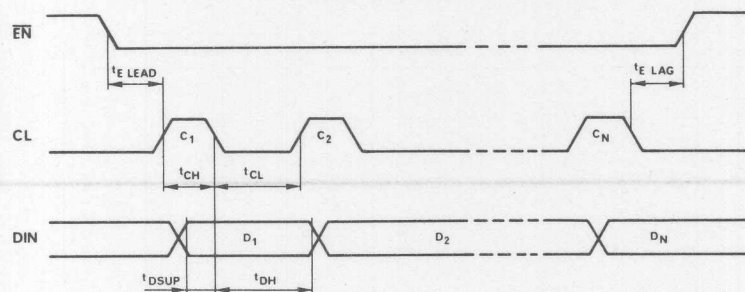


FIGURE 2b – SERIAL INPUT, NEGATIVE CLOCK

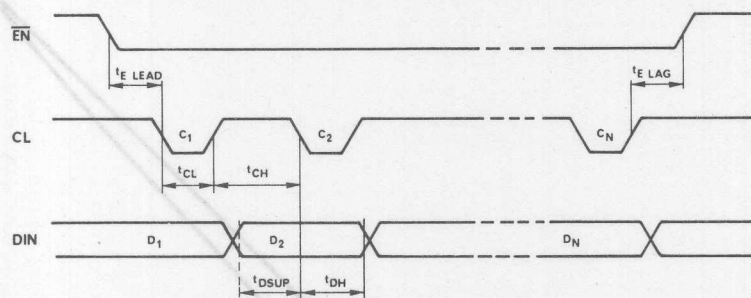
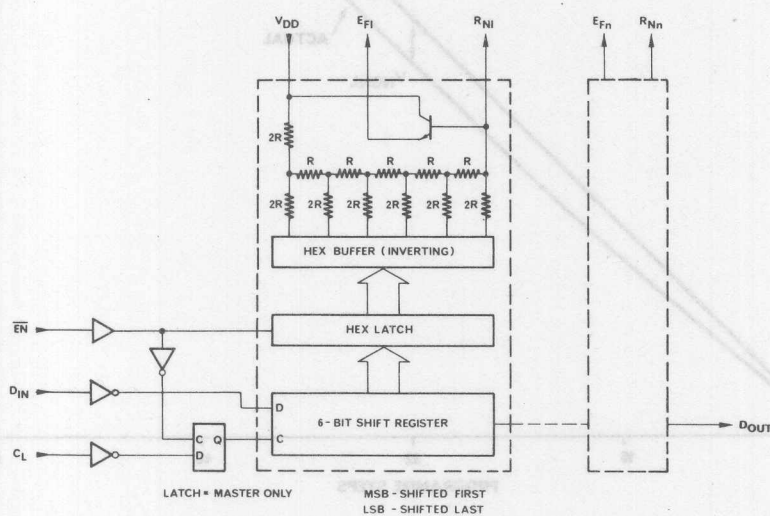
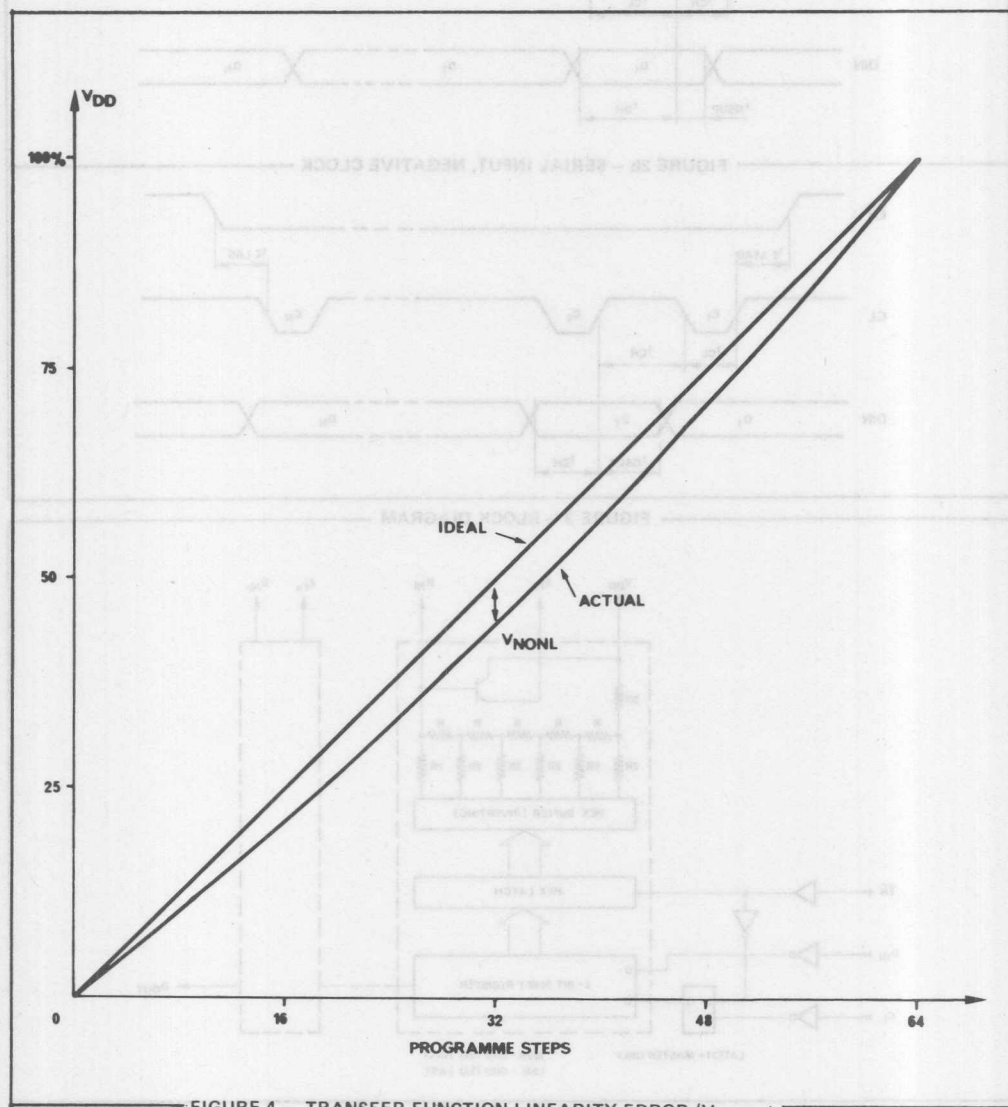


FIGURE 3 – BLOCK DIAGRAM

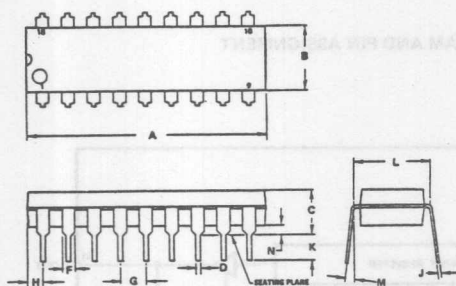


FIGURE 4 - TRANSFER FUNCTION LINEARITY ERROR (V_{NONL})

OUTLINE DIMENSIONS

PLASTIC PACKAGE

CASE 707-02

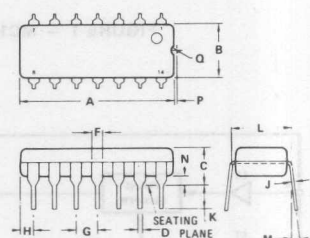


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 646



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

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is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MC144115

ADVANCE INFORMATION

2-DIGIT/ 16-SEGMENT LCD DRIVER

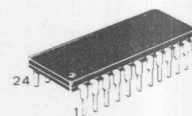
The MC144115 is a CMOS, cascadable, 2-digit/ 16-segment LCD driver with an on-chip oscillator. Data are clocked serially into and out of the circuit.

- Input level translators
- Direct drive (not multiplexed)
- On-chip oscillator
- Cascadable
- Internal 16-bit latch
- Wide power supply range, 3 to 18 V DC

CMOS

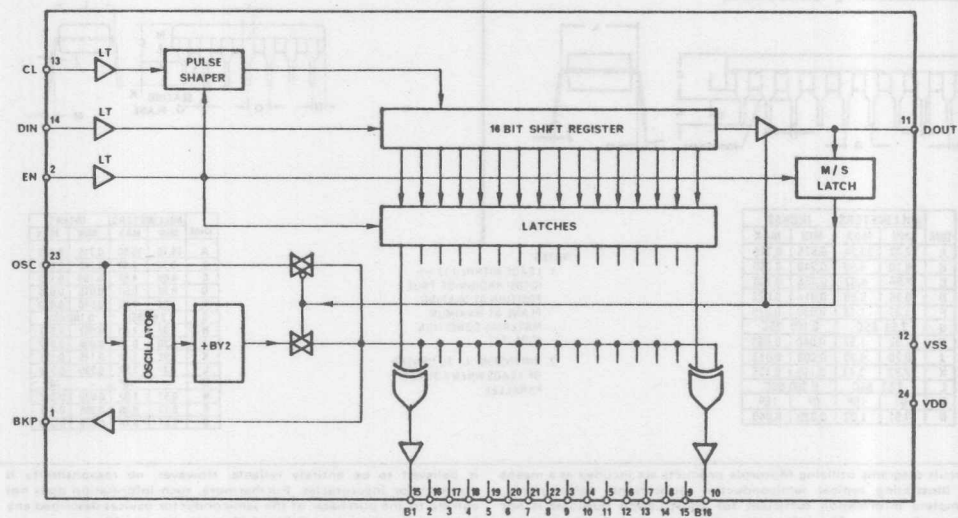
(LOW-POWER COMPLEMENTARY MOS)

2-DIGIT/ 16-SEGMENT LCD DRIVER



CP SUFFIX
PLASTIC PACKAGE
CASE 709

FIGURE 1 — MC144115 BLOCK DIAGRAM AND PIN ASSIGNMENT



LT = Level Translator

This is advance information and specifications are subject to change without notice

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V _{DD}	18 to -0.5	Vdc
Input Voltage, All Inputs	V _{in}	V _{DD} + 0.5 to V _{SS} - 0.5	Vdc
Input Current, All Pins	I _{in}	10	mAdc
Operating Temperature Range	T _A	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} - (V_{in} or V_{out}) - V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

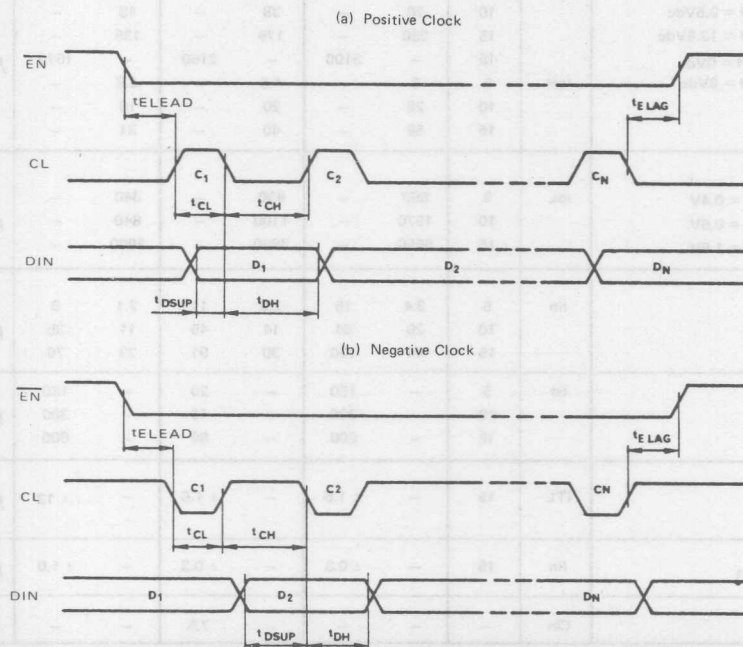
Characteristic	Symbol	V _{DD} Vdc	-40 °C		25 °C		85 °C		Unit
			Min	Max	Min	Max	Min	Max	
Segment Output Drive Current (pins 3, 4, 10, 15, 16, ... 22)									
Source V _{OH} = 4.6Vdc	ioH	5	220	—	160	—	120	—	
V _{OH} = 9.5Vdc		10	525	—	370	—	280	—	
V _{OH} = 13.5Vdc		15	1900	—	1300	—	1000	—	
Sink V _{OL} = 0.4Vdc	ioL	5	330	—	240	—	190	—	
V _{OL} = 0.5Vdc		10	880	—	600	—	470	—	
V _{OL} = 1.5Vdc		15	3100	—	2100	—	1600	—	
Source Current pin 1									
V _{OH} = 4.6 Vdc	ioH	5	690	—	500	—	390	—	μAdc
V _{OH} = 9.5Vdc		10	1620	—	1140	—	870	—	
V _{OH} = 1.3Vdc		15	5880	—	4000	—	3100	—	
Source Current pin 11									
Chip V _{OH} = 4.6Vdc	ioH	5	29	—	21	—	16	—	
Enabled V _{OH} = 9.5Vdc		10	70	—	38	—	49	—	
V _{OH} = 13.5Vdc		15	250	—	175	—	135	—	
V _{OH} = 0Vdc	ioH	15	—	3100	—	2160	—	1670	μAdc
Chip disabled V _{OH} = 0Vdc		5	6	—	4.5	—	3.8	—	
		10	28	—	20	—	16	—	
		15	58	—	40	—	31	—	
Sink Current for pins									
1 and 11 V _{OL} = 0.4V	ioL	5	590	—	430	—	340	—	μAdc
V _{OL} = 0.5V		10	1570	—	1100	—	840	—	
V _{OL} = 1.5V		15	5550	—	3850	—	2900	—	
Pin 23 Input Current (Master chip only)	I _{in}	5	3.4	15	2.6	11	2.1	9	μAdc
Sink (V _{in} = V _{DD}) or		10	20	64	14	45	11	35	
Source (V _{in} = V _{SS})		15	44	130	30	91	23	70	
Quiescent current	I _{ss}	5	—	150	—	20	—	150	μAdc
		10	—	300	—	40	—	300	
		15	—	600	—	80	—	600	
Tristate Output Leakage Current pins 11, 23	ITL	15	—	± 1.6	—	± 1.6	—	± 12	μAdc
Input Current Except pins 11 and 23	I _{in}	15	—	± 0.3	—	± 0.3	—	± 1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	7.5	—	—	PF

SWITCHING CHARACTERISTICS ($T_A = -40$ to $+85^\circ\text{C}$, $C_L = 50\text{pF}$, except DOUT = 20pF)

Characteristic	Condition	Symbol	Min	Max	Unit
Clock High Time	$V_{DD} = 5\text{V}$	t_{CH}	5	—	μs
	$V_{DD} = 10\text{V}$		4	—	μs
	$V_{DD} = 15\text{V}$		2	—	μs
Clock Low Time	$V_{DD} = 5\text{V}$	t_{CL}	5	—	μs
	$V_{DD} = 10\text{V}$		4	—	μs
	$V_{DD} = 15\text{V}$		2	—	μs
Enable Lead Time	$V_{DD} = 5\text{V}$	t_{Elead}	2	—	μs
	$V_{DD} = 10\text{V}$		1	—	μs
	$V_{DD} = 15\text{V}$		500	—	ns
Enable Lag Time	$V_{DD} = 5\text{V}$	t_{Elag}	500	—	ns
	$V_{DD} = 10\text{V}$		300	—	ns
	$V_{DD} = 15\text{V}$		200	—	ns
Data Set-up Time	$V_{DD} = 5\text{V}$	t_{Dsup}	500	—	ns
	$V_{DD} = 10\text{V}$		300	—	ns
	$V_{DD} = 15\text{V}$		200	—	ns
Data Hold Time	$V_{DD} = 5\text{V}$	t_{Dhold}	2	—	μs
	$V_{DD} = 10\text{V}$		1	—	μs
	$V_{DD} = 15\text{V}$		500	—	ns
Clock Rise Time	10% to 90% of V_{DD}	t_{Crise}	—	2	μs
Clock Fall Time	10% to 90% of V_{DD}	t_{Cfall}	—	2	μs
Min. \overline{EN} High Time, $C_L = 50\text{pF}^*$	5 to 15V	t_{Enh}	50	—	μs

* Min. time for the master/slave status of the chip to be latched in.

FIGURE 2 — TIMING DIAGRAM



CIRCUIT OPERATION

The circuit operation can be followed by referring to the block diagram, Figure 1.

Data are entered serially into the circuit's 16-bit shift register via the DIN pin. The data transfer rate is controlled by the clock input, CL, either positive or negative clock pulses may be used, see Figure 2.

The CL input is enabled only when the $\overline{\text{EN}}$ input is in the low state, logical '0'. On the positive going edge of $\overline{\text{EN}}$ data in the shift register are latched and transferred to the display drivers.

If more than two digits are to be displayed two, or more, circuits can be simply cascaded, as shown in Figure 3.

Level translators are provided on inputs CL, DIN and $\overline{\text{EN}}$ to allow the circuit to interface directly with a 5V powered controller, regardless of the circuit's own power supply voltage—which can lie anywhere in the range 5V to 15V.

LCD DRIVE

AC drive for the LCDs is provided by an on-chip, 50% duty cycle oscillator whose frequency is determined by a single external capacitor, see Figure 4.

A segment output is in phase with the backplane when the corresponding data bit in the shift register is low, logical '0'. The segment is in anti-phase when the corres-

ponding data bit is high, logical '1'.

CASCADING

When MC144115s are cascaded, that which controls the backplane frequency, called the master, is the last circuit in the shift register chain, see Figure 3.

The master's BKP output is connected directly to the slaves' OSC inputs. The slaves' oscillator circuits are bypassed and their backplane frequency is controlled by the OSC input.

DOUT acts as an input/output. When $\overline{\text{EN}}$ is high it acts as an input and when $\overline{\text{EN}}$ is low DOUT acts as an output. While the chip is disabled, $\overline{\text{EN}}$ at logical '1', an internal resistive pull-up pulls the slaves' DOUT pin high, to logical '1'. A falling edge on $\overline{\text{EN}}$ latches-in the logic state of DOUT which defines the master/slave status of each IC.

During the $\overline{\text{EN}}$ low time DOUT acts as an output; the internal pull-up is inactive and an output buffer is enabled (standard push-pull buffer in the slave mode, open drain N channel buffer in the master mode).

It is recommended that in a cascaded configuration the $\overline{\text{EN}}$ input is held high during power-up to avoid any chance of the circuit whose DOUT pin is grounded trying to act as a slave and drawing current through its P channel buffer transistor. This transistor is designed to limit the short circuit current to 3mA with a 15V supply.

INPUT/OUTPUT FUNCTIONS

CL — (pin 13) This is the clock input.

DIN — (pin 14) This is the serial data input pin.

$\overline{\text{EN}}$ — (pin 2) This is the chip enable pin and is active when low, logical '0'. On its positive going edge it causes the contents of the shift register to be loaded into the latches and transferred to the display drivers. When it is high it causes DOUT to act as an input and when low as an output.

BKP — (pin 1) This is the backplane driver output.

DOUT — (pin 11) This is the serial data output pin and is also used to determine the master/slave status of

the circuit.

In a master configuration the pin is tied to ground thus enabling the oscillator and disabling the push-pull data output buffer. In the slave configuration DOUT is tied to DIN of the following device, the oscillator is bypassed and the output buffer is enabled.

OSC — (pin 23) This pin, in the master role, needs an external frequency determining capacitor to ground, see Figure 3. In the slave role the oscillator circuitry is bypassed and the pin serves as the input for the backplane frequency.

B1 to B16 — (pins 3 to 10 and 15 to 22) These are the segment output drivers.

FIGURE 3 — Cascading MC144115s

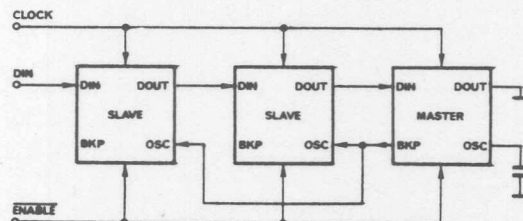
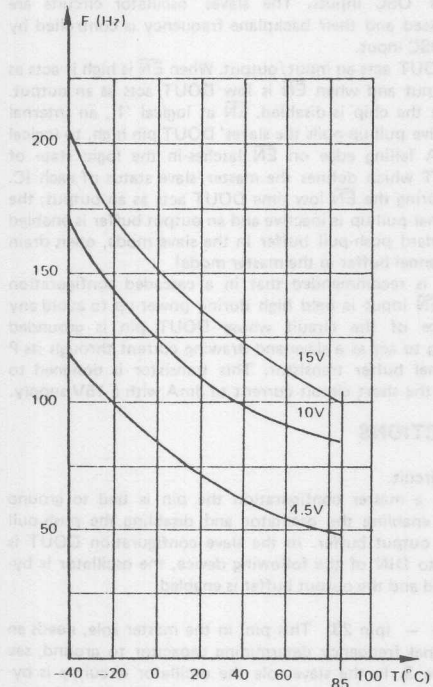
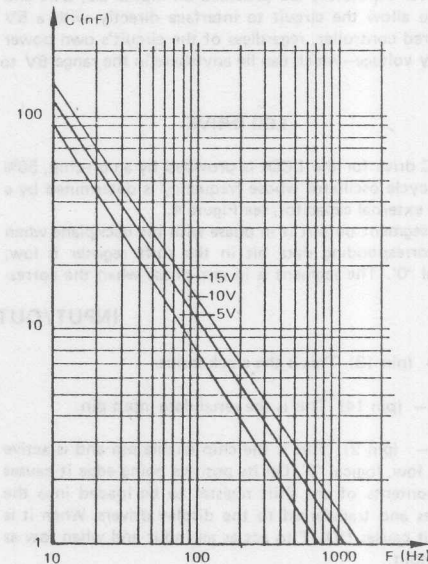


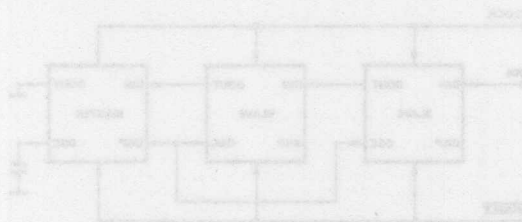
FIGURE 4 - BACKPLANE FREQUENCY



Typical Backplane Frequency
as a Function of Temperature
(10nF capacitor)



Typical Backplane Frequency
as a Function of Capacitor Value
(18°C)



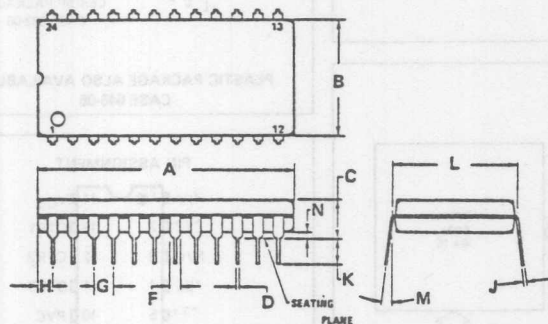
MC144115

MECHANICAL OUTLINES

CASE 709-02

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. 709-01 OBSOLETE, NEW STD 709-02.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24	BSC	0.600	BSC
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

MCM2801 (SMA2001)

Advance Information

16 × 16-BIT SERIAL ELECTRICALLY ERASABLE PROM

The MCM2801 is a 256-bit serial Electrically Erasable PROM designed for handling small amounts of data in applications requiring both non-volatile memory and in-system information updates.

The MCM2801 saves time and money because of the in-system erase and reprogram capability. It has external control of timing functions and serial format for data and address. The MCM2801 is fabricated in floating gate technology for high reliability and producibility.

- Single +5 V Power Supply
- Organized as 16 Words of 16 Bits
- Fully TTL Compatible
- Single +25 V Power Supply for Erase and Program
- In-System Program/Erase Capability

BLOCK DIAGRAM

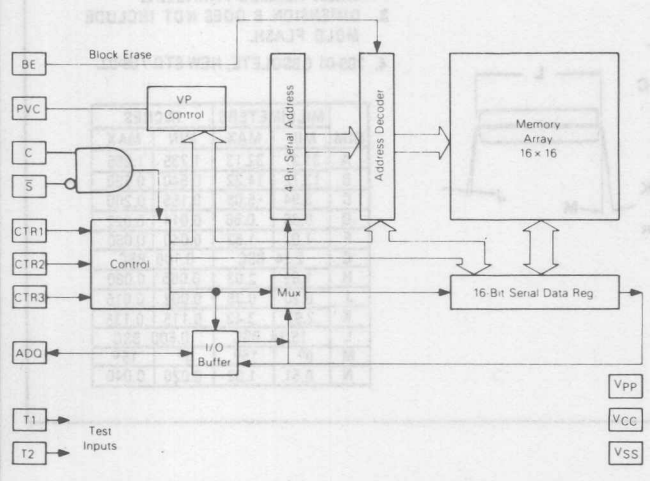
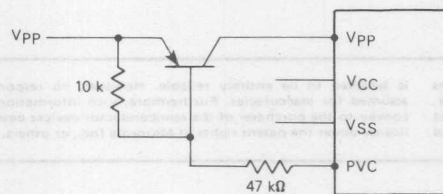


FIGURE 1 — Vpp CONTROL

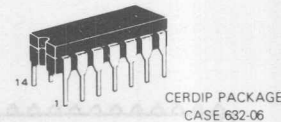


This is advance information and specifications are subject to change without notice.

MOS

(N-CHANNEL, SILICON GATE)

16 × 16 BIT ELECTRICALLY ERASABLE PROM



PLASTIC PACKAGE ALSO AVAILABLE —
CASE 646-05

PIN ASSIGNMENT

Vpp	1	14	VCC
*T2	2	13	CTR1
N/C	3	12	CTR2
*BE	4	11	CTR3
*T1	5	10	PVC
S	6	9	C
VSS	7	8	ADQ

*For normal operation, these inputs should be hardwired to VSS.

PIN NAMES

ADQ	Multiplexed Address/ Data-In/Data-Out
C	Clock
PVC	Program Voltage Control
CTR1, 2, 3	Control
BE	Block Erase
S	Chip Select
T1, T2	Test Pins

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ADI-841

MODE SELECTION

Mode	Pin Number						
	1 V _{PP}	6 S	7 V _{SS}	11 CTR3	12 CTR2	13 CTR1	14 V _{CC}
Standby	V _{SS} or V _{CC}	V _{IH}	V _{SS}	V _{IH}	V _{IH}	V _{IH}	V _{CC}
Word Erase	V _{PP}	V _{IL}	V _{SS}	V _{IH}	V _{IL}	V _{IL}	V _{CC}
Write	V _{PP}	V _{IL}	V _{SS}	V _{IL}	V _{IH}	V _{IL}	V _{CC}
Serial Data Out	V _{SS} or V _{CC}	V _{IL}	V _{SS}	V _{IH}	V _{IH}	V _{IL}	V _{CC}
Serial Address In	V _{SS} or V _{CC}	V _{IL}	V _{SS}	V _{IL}	V _{IL}	V _{IH}	V _{CC}
Serial Data In	V _{SS} or V _{CC}	V _{IL}	V _{SS}	V _{IH}	V _{IL}	V _{IH}	V _{CC}
Read	V _{SS} or V _{CC}	V _{IL}	V _{SS}	V _{IL}	V _{IH}	V _{IH}	V _{CC}
Standby	V _{SS} or V _{CC}	V _{IH}	V _{SS}	V _{IL}	V _{IL}	V _{IL}	V _{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Temperature Under Bias	-40 to +85	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	-55 to +150	°C
All Input or Output Voltages with Respect to V _{SS}	+8 to -0.5	V _{dc}
V _{PP} Supply Voltage with Respect to V _{SS}	+30 to -0.5	V _{dc}

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (Full operating voltage and temperature range unless otherwise noted.)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V _{dc}
	V _{PP}	24.0	25.0	26.0	V _{dc}
Input High Voltage	V _{IH}	4.0	—	V _{CC} + 1.0	V _{dc}
Input Low Voltage	V _{IL}	-0.1	—	0.8	V _{dc}

OPERATING DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Units
Input Sink Current	0 < V _{in} < V _{CC}	I _{in}	—	—	10	μA
V _{CC} Supply Current	S = V _{IL}	I _{CC}	—	—	30	mA
V _{PP} Supply Current	V _{PP} = 26.0 V	I _{PP}	—	—	4.0	mA
Output Low Voltage	I _{OL} = 1.0 mA	V _{OL}	—	—	0.5	V
Output High Voltage	I _{OH} = -0.1 mA	V _{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = +5 V, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V _{in} = 0 V)	C _{in}	—	6.0	pF
Output Capacitance (V _{out} = 0 V)	C _{out}	—	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I_{\Delta V} / \Delta V$.

Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others.

AC OPERATING CONDITIONS AND CHARACTERISTICS

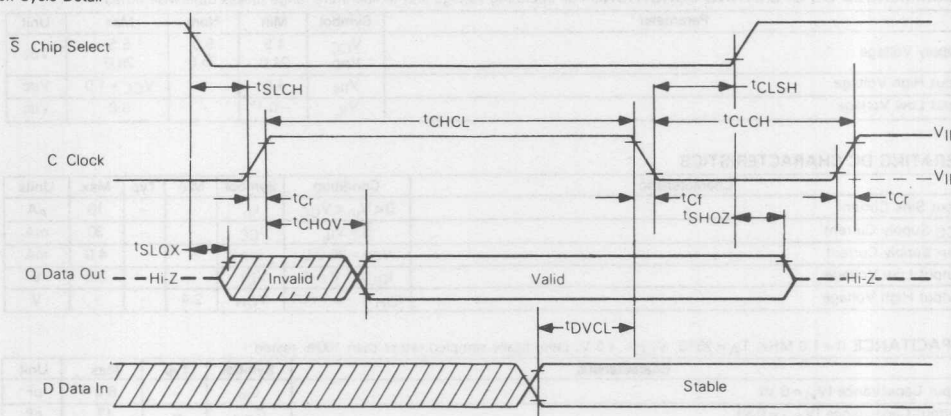
(Full operating voltage and temperature range unless otherwise noted.)

Input Pulse Levels..... 0.8 Volt and 4.0 Volts Input and Output Timing Levels..... 0.8 Volts and 4.0 Volts
 Input Rise and Fall Times..... 20 ns Output Load..... See Figure 2

Characteristic	Symbol	Min	Max	Unit
Clock High Level Hold Time	t_{CHCL}	4	10	μs
Clock Low Level Hold Time	t_{CLCH}	4	—	μs
Clock Rise Time	t_{Cr}	5	1000	ns
Clock Fall Time	t_{Cf}	5	1000	ns
Chip Select Lead Time	t_{SLCH}	1	—	μs
Chip Select Lag Time	t_{CLSH}	1	—	μs
Erase Time	t_{ERASE}	100	—	ms
Write Time	t_{WRITE}	10	—	ms
Data Out Delay	t_{CHQV}	0	3.0	μs
Address In Setup	t_{AVCL}	2	—	μs
Data In Setup	t_{DVCL}	2	—	μs
Control Setup Lead	t_{CtrVCH}	2	—	μs
Control Setup Lag	t_{CLCtrV}	50	—	ns
Data-Off Time (from the Clock)	t_{CHOZ}	0	3.0	μs
Chip Select Low to Output Active Time	t_{SLQZ}	0	3.0	μs
Data-Off Time (from Chip Select)	t_{SHQZ}	0	3.0	μs

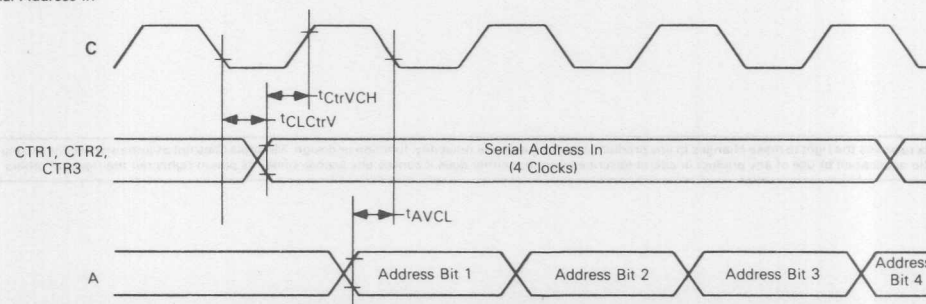
TIMING DIAGRAMS

Clock Cycle Detail

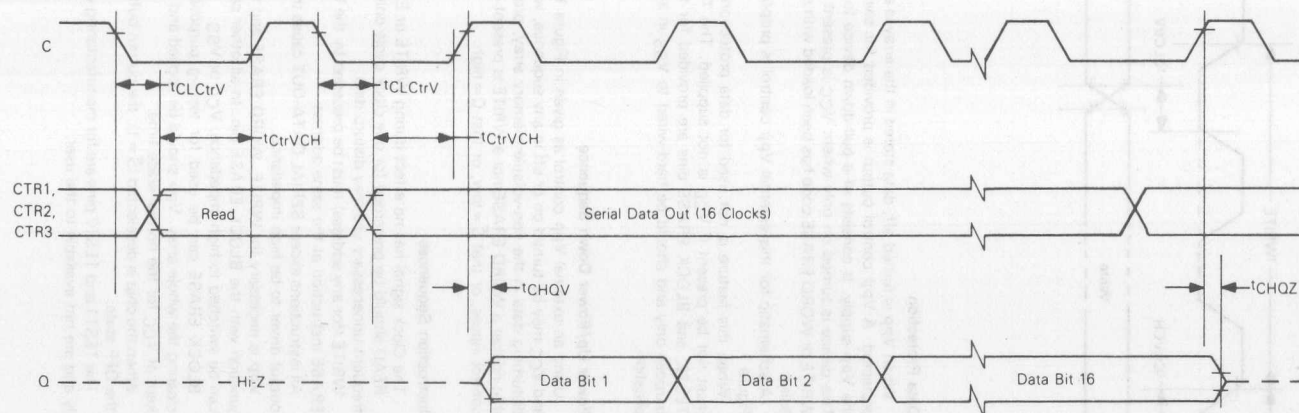


All times defined at 10% or 90% points.

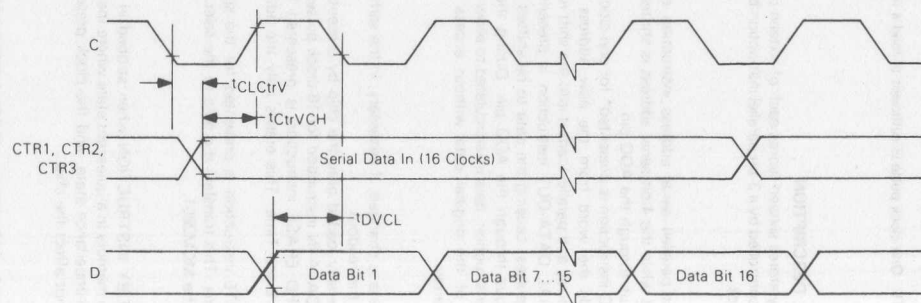
Serial Address In



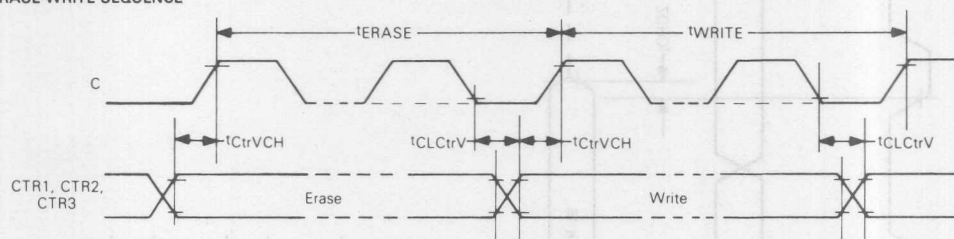
READ AND SERIAL DATA OUT



SERIAL DATA IN



ERASE-WRITE SEQUENCE



NOTE: One clock pulse is sufficient to load a new op code.

FUNCTIONAL DESCRIPTION

The memory stores sixteen words each of sixteen bits. All functions are controlled by a 3-bit parallel instruction bus and an applied clock.

Read-Out

- 1) The (3-bit parallel) serial address instruction code is presented while the 4-bit serial address is shifted in on the I/O bus through the ADQ pin.
- 2) The READ instruction is presented* for one clock time. This reads the word from the new address in the memory array and parallel loads it into the shift register.
- 3) The SERIAL DATA-OUT instruction is presented for 16-clock pulses, causing the data to be shifted out on the I/O bus through the ADQ pin. During the serial data-out instruction, data is recirculated to allow further read-out of the original data without access to the memory array.

Writing

- 1) The address is changed, if necessary, in the same manner as in the readout.
- 2) Data is serially loaded onto the chip by presenting the SERIAL DATA-IN instruction for 16-clock pulses.
- 3) The WORD ERASE instruction is presented for the specified Erase Time. This erases only the addressed word.
- 4) The WRITE instruction is presented for the specified Write Time. This transfers the data to the selected address in the MCM2801.

Standby

The STANDBY INSTRUCTION when strobed in by the clock puts the memory in a quiescent state where the output is in the high-impedance state, and the clock presence or absence will not affect the chip.

Clock

The active high clock signal is used for loading instruction codes, for introducing serial addresses and data, and for shifting serial data out. The clock has no influence on any other function.

Data Protection

When Vpp is turned off, data stored in the array is always protected. A Vpp control output is provided for switching the Vpp supply. It consists of a pull-down device to VSS. This device is turned on only when: VCC is present and a WRITE or WORD ERASE code has been loaded with a clock pulse.

A schematic for this external Vpp control is proposed in Figure 1.

When this feature is not used for data protection, Vpp must not be present if VCC is not supplied. The TEST1, TEST2, and BLOCK ERASE pins are provided for testing purpose only and should be hard-wired to VSS in any application.

Power Up/Power Down Sequence

Using an external Vpp control as given in Figure 1, Vpp and VCC may be turned on or off in any sequence, without disturbing data in the non-volatile memory array, providing that neither a WORD ERASE nor a WRITE is present on the control inputs, or that \bar{S} = low, or that C = high.

Instruction Sequences

The Clock signal has no effect during WRITE or ERASE. READ should be presented for one clock cycle only since frequent unnecessary use may disturb data.

WRITE (for any address) must be preceded by the WORD ERASE instruction at the same address.

All instructions except SERIAL DATA-OUT cause the data output driver to be high impedance.

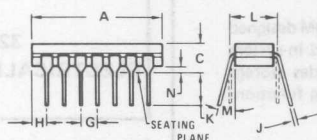
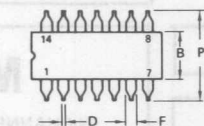
Vpp is necessary for WRITE, WORD ERASE and in conjunction with the BLOCK ERASE pin. In all other cases, it can be switched to high impedance, VCC or VSS.

BLOCK ERASE can be used for testing purposes. For clearing the whole array, Vpp should be applied and BE pin kept at VCC for the normal erase time.

When the chip is deselected (\bar{S} = 1), the output buffer is in the OFF state.

The TEST1 and TEST2 pins are for manufacturing use only and are not available to the user.

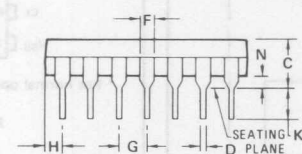
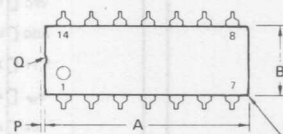
OUTLINE DIMENSIONS



DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC	—	0.100 BSC	—
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	5.08	0.125	0.200
L	7.62 BSC	—	0.300 BSC	—
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:

1. ALL RULES AND NOTES ASSOCIATED WITH MO 001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "A" AND "B" (632-06) DO NOT INCLUDE GLASS RUN-OUT.
4. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.



DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC	—	0.100 BSC	—
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC	—	0.300 BSC	—
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

MCM2802

Advance Information

32 X 32 BIT SERIAL ELECTRICALLY ERASABLE PROM

The MCM6224 is a 1K-bit serial Electrically Erasable PROM designed for applications requiring both non-volatile memory and in-system information updates. In digital tuning systems, it provides storage for up to 32 channels. It has external control of timing functions and serial format for data and address.

- Single 5V supply in Read mode
- 5V and 25V supply for Erase and Program
- In-System Program/Erase Capability
- 0-100kHz clock rate
- Floating gate process
- Expandable to 16K-bit systems

MOS

(N-CHANNEL, SILICON GATE)

32 X 32 BIT ELECTRICALLY ERASABLE PROM

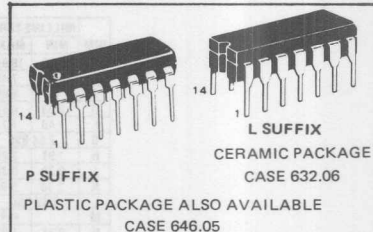
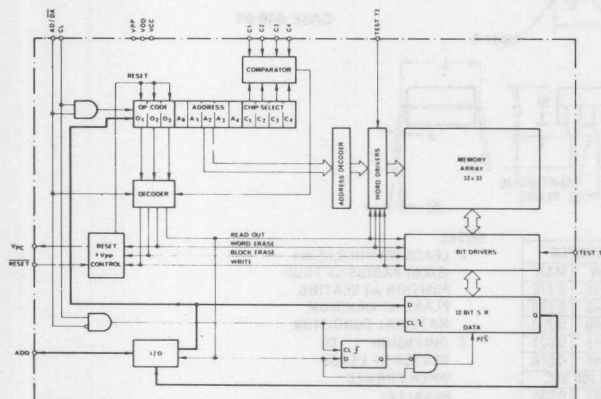
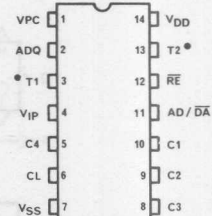


FIGURE 1 - BLOCK DIAGRAM



PIN ASSIGNMENT



* For normal operation, hardwired to V_{SS}.

PIN NAMES

VPC Program Voltage Control
ADQ Address Input + Data Input/Output
T1, T2 Margin Testing
C1, C2, C3, C4 Chip Address 1 to 4
CL Clock
RE Reset
AD/DA Shift Register Select

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V_{SS})

Rating	Symbol	Min	Max	Unit
DC Supply Voltage	V_{DD}	-0.5	8	Vdc
Programming Voltage	V_{PP}	-0.5	28	Vdc
Input Voltage	V_{IN}	-0.5	8	Vdc
VP Control Output	V_{PC}	-0.5	28	Vdc
Operating Temperature Range	T_A	-40	85	°C
Storage Temperature Range	T_{STC}	-55	150	°C

NOTE — Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

SWITCHING CHARACTERISTICS ($T_A = 0 \dots 70^\circ\text{C}$; $V_{DD} = 5V \pm 10\%$; $V_P = 25V \pm 1V$)

Pin	Symbol	Parameter	Fig No	Min	Max
	t_{ER}	Erase time		100ms	
	t_{WR}	Write time		10ms	
CL	F_{CL}	Clock Frequency $F_{CL} = 1/T_{CL}$	2		100kHz
CL	t_{CLH}	Clock High Level Hold Time	2	4 μs	
CL	t_{CLL}	Clock Low Level Hold Time	2	4 μs	
CL	t_{CLRF}	Clock Fall Time and Rise Time	2		1 μs
AD/DA	$t_{AD/DA}$	Register Control to Clock			
		Delay Time except for t_{READ}	2	1 μs	
	t_{READ}	After READ opcode only	3	5 μs	100 μs
I/O	t_{DSUP}	Data In Set-Up	2, 3	2 μs	
	t_{DH}	Data In Hold	2, 3	0.1 μs	
I/O	t_{DOUS}	Data Out Serial Delay	3	50 ns	1 μs
	t_{DOUTP}	Data Out Parallel Delay	3	50 ns	3 μs

RETENTIVITY CHARACTERISTICS (ESTIMATED)

For normal operating conditions :

$$T_A = 0 \dots 70^\circ\text{C}$$

$$V_{DD} = 5V \pm 10\%$$

$V_P = 25V \pm 1V$ continuously, or switched to open circuit.

Minimum retention time is one year under worst case conditions. Minimum number of times a complete 32 bit word may be accessed without loss of stored data after 10^4 erase/write cycles is 10^6 cycles per word.

DC CHARACTERISTICS ($T_A = 0 \dots 70^\circ\text{C}$; $V_{DD} = 5V \pm 10\%$; $V_P = 25V \pm 1V$)

Pin	Characteristic	Condition	Symbol	Min	Max	Unit
V_{PP}	Supply Current		I_{PP}		5	mA
V_{DD}	Supply Current		I_{DD}		30	mA
I/O	Tristate Input/ Output	$V_{OH} = 2.4V$	I_{OH}	-0.1		mA
		$V_{OL} = 0.5V$	I_{OL}	1.6		mA
		Tristate	I_{IN}		10	μA
All Inputs Except I/O	Input Leakage		I_{IN}		1	μA
V_{PC}	VP Control Pull down device	$V_{ON} = 1V$	I_{ON}	0.7		mA
		OFF state $V_{OFF} = V_P$	V_{MAX} I_{OFF}		V_{PP} 5	μA
All Inputs	Input Low Voltage	V_{IL}			0.8	V
	Input High Voltage	V_{IH}		2.4		V

FIGURE 2 — GENERAL TIMINGS

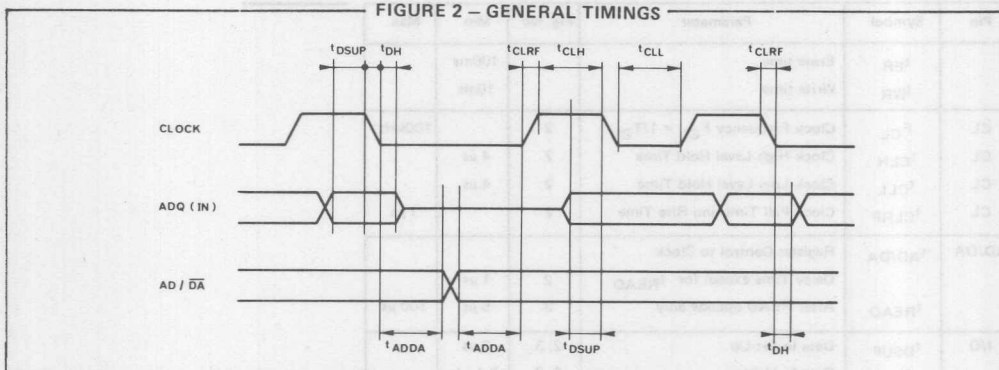
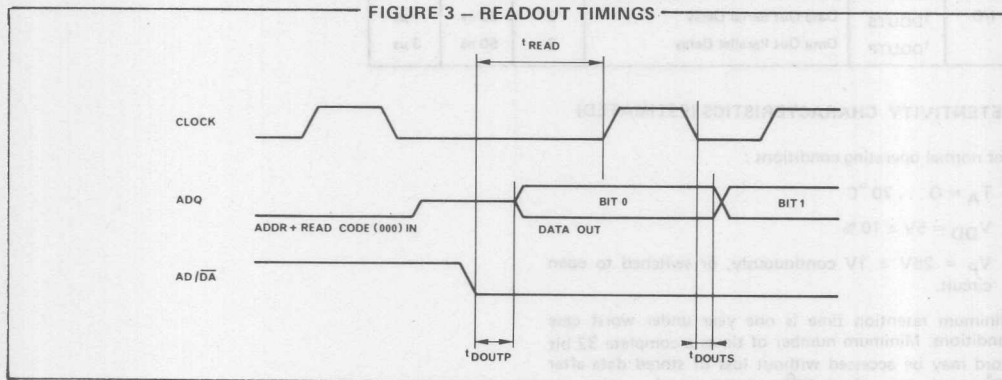


FIGURE 3 — READOUT TIMINGS



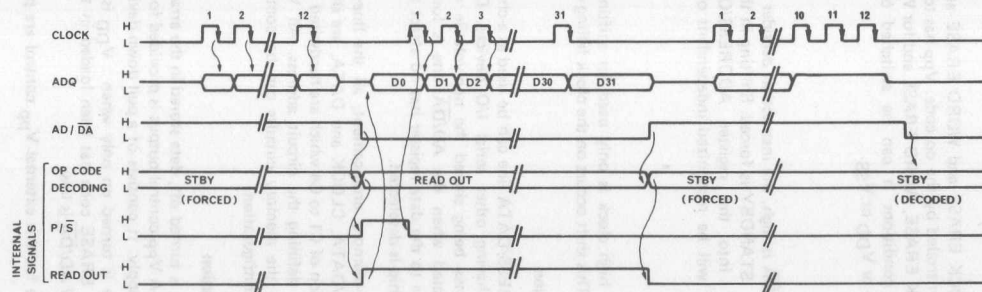


FIGURE 4 - READOUT SEQUENCE

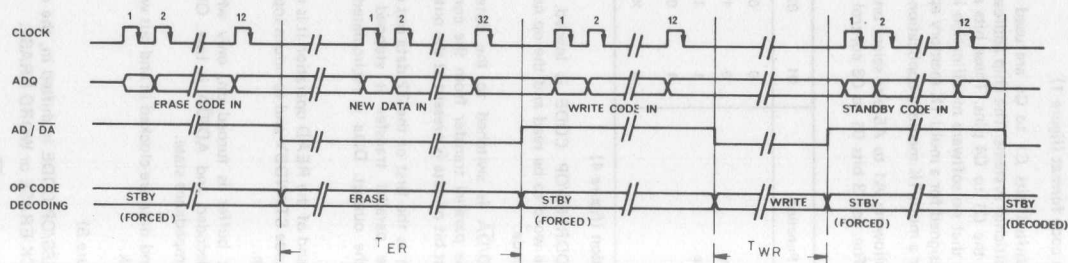


FIGURE 5 - WRITE SEQUENCE

FUNCTIONAL DESCRIPTION

The circuit accepts 12 bits of Address/Op code and 32 bits of data in two different shift registers. (see figure 1 : Block diagram)

Address/Op code format (figure 1)

The four shifted bits C1 to C4 are used as chip select word in multichip systems. The chip address is defined by hardwiring the C1 to C4 pins. These bits are part of the address, so that no software modification is required in a program designed for a multi-1K memory application.

The five following A1 to A5 bits select one of the word addresses. The last 3 bits O1 to O3 control the operating modes.

Function	O1	O2	O3
Read	0	0	0
Word Erase	0	1	0
Block Erase	1	1	0
Write	1	0	0
Standby	X	X	1

Read operation (figure 4)

- 1) The ADDRESS/OP CODE is loaded. The address selecting the word to be read and the op code bits being the READ code.
- 2) The AD/ \overline{DA} is switched to the data mode, thus initiating the parallel transfer from the core to the shift register. First bit of data is present at the output.
- 3) As soon as the first of the 32 data out clock pulses is applied, the parallel transfer is stopped and data is shifted at the output. Data is recirculated in the data register.
- 4) At the end of the READ operation it is recommended to load op code STANDBY and to return input AD/ \overline{DA} to the low state.

The output buffer is turned on, only when READ is internally decoded and AD/ \overline{DA} is low. Otherwise it is in the high impedance state.

Addresses and data are clocked in and out with the falling edge of clock.

Writing (figure 5)

- 1) ADDRESS/OP CODE is shifted in, the op code being either BLOCK ERASE or WORD ERASE.
- 2) Switching the AD/ \overline{DA} line low for $t = t_{\text{ERASE}}$, erases the selected word. During this period of time, a data word can be shifted in to the data register.
- 3) Then the WRITE code and the same address is loaded to the address register.

- 4) The AD/ \overline{DA} line is switched low again for a $t = t_{\text{WRITE}}$.

- 5) At the end of the WRITE operation it is recommended to load op code STANDBY and to return input AD/ \overline{DA} to the low state.

Erase

Both BLOCK ERASE and WORD ERASE are provided and are controlled by the op code. V_{pp} has to be applied for BLOCK ERASE, WORD ERASE and for WRITE. For all other conditions it can be switched off to high impedance or V_{DD} or V_{SS} .

Standby

When AD/ \overline{DA} is high, the instruction decoder is disabled and hence STANDBY is forced. Shifting in the op code STANDBY into the register ADDRESS/OP CODE, STANDBY will be recognized independent of the state of AD/ \overline{DA} .

Clock

The active high clock is only used for shifting data and addresses. This shift occurs on the clock falling edge.

Chip selection

The ADDRESS/DATA line can be used as a chip select in a system having other serial I/O devices. DATA and CLOCK lines being shared the non-volatile memory is only activated when the AD/ \overline{DA} line is low. Shifting information to the data register has no effect to the core while the chip is deselected.

In a multi-memory arrangement, all the lines including ADDRESS/DATA, CLOCK and DATA, are shared, with the exception of C1 to C4 which are hardwired to V_{DD} or V_{SS} , thus defining the circuit address. All V_{p} control outputs of the memory circuits can be combined in a wired OR configuration.

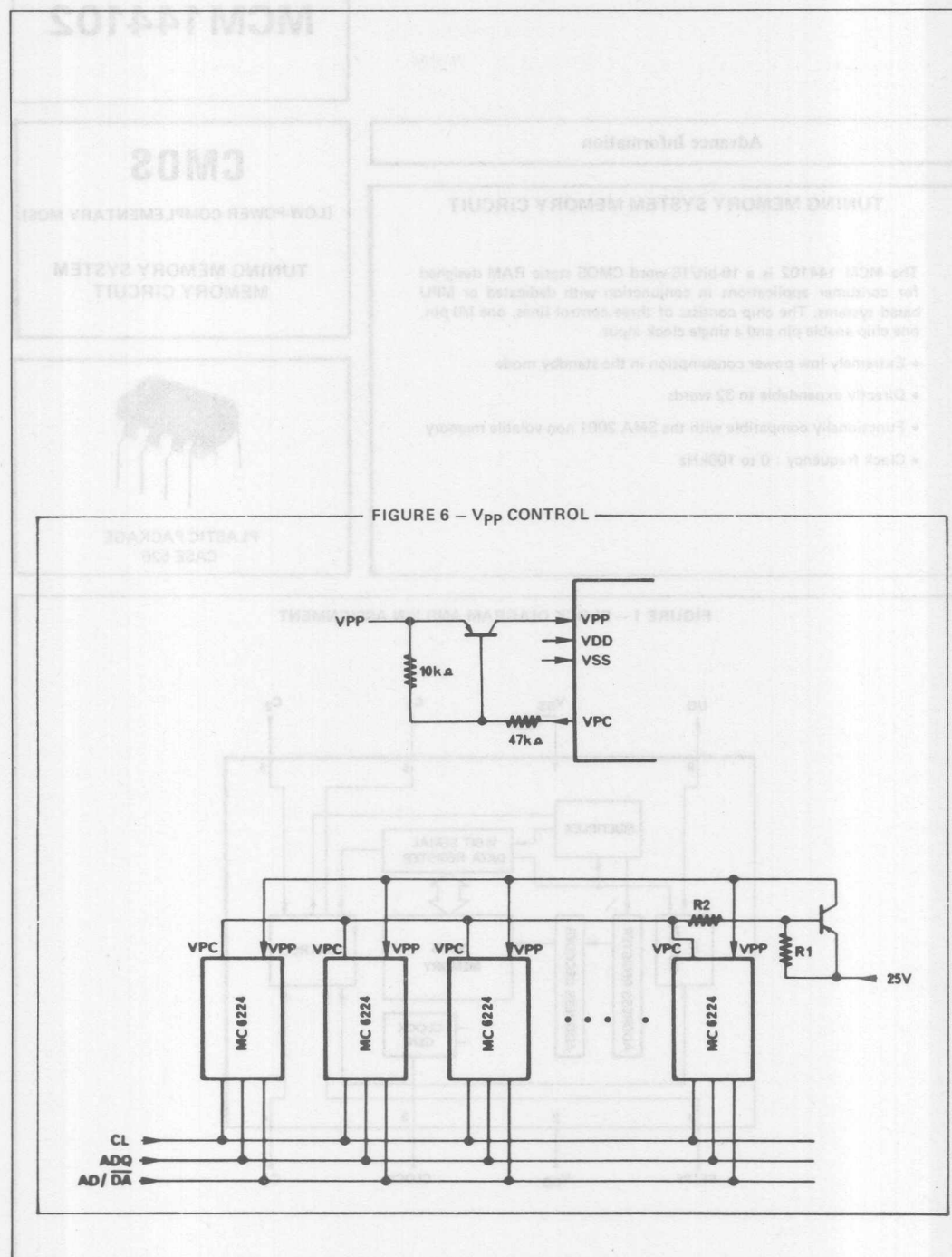
Data protection

When V_{pp} is turned off, data stored in the array is always protected. A V_{pp} control output is provided for switching the V_{pp} supply. It consists of a pull down device to V_{SS} . This device is turned on only when : V_{DD} is present, a WRITE or ERASE code has been loaded in the address register and AD/ \overline{DA} is low.

Schematics for this external V_{pp} control are proposed in figure 6.

Reset

V_{pp} and V_{DD} may be turned on or off in any sequence without disturbing data in the NVM array. During power-up, the op code is preset to the standby mode. The RESET input can be connected to the system RESET.



MCM144102

Advance Information

TUNING MEMORY SYSTEM MEMORY CIRCUIT

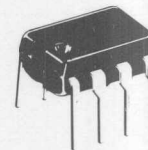
The MCM 144102 is a 16-bit/16-word CMOS static RAM designed for consumer applications in conjunction with dedicated or MPU based systems. The chip consists of three control lines, one I/O pin, one chip enable pin and a single clock input.

- Extremely low power consumption in the standby mode
- Directly expandable to 32 words
- Functionally compatible with the SMA 2001 non-volatile memory
- Clock frequency : 0 to 100kHz

CMOS

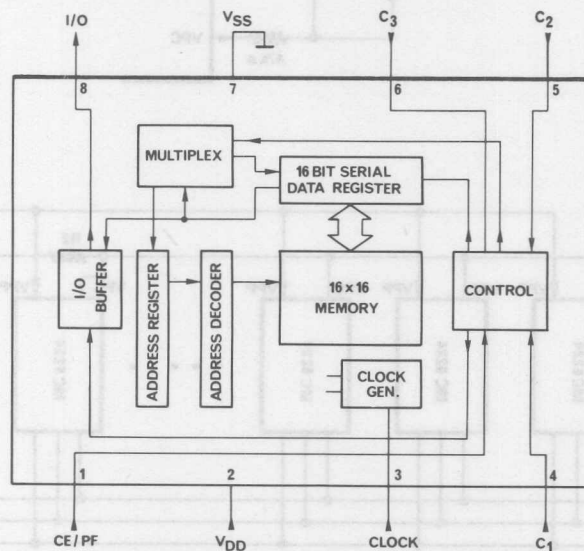
(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM MEMORY CIRCUIT



PLASTIC PACKAGE
CASE 626

FIGURE 1 – BLOCK DIAGRAM AND PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS} , Pin 7.)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	7 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	$V_{DD} + 0.5$ to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C , $V_{DD} = 4.5\text{V}$ to 6.5V)

Characteristic	Symbol	V_{DD} Vdc	-40°C		25°C			+70°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5V	-	0.05	-	0	0.05	-	0.05	Vdc
$V_{in} = 0$ or V_{DD} "1" Level	V_{OH}	5V	4.95	-	4.95	5	-	4.95	-	Vdc
Input Voltage "0" Level ($V_O = 4\text{V}$ or 0.5V) ($V_O = 4.5\text{V}$ or 0.5V) ($V_O = 6.0\text{V}$ or 0.5V)	V_{IL}	4.5V 5.0V 6.5V	- - -	1.35V 1.5V 1.95V	- - -	- - -	1.35V 1.5V 1.95V	- - -	1.35V 1.5V 1.95V	Vdc
"1" Level ($V_O = 0.5\text{V}$ or 4V) ($V_O = 0.5\text{V}$ or 4.5V) ($V_O = 0.5\text{V}$ or 6V)	V_{IH}	4.5V 5.0V 6.5V	3.5 3.50 4.55	- - -	3.5 3.50 4.55	- - -	- - -	3.15 3.50 4.55	- - -	Vdc
Input Current (all inputs) Low $V_{IN} = 0\text{V}$	I_{IL}	6.5V	-	-1	-	-	-1	-	-1	μAdc
High	I_{IH}	6.5V	-	1	-	-	1	-	1	μAdc
Output Current, Source (Data I/O) $V_{OH} = V_{DD} - 0.8\text{V}$	I_{OH}	-	-2	-	-1.4	-	-	-1	-	mAdc
$V_{OL} = 0.8\text{V}$ Sink	I_{OL}	-	2	-	1.4	-	-	1	-	mAdc
Tri-state output (Data I/O Leakage Current) $V_{OT} = V_{DD}$	I_{TH}	-	-	1	-	-	1	-	1	μAdc
$V_{OT} = 0\text{V}$	I_{TL}	-	-	-1	-	-	-1	-	-1	μAdc
Quiescent Current Operating	I_{DDOP}	5V	-	50	-	-	50	-	350	μAdc
Standby	I_{DDSTB}	1.2V	-	10	-	-	10	-	80	μAdc

SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C , $V_{DD} = +4.5$ to $+6.5\text{V}$)

Parameter	Pin	Symbol	Min	Typ	Max	Unit
Clock Frequency ($f_{CL} = 1/t_{CL}$)	3 ¹⁾	f_{CL}			100	kHz
Clock Hold Time High		t_{CLH}	4		20	μs
Low		t_{CLL}	4			μs
Clock Rise and Fall Time		t_{CLF}			1	μs
Write Time (per word)		t_{WRITE}	1 clock cycle			
Read Time (per word)		t_{READ}	1 clock cycle			
Data Out Delay	8 ³⁾	$t_1^{2)}$	50n		3	μs
Data In Set Up Time		t_2	2			μs
Instruction Set up Lead	4 ¹⁾ , 5, 6	t_3	2			μs
Lag		t_4	50			ns

NOTES :

¹ The maximum pin capacitance is 10pF to V_{SS} for : C_1 , C_2 , C_3 and clock

² t_1 applies only during data transition as the data format is NRZ

³ The output external loading capacitance will be 10pF (max)

INPUT/OUTPUT FUNCTIONS

READ — The memory can store up 16, 16-bit words, with all functions controlled by a 3-bit parallel instruction bus and an applied clock, which may be free running.

A READ instruction, presented for one clock period moves data from memory and parallel loads it in to the shift register.

A SERIAL DATA OUT instruction, presented for 16 clock pulses, causes the data to be moved out of the chip on the I/O bus. During this time the data are internally recirculated to allow further read out without accessing the memory array.

WRITE — This is basically the inverse of READ. The address can be changed and data serially loaded in to the chip over 16 clock cycles. The WRITE instruction, presented for one clock period, shifts the data in to the selected address in the memory array.

CLOCK — This is active high. In all modes, other than WRITE, the memory array remains undisturbed by the presence, or absence, of signals on the clock line.

POWER FAIL/CHIP ENABLE — Only when this dual purpose pin is high, = 1, is the chip selected. At all other times, including low power conditions, the memory is disabled thus avoiding erroneous data transfer and excessive drain on the standby battery due to intermediate levels on the inputs.

STANDBY — When this instruction is received the memory goes in to a quiescent state, when only a 1.2V battery is necessary to supply the device's modest power requirements.

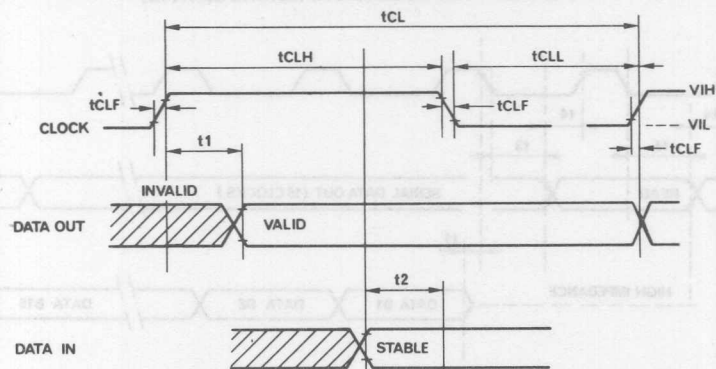
INSTRUCTION SEQUENCES — The READ and WRITE instructions need to be presented for one clock cycle only. All instructions, except SERIAL DATA OUT, force the output data driver to a high impedance state.

TABLE 1 — INSTRUCTION CODES

C1	C2	C3	INSTRUCTION	CLOCK FREQUENCY	
				MIN	MAX
1	1	1	Standby	0	100kHz
0	0	1	No operation	—	—
0	1	0	Write	0	100kHz
0	1	1	Serial Data Out	0	100kHz
0	0	0	No Operation	—	—
1	0	0	Serial Address In	0	100kHz
1	0	1	Serial Data In	0	100kHz
1	1	0	Read	0	100kHz

1 = high 0 = low

FIGURE 2a – TIMING DIAGRAM (GENERAL)



Note: Figure 2A defines V_H and V_L levels for all figures.

FIGURE 2b – TIMING DIAGRAM (SERIAL ADDRESS IN)

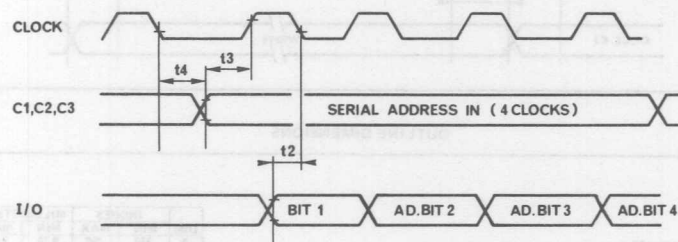


FIGURE 2c – TIMING DIAGRAM (READ & SERIAL DATA OUT)

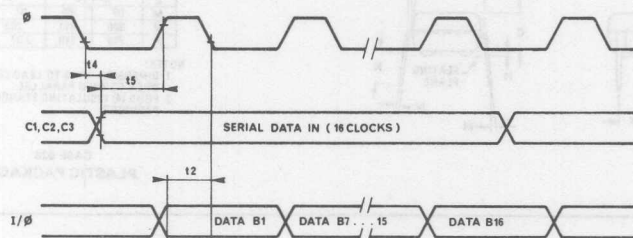


FIGURE 2d - TIMING DIAGRAM (SERIAL DATA IN)

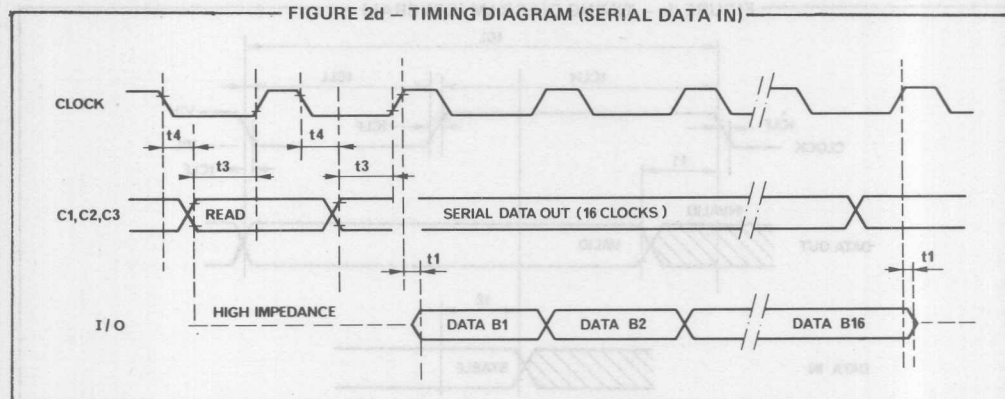
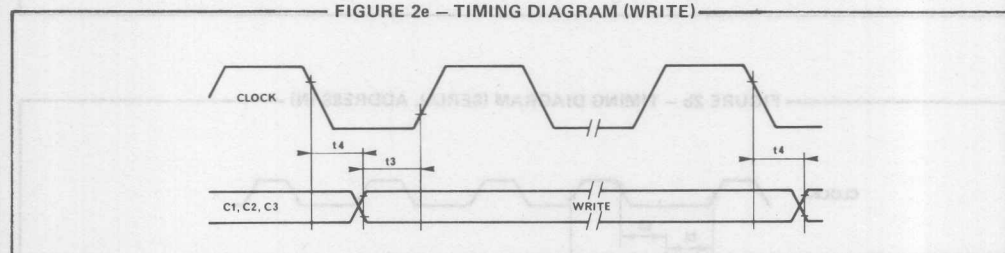
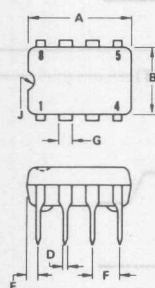
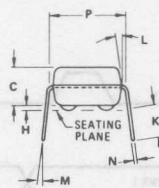


FIGURE 2e - TIMING DIAGRAM (WRITE)



OUTLINE DIMENSIONS

Weight ≈ 0.446 gram

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.370	.390	9.39	9.90
B	.240	.250	6.09	6.35
C	.135	.155	3.43	3.94
D	.015	.019	.381	.483
E	—	.045	—	1.14
F	0.100 TYP			
G	.030	.060	.762	1.52
H	.020 NOM			
J	.030	.040R	.762	1.02R
K	.115	.135	2.92	3.43
L	.70 TYP			
M	.00	.100	.00	100
N	.008	.011	.203	.279
P	.290	.310	7.37	7.87

NOTES:
 1. DIMENSION "P" IS TO LEAD CENTERLINE WHEN FORMED PARALLEL
 2. FOUR (4) INSULATING STANDOFFS ARE PROVIDED.

CASE 626
 PLASTIC PACKAGE

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

SAA1006

DIODE MATRIX ENCODER

The SAA 1006 provides a 16 line to 4-bit binary encoding for general purpose applications.

It is also suitable to be used in conjunction with the remote control receiver MC6525, MC6526, MC6527, MC6529 for local instruction encoding.

DIODE MATRIX ENCODER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Forward Current per Pin	I_F	20	mAdc
Reverse Voltage all Pins	V_R	6,5	Vdc
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

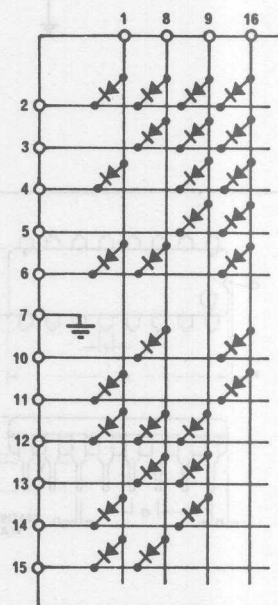
Characteristics	Symbol	Min.	Typ.	Max.	Unit
Reverse Current per Pin @ $V_R = 6.0\text{ V}$	I_R			30	μA
Forward Voltage Drop per Pin @ $I_F = 2.0\text{ mA}$	V_F			1	Volt

FUNCTIONAL TRUTH TABLE

OUTPUT PINS	INPUT PINS ¹															
	2	3	4	5	6	10	11	16	12	13	14	9	15	8	1	all open
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
8	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
9	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
16	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

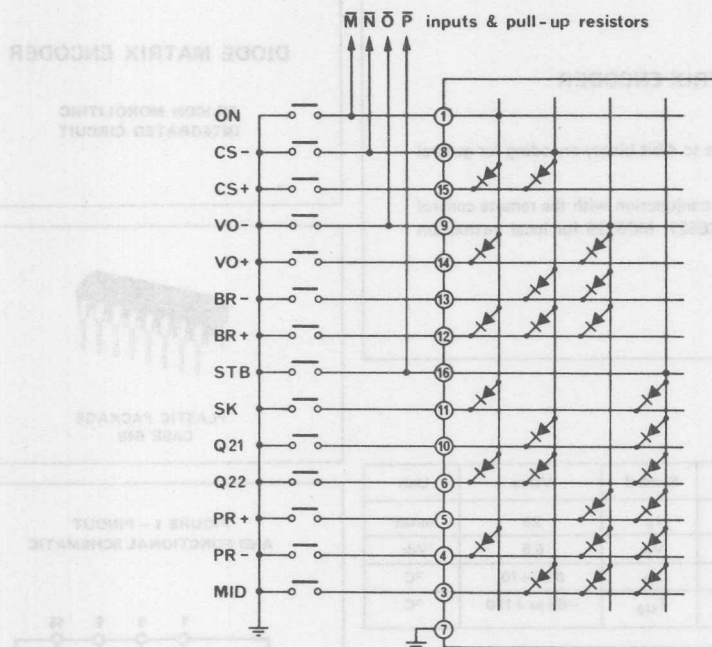
¹ One pin at a time to be grounded.

FIGURE 1 - PINOUT
AND FUNCTIONAL SCHEMATIC

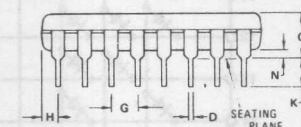
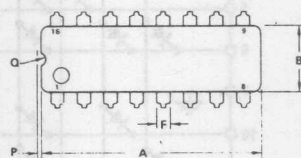


APPLICATION INFORMATION

When used in conjunction with the remote control receivers MC6525/6/7/9 it will encode the following commands.



PACKAGE DIMENSIONS



NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.54	BSC	0.100	BSC
G	1.32	1.83	0.052	0.072
H	0.20	0.30	0.008	0.012
I	2.92	3.43	0.115	0.135
J	7.37	7.87	0.290	0.310
K	10°		10°	
L	0.51	1.02	0.020	0.040
M	0.13	0.38	0.005	0.015
N	0.51	0.76	0.020	0.030

TBA 120 C
TBA 120 D*

FM IF AMPLIFIER, LIMITER AND DETECTOR

An integrated circuit specifically designed for use in the sound section of TV-receivers and the FM/IF portion of radio receivers.

The TBA 120 C is pin for pin and function compatible with the proelectron type TBA 120 S but includes an improved D.C. volume control, which makes "grouping" or selection unnecessary.

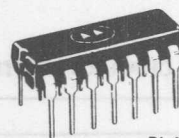
The TBA 120 D is pin for pin compatible with the proelectron type TBA 120, which is using external phase shift capacitors.

Features:

- Excellent 3dB limiting
- High A.M. rejection
- Wide supply voltage range
- Auxiliary zener diode & transistor
- Minimum number of external components required.

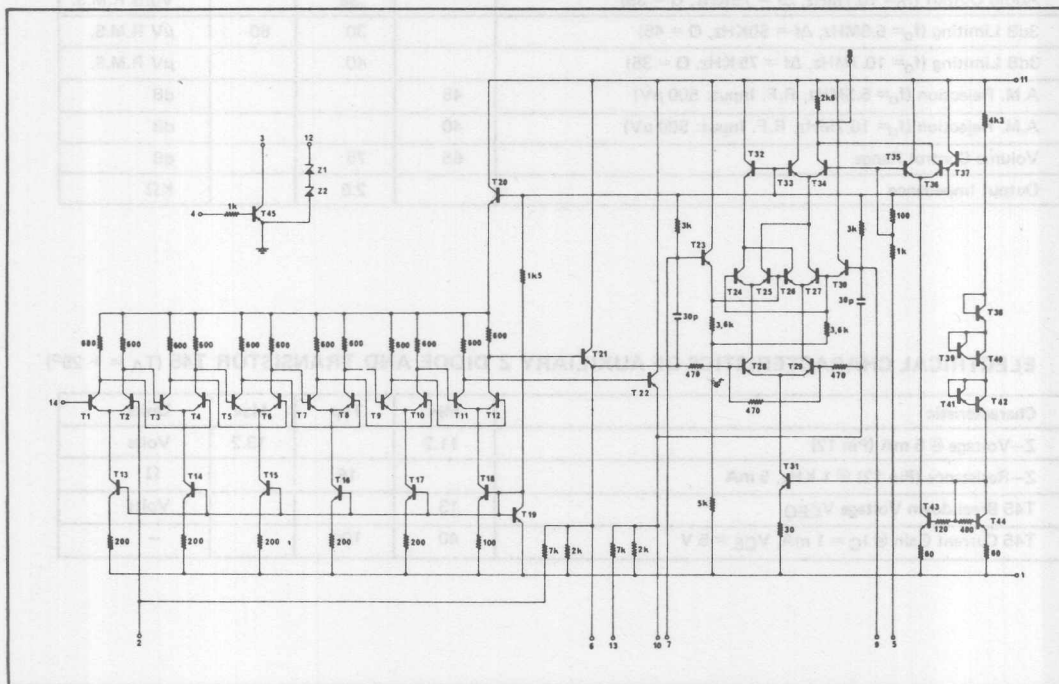
**FM IF AMPLIFIER,
LIMITER, FM DETECTOR
AND
AUDIO PREAMPLIFIER**

**MONOLITHIC SILICON
INTEGRATED CIRCUIT**



PLASTIC PACKAGE
CASE 646 TO-116

CIRCUIT SCHEMATIC



*TBA 120 D: Pins 6 and 10 are not connected internally otherwise same as TBA 120 C.

TBA120C, TBA120D

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless other wise noted.)

Rating	Value	Unit
Power Supply Voltage	+ 18	Vdc
Power Dissipation (Package Limitation)	625	mW
Plastic Package	5.0	mW/ $^\circ\text{C}$
Derate above $T_A = +25^\circ\text{C}$		
Operating Temperature Range	0 to + 75	$^\circ\text{C}$
Storage Temperature Range	-65 to + 150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_A = +25^\circ$, $V_{CC} = 12\text{V}$, $R^* = 20\text{K}$, Test circuit: FIG. 1)

Characteristic	Min	Typ	Max	Units
Supply Voltage Range	6	—	18	Volts
Supply Current	10	14	18	mA
Audio Output ($f_o = 5.5\text{MHz}$, $\Delta f = 50\text{KHz}$, $Q = 45$)		1		Volts R.M.S.
Audio Output ($f_o = 10.7\text{MHz}$, $\Delta f = 75\text{KHz}$, $Q = 35$)		.38		Volts R.M.S.
3dB Limiting ($f_o = 5.5\text{MHz}$, $\Delta f = 50\text{KHz}$, $Q = 45$)		30	60	μV R.M.S.
3dB Limiting ($f_o = 10.7\text{MHz}$, $\Delta f = 75\text{KHz}$, $Q = 35$)		40		μV R.M.S.
A.M. Rejection ($f_o = 5.5\text{MHz}$, R.F. Input: $500\mu\text{V}$)	45			dB
A.M. Rejection ($f_o = 10.7\text{MHz}$, R.F. Input: $500\mu\text{V}$)	40			dB
Volume Control Range	65	75		dB
Output Impedance		2.6		$\text{K}\Omega$

ELECTRICAL CHARACTERISTICS OF AUXILIARY Z DIODE AND TRANSISTOR T45 ($T_A = +25^\circ$)

Characteristic	Min	Typ	Max	Units
Z-Voltage @ 5 mA (Pin 12)	11.2		13.2	Volts
Z-Resistance (Pin 12) @ 1 KHz, 5 mA		15		Ω
T45 Breakdown Voltage V_{CEO}	13			Volts
T45 Current Gain @ $I_C = 1\text{mA}$, $V_{CE} = 5\text{V}$	40	100		—

TBA120C, TBA120D

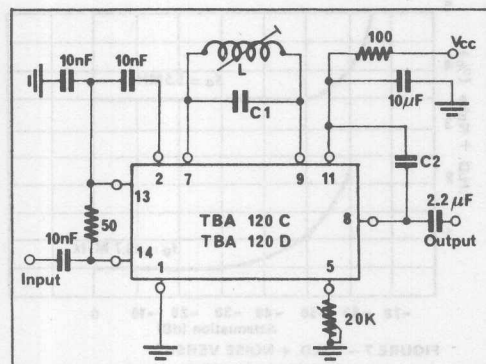


FIGURE 1 - TEST CIRCUIT

COMPONENT VALUES:

	L	C ₁	Q
5.5MHz	.55μH	1.5nF	45
6MHz	.55μH	1.2nF	45
10.7MHz	2.2μH	100pF	35

C₂ = 22nF, together with the integrated resistor of 2.6KΩ (PIN 8) gives the deemphasis and can be reduced if required. For stereo 470pF should be used to provide H.F. decoupling.

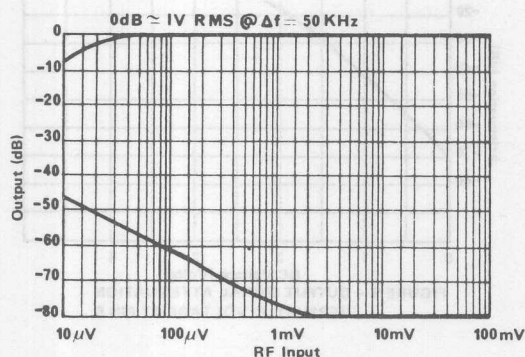


FIGURE 2 - AUDIO OUTPUT AND S/N VERSUS INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz

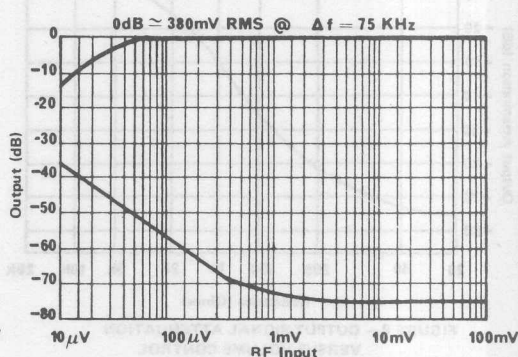


FIGURE 3 - AUDIO OUTPUT AND S/N VERSUS INPUT SIGNAL LEVEL AT 10.7 MHz

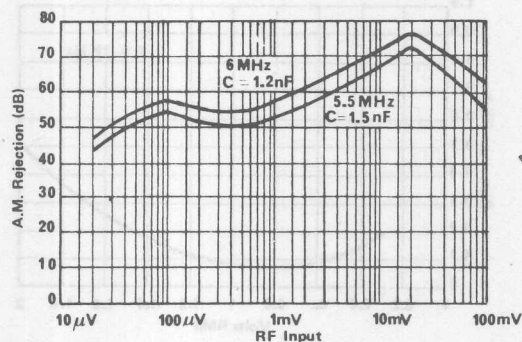


FIGURE 4 - A.M. REJECTION VERSUS INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz (30% A.M., 50 KHz F.M.)

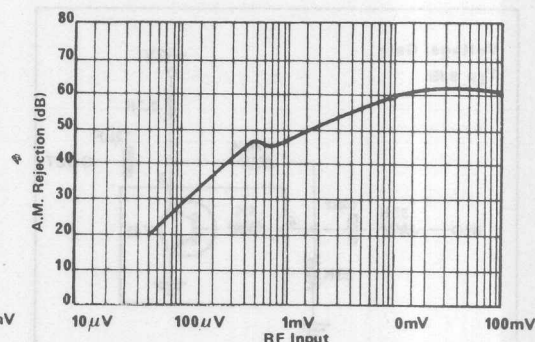


FIGURE 5 - A.M. REJECTION VERSUS INPUT SIGNAL LEVEL AT 10.7MHz (30% A.M., 75KHz FM)

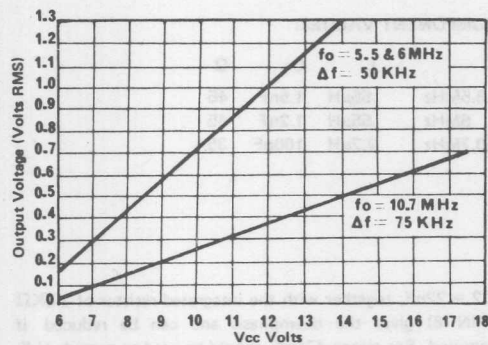


FIGURE 6 - OUTPUT VOLTAGE VERSUS SUPPLY VOLTAGE

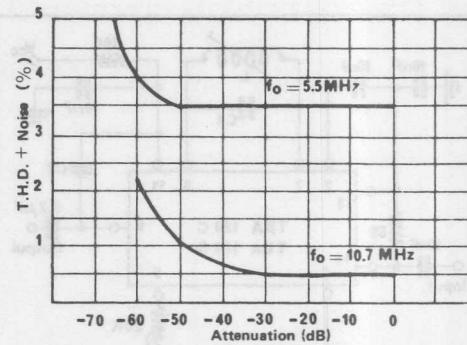


FIGURE 7 - T.H.D. + NOISE VERSUS ATTENUATION (D.C. VOLUME CONTROL)

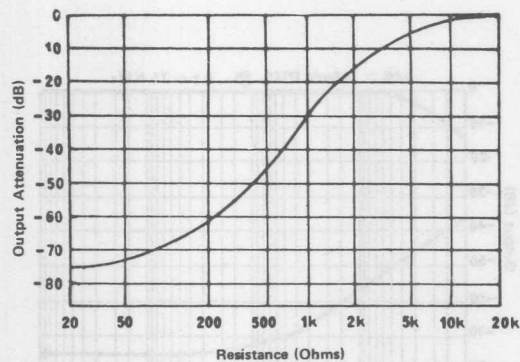


FIGURE 8 - OUTPUT SIGNAL ATTENUATION VERSUS VOLUME CONTROL RESISTANCE

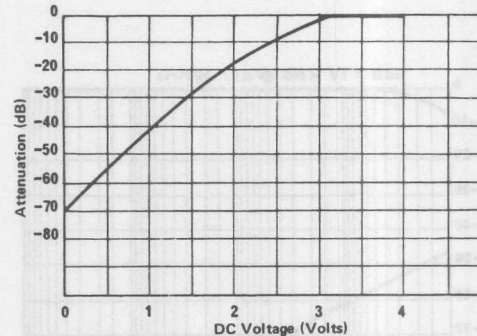


FIGURE 9 - OUTPUT SIGNAL ATTENUATION VERSUS D.C. VOLTAGE AT PIN 5.

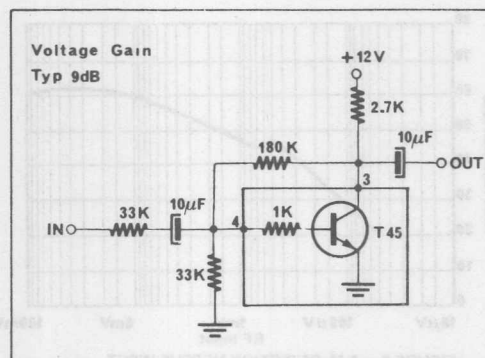


FIGURE 10 - AUDIO PREAMPLIFIER TEST CIRCUIT

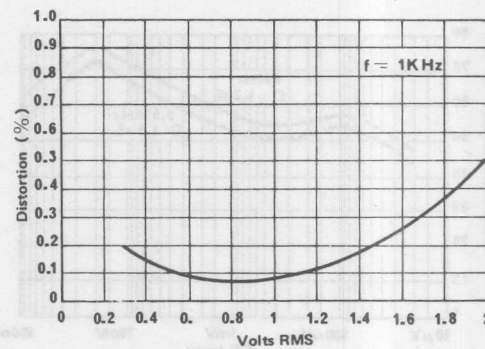


FIGURE 11 - T.H.D. VERSUS OUTPUT VOLTAGE FOR AUDIO PREAMPLIFIER SHOWN IN FIGURE 10.

TBA120C, TBA120D

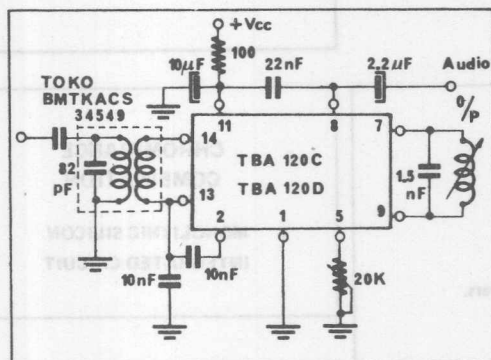


FIGURE 12 — TYPICAL APPLICATION FOR 5.5MHz WITH L-C INPUT FILTER

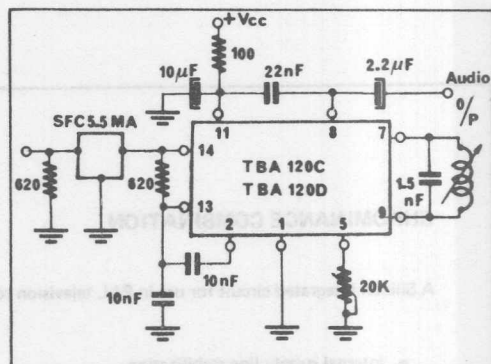


FIGURE 13 — TYPICAL APPLICATION FOR 5.5MHz WITH CERAMIC INPUT FILTER

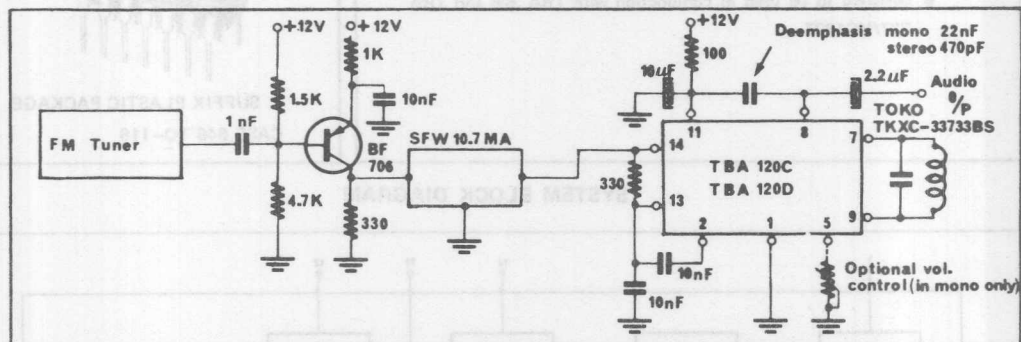
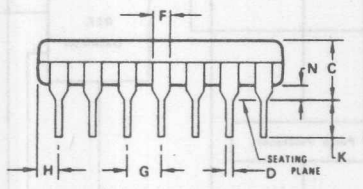
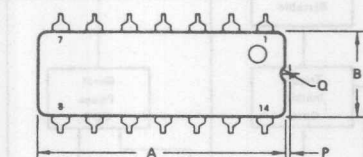


FIGURE 14 — TYPICAL APPLICATION FOR 10.7MHz WITH CERAMIC FILTER

OUTLINE DIMENSIONS



NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 646
PLASTIC PACKAGE

TBA 395

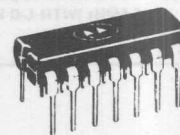
CHROMINANCE COMBINATION

A Silicon integrated circuit for use in PAL television receivers.

- internal supply line stabilization
- 20 dB A.C.C. range
- low external component count
- designed to be used in conjunction with TBA 396 and TBA 327/MC1327

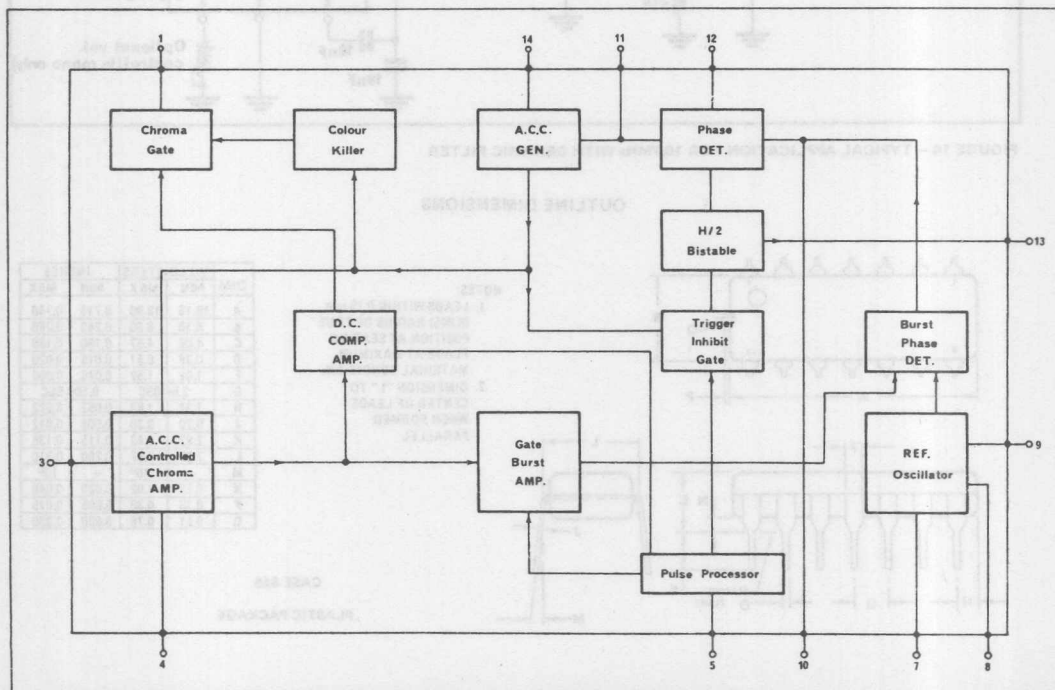
CHROMINANCE COMBINATION

MONOLITHIC SILICON
INTEGRATED CIRCUIT



P. SUFFIX PLASTIC PACKAGE
CASE 646 TO-116

SYSTEM BLOCK DIAGRAM



MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise stated)

Rating	Pin	Value	Unit
Power Supply Current	2	60	mA
D.C. Current Capability of Reference Output	9	4.0	mA
Chrominance Input Voltage	3	1.2	V p.t.p.
Operating Temperature Range		0 to + 70	$^{\circ}\text{C}$
Power Dissipation (Package Limitation)		625	mW
Derate above $T_A = +25^{\circ}\text{C}$		5.0	mW/ $^{\circ}\text{C}$
Storage Temperature Range		- 65 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^{\circ}\text{C}$ unless Otherwise Stated)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	2	7.5	8.4	9.5	V d.c.
Forward Transconductance (Chrominance Output Load = 560 Ω) ($f_{IN} = 4.43\text{ MHz}$)	3-1	6.4			mmho
Chrominance Input Resistance	3	2.0			K Ω
Reference Oscillator Pull-in Range		± 250			Hz
Reference Output	9	400	700		mV
H/2 Bistable Output	13	1.3			V p.t.p.
Burst Gate Operating Voltage	5	2.0		5.0	V
Chrominance Output D.C. Current 1. Colour killer operating 2. Colour killer off		200		4.0	μA μA

APPLICATION NOTES

1. Normal decoupling precautions must be taken. For example pin 2 (8.4 volt circuit supply point) must be decoupled closely to pin 6 (ground) thus preventing sub-carrier components leaking into sensitive areas of the circuit.
2. To prevent the radiation of sub-carrier harmonics, the connection from pin 9 (reference output) and pin 8 (crystal feedback) must be kept as short as possible.
3. The connection from pin 1 (chroma output) should be also as short as possible to prevent capacitive loading of the 1K8 Ω output resistor.

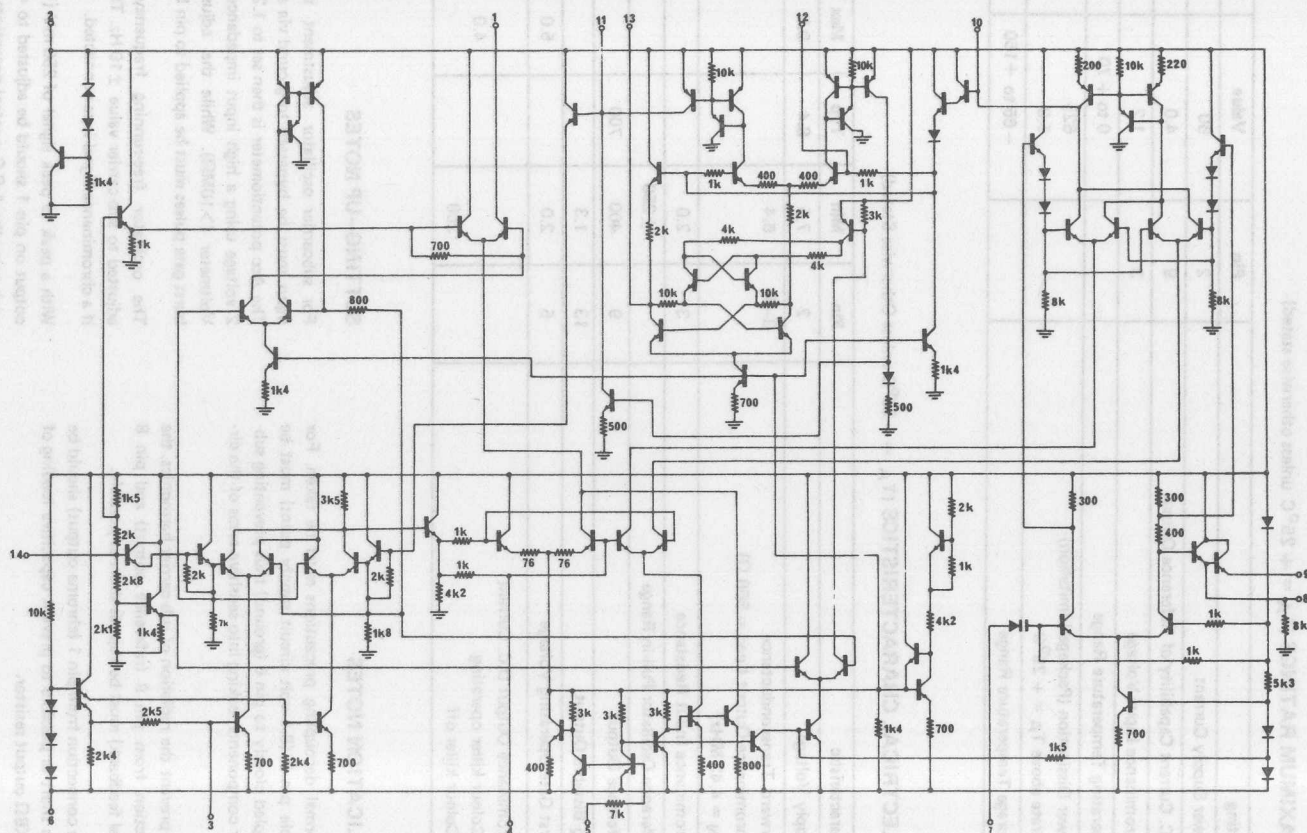
SETTING-UP NOTES

For subcarrier oscillator adjustment the chrominance input must be bypassed to ground via a 1 nf capacitor. The Acc potentiometer is then set to 1.2 volts below pin 2 voltage using a high input impedance oscilloscope or Voltmeter ($>10\text{M}\Omega$). While the adjustment is made burst gate pulses must be applied to pin 5.

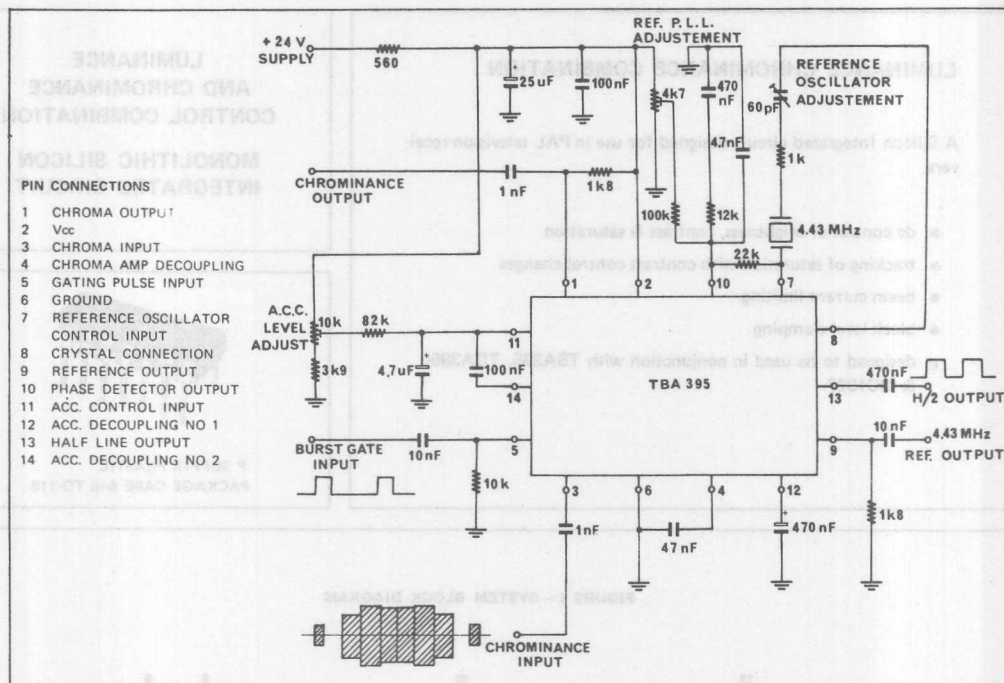
The oscillator free-running frequency can then be adjusted to sub-carrier value $\pm 10\text{ Hz}$. The loop will lock if a chrominance signal is re-connected.

With a peak to peak signal of 250 mV (100 $^{\circ}$ /o bars) the output on pin 1 should be adjusted to 400 mV peak to peak using the A.C.C. control potentiometer.

CIRCUIT SCHEMATIC



TYPICAL CIRCUIT CONFIGURATION



TBA396

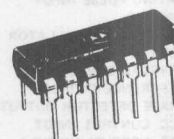
LUMINANCE CHROMINANCE COMBINATION

A Silicon Integrated circuit designed for use in PAL television receivers.

- dc control of brightness, contrast & saturation
- tracking of saturation with contrast control changes
- beam current limiting
- black level clamping
- designed to be used in conjunction with TBA395, TDA3950 & MC1327

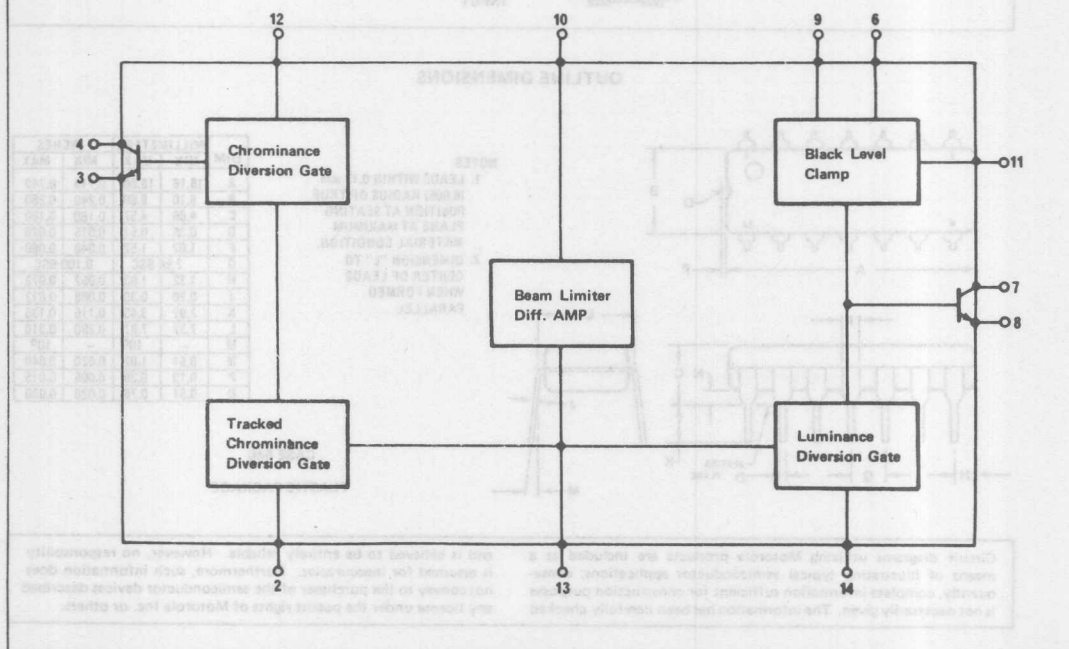
LUMINANCE AND CHROMINANCE CONTROL COMBINATION

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX PLASTIC
PACKAGE CASE 646 TO-116

FIGURE 1 - SYSTEM BLOCK DIAGRAM



MAXIMUM RATINGS ($T_A = + 25^{\circ}\text{C}$ unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	5	20	V d.c.
Luminance Output Collector Voltage	7	30	V d.c.
Luminance Output Emitter Current	8	7.0	mA
Chrominance Output Emitter Current	3	5.0	mA
Operating Temperature Range		0 to + 70	$^{\circ}\text{C}$
Power Dissipation (Package Limitation)		625	mW
Derate above $T_A = - 25^{\circ}\text{C}$		5.0	mW/ $^{\circ}\text{C}$
Storage Temperature Range		- 65 to + 150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^{\circ}\text{C}$ Unless Otherwise Stated)

Characteristic	Pin	Min	Typ	Max	Unit
Luminance Input Resistance	14	100			K Ω
Luminance gain	14-8	0.6	1.0	1.2	
Change of black level with contrast and signal changes (black to white 4 μS gating)				3.0	%
Black level clamp gating pulse	11	50		1000	μA
Contrast control range		35			dB
Saturation control range		35			dB
3dB luminance bandwidth (resistive load)	14-8		7.5		MHz
Video input aperture	14	1.4		3.4	V.p.t.p.
Chrominance input resistance	2	5.0			K Ω
Chrominance voltage gain (Resistive load)	2-3	2.5	3.8	5.0	
Chrominance phase shift with saturation control				± 3	$^{\circ}/\text{o}$
Chrominance phase shift with contrast control				± 3	$^{\circ}/\text{o}$
Chrominance/Luminance tracking error with contrast control				± 2	dB
Threshold of beam limiter	10	1.8	2.0	2.2	V

APPLICATION NOTES

1. The d.c. controls are relatively insensitive to interference if the decoupling associated with these lines is close to the I.C.
2. Good decoupling is required close to the "cold" end of the PAL delay line driving coil to prevent spurious subcarrier components reaching the I.C. supply line.

SETTING UP NOTES

The pre-set brilliance control must be adjusted to give the correct black level of - 16.5 V at pin 7. If the color demodulator IC MC1327 is used to complete the system a voltage of - 7.5 V at the chroma outputs can be set using the same procedure.

This operation must be performed with the brilliance control at the centre of its range.

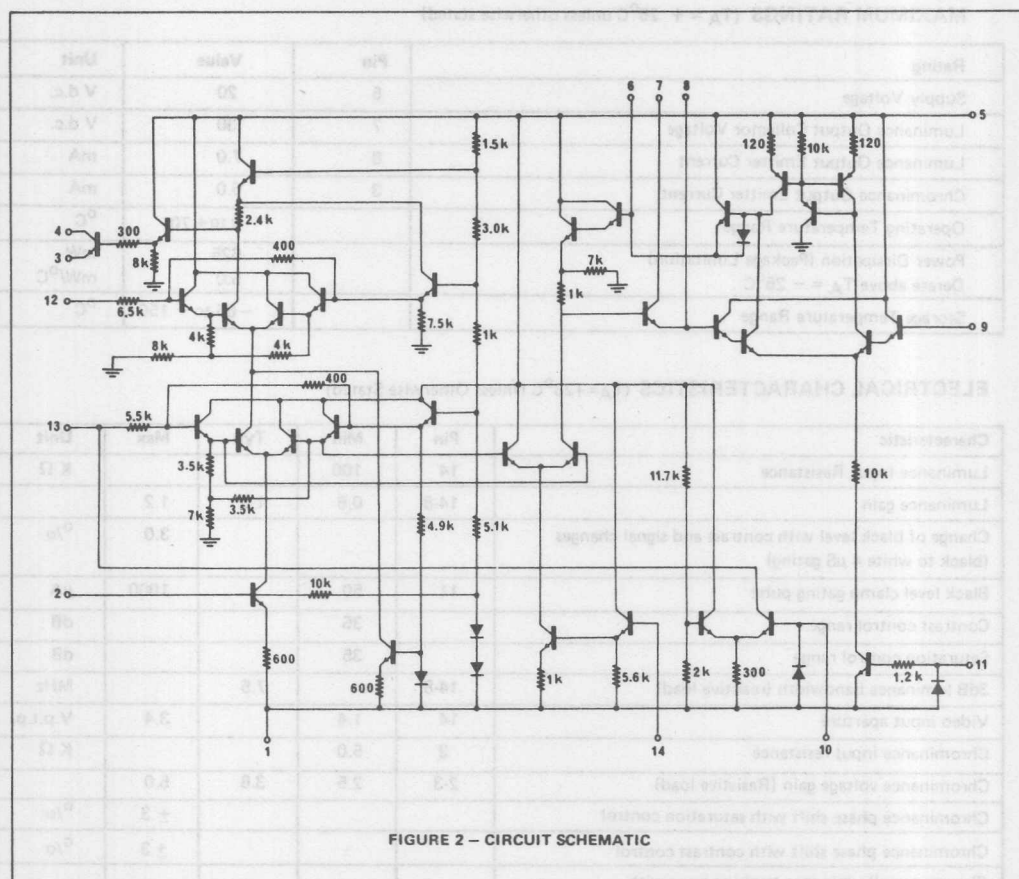
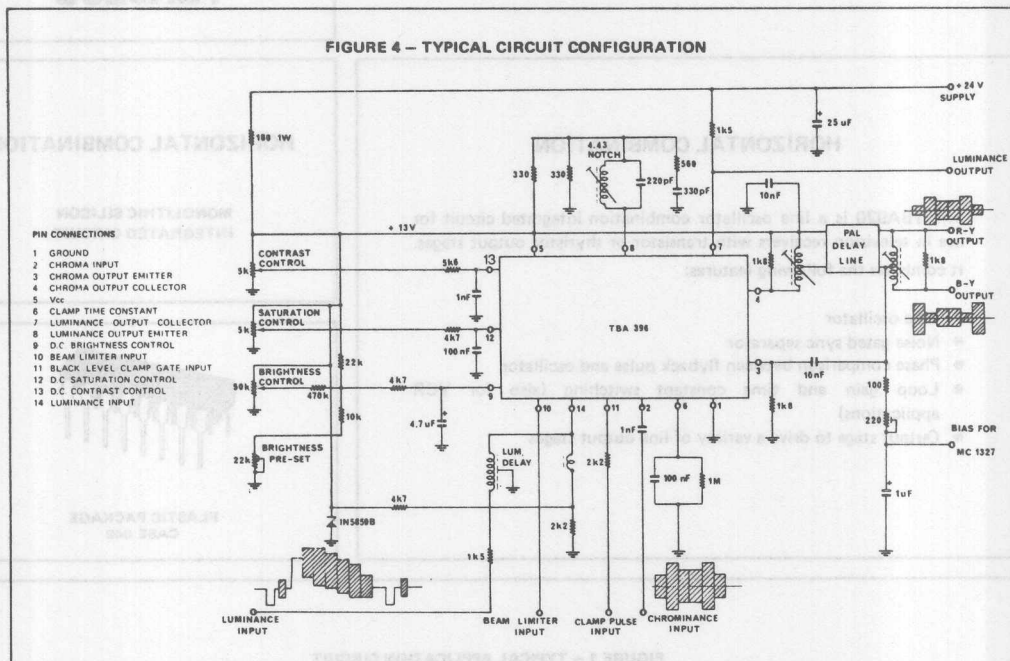
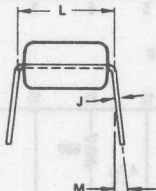
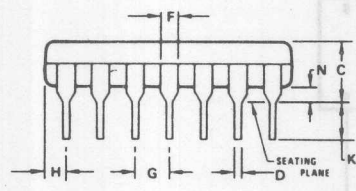
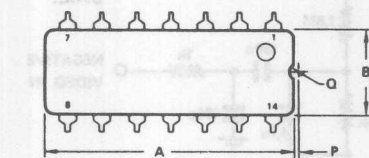


FIGURE 4 - TYPICAL CIRCUIT CONFIGURATION



OUTLINE DIMENSIONS



NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.54	BSC	0.100	BSC
G	1.32	1.83	0.052	0.072
H	0.20	0.30	0.008	0.012
I	2.92	3.43	0.115	0.135
J	7.37	7.87	0.290	0.310
K	—	10 ⁰	—	10 ⁰
L	0.51	1.02	0.020	0.040
M	0.13	0.38	0.005	0.015
N	0.51	0.76	0.020	0.030

CASE 646

PLASTIC PACKAGE

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is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

TBA920 TBA920S

HORIZONTAL COMBINATION

The TBA920 is a line oscillator combination integrated circuit for use in television receivers with transistor or thyristor output stages.

It combines the following features:

- Line oscillator
- Noise gated sync separator
- Phase comparison between flyback pulse and oscillator
- Loop gain and time constant switching (also for VCR applications)
- Output stage to drive a variety of line output stages

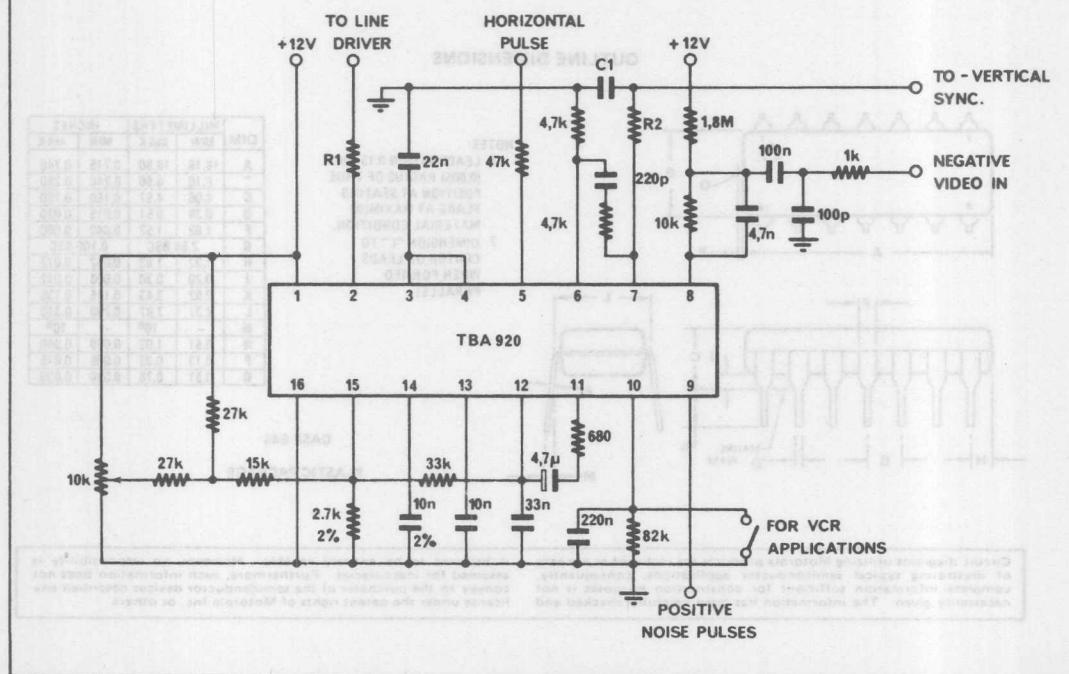
HORIZONTAL COMBINATION

MONOLITHIC SILICON
INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

FIGURE 1 - TYPICAL APPLICATION CIRCUIT



MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise stated)

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	13.2	Vdc
Power Dissipation Derate Above $T_A = +25^\circ\text{C}$	P_D	1.2 10	W mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C)

Characteristic	Pin	Symbol	Min.	Typ.	Max.	Unit
Power Supply Operating Voltage	1	V_{CC}	10.8	12	13.2	Vdc
Current Consumption	1	I_{CC}		24		mA
Input Signals:						
– Video (Positive going sync)	Fig. 1			3		Vp/p
– Noise Gating	9	V_g	0.7			Vp/p
– Flyback Pulse	5	V_5		± 1		Vp/p
Pulse Duration @ 15.625 KHz	5	t_5	10			μsec
Output Signals:						
– Driver Pulse Amplitude	2	V_o		10		Vp/p
Output Current Average	2	I_o			20	mA
Peak					200	mA
– Composite Sync Pulses	7	V_7		10		Vp/p
Oscillator:						
– Free Running Frequency	Fig. 1	f_o		15625		Hz
– Frequency Spread (TBA920)		$\frac{\Delta f_o}{f_o}$			± 5	$\%$
(TBA920S)					± 1.5	$\%$
– Frequency Change, $V_{CC} = 5.0\text{ V}$		$\frac{\Delta f_o}{f_o}$			5	$\%$
– Frequency Control Sensitivity		$\frac{\Delta f_o}{\Delta I}$		16.5		Hz/ μA
– Adjustment Range	Fig. 1			± 10		$\%$
– Influence of Supply Voltage		$\frac{\delta f_o/f_o}{\delta V_{CC}/V_{CC}}$			5	$\%$
Variations @ $V_{CC} = 12\text{ V}$ on frequency						
Control Loop 1:						
– Control Voltage Range	12	V_{12}	0.5		5.8	V
– Control Current						
$V_{10} > 4.4\text{ V}, V_6 > 1.5\text{ V}$	12	I_{12}		± 2		mA p/p
$V_{10} < 2\text{ V}, V_6 > 1.5\text{ V}$				± 6		mA p/p
– Loop Gain of APC System						
Coincidence between sync.		$\frac{\Delta t}{\Delta t}$		1		KHz/ μsec
and Flyback or $V_{10} > 4.5\text{ V}$				3		KHz/ μsec
No coincidence or $V_{10} < 2\text{ V}$						
– Catching and Holding Range		Δf		± 1		KHz

TBA920, TBA920S

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C)

Characteristic	Pin	Symbol	Min.	Typ.	Max.	Unit
Control Loop 2						
— Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse.		td	0		15	μsec
— Static Control Error		$\frac{\Delta t}{\Delta t_{ol}}$			0.5	%
— Output Current at Flyback		I _f		±0.7		mA
Phase Relations						
— Phase relation between leading edge of sync pulse and middle of flyback pulse		t		4.9 ¹		μsec
— Tolerance of Phase Relation (TBA920) (TBA 920S)		t			0.7 0.4	μsec
— Voltage for T ₂ = 12 to 32 μsec	3	V ₃	6		8	V
— Adjustment Sensitivity	3			10		μsec/V
— Input Current	3	I ₃			2	μA

¹With leading edge synchronization as shown in circuit diagram Fig. 1

PACKAGE DIMENSIONS

**PLASTIC PACKAGE
CASE 648**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

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TBA2110

Advance Information

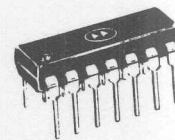
FSK DEMODULATOR

The TBA 2110 FSK Demodulator is designed for frequency detection in PCM Remote Control systems for TV applications. It contains an infrared amplifier, multiplier and VCO forming a phase locked loop system. It is specifically designed for use with the MC6203 and MC6215 remote control receivers.

- Limiting with 20 μ V signal
- Wide range of supply voltages (10 to 20 V)
- No adjustments

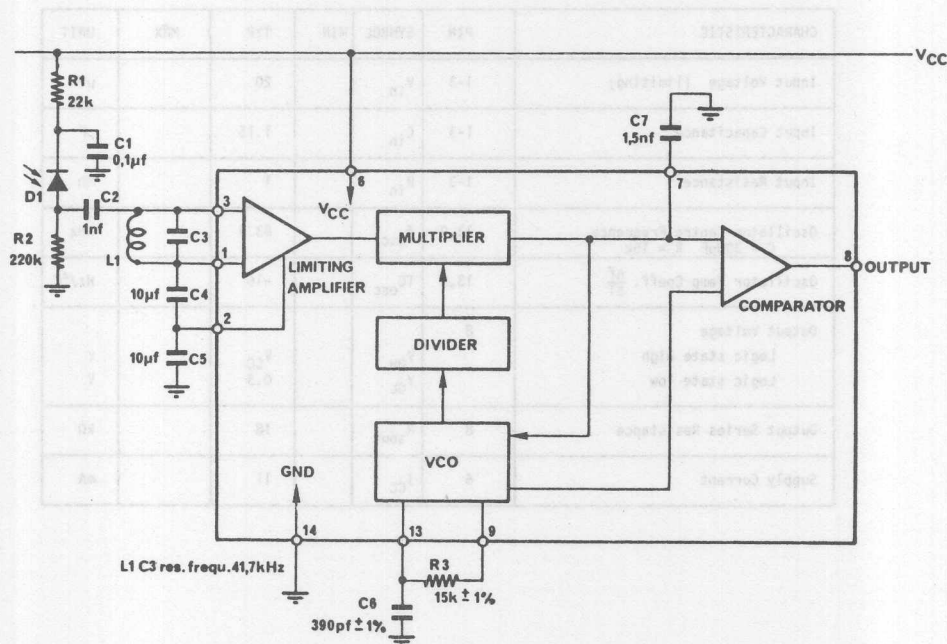
FSK DEMODULATOR

MONOLITHIC SILICON
INTEGRATED CIRCUIT



P SUFFIX PLASTIC
PACKAGE CASE 646 TO-116

FIGURE 1 - SYSTEM BLOCK DIAGRAM



This is advance information on a new introduction and specifications are subject to change without notice.

TBA2110

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless other wise noted.)

RATING	SYMBOL	VALUE	UNIT
Power Supply Voltage	V_{CC}	20	V
Input Voltage	V_{in}	0.7	V (rms)
Power Dissipation (Package Limit)	P_D	1.25	W
Derate above $+25^\circ\text{C}$	$1/Q_{JA}$	10	mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	0 - 75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 - 150	$^\circ\text{C}$

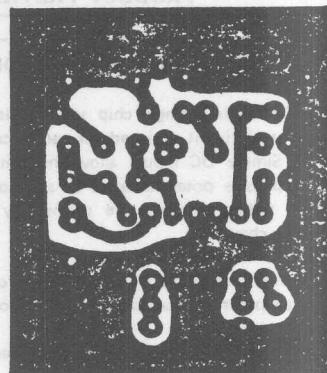
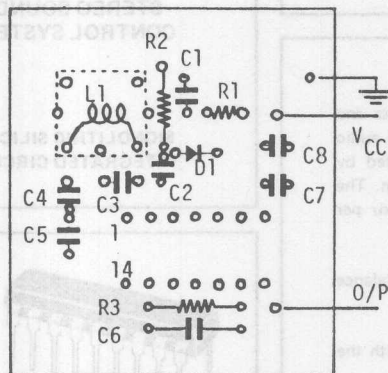


FIGURE 1 - SYSTEM BLOCK DIAGRAM

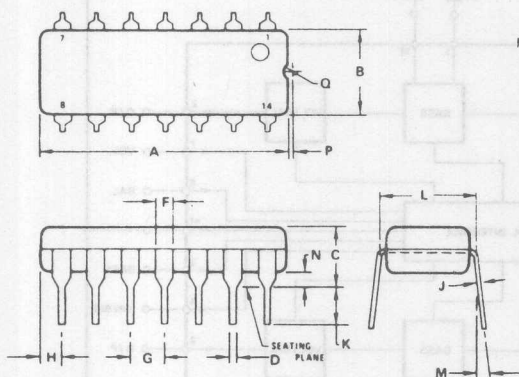
ELECTRICAL CHARACTERISTICS: ($T_A = +25^\circ$, $V_{CC} = 15\text{ V}$)

CHARACTERISTIC	PIN	SYMBOL	MIN	TYP	MAX	UNIT
Input Voltage (limiting)	1-3	V_{in}		20		μV
Input Capacitance	1-3	C_{in}		1.15		pF
Input Resistance	1-3	R_{in}		1		M Ω
Oscillator Centre Frequency $C = 390\text{pF}$ $R = 15\text{k}$	13,9	f_{osc}		83.4		kHz
Oscillator Temp Coeff. $\frac{\Delta f}{\Delta T}$	13,9	TC_{osc}		-16		Hz/ $^\circ\text{C}$
Output Voltage Logic state high Logic state low	8	V_{OH} V_{OL}		V_{CC} 0.3		V V
Output Series Resistance	8	R_{sout}		18		k Ω
Supply Current	6	I_{CC}		11		mA

figure 2 - APPLICATION INFORMATION

Possible PCB and component layout, foil side - not to scale
for use with the Toko coil type SH-10

OUTLINE DIMENSIONS



NOTES

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	10°		10°	
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 646
PLASTIC PACKAGE

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TCA 5500

PRODUCT PREVIEW

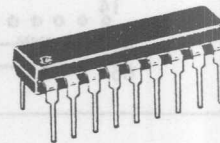
STEREO SOUND CONTROL SYSTEM

The TCA5500 is a single chip stereo balance, volume, bass and treble control circuit designed for use in car radios, TV and audio systems. Simple DC inputs allow the control to be effected by four inexpensive potentiometers or a remote control system. The bass and treble responses are defined by a single capacitor per control per channel.

- Four high impedance DC controls — Vol, Bass, Treble, Balance
- A single external capacitor defines each tone control's characteristic
- Low distortion, 0.1% at nominal input level, 12dB gain with the tone controls flat
- Channel separation better than 45dB
- Wide power supply tolerance, 8 to 18V DC
- ± 14 dB of tone control
- More than 75dB of volume control
- Wide dynamic range: 25mV to 150mV RMS input signal
- Low output impedance
- Easily added loudness compensation

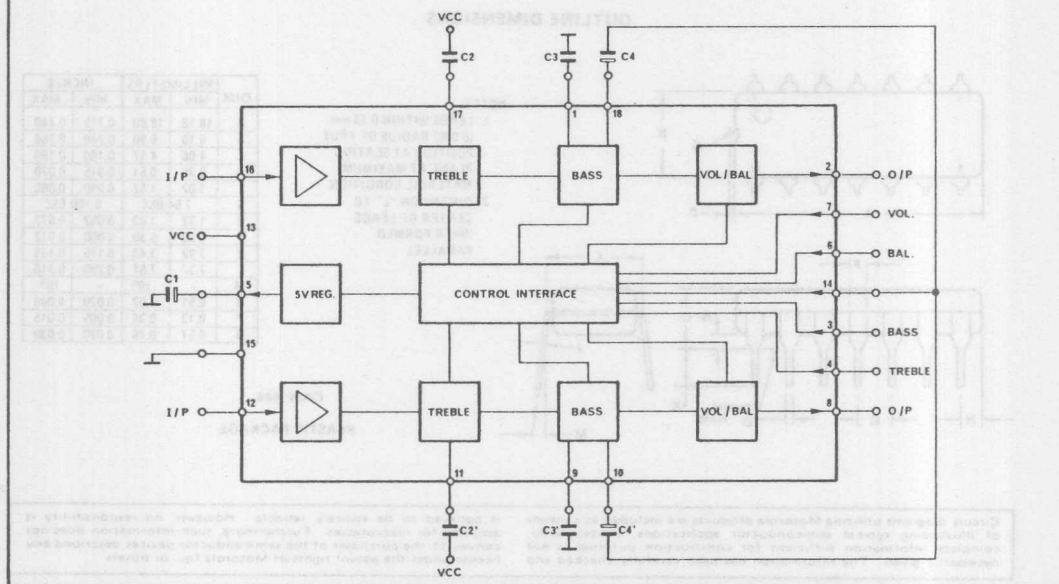
STEREO SOUND CONTROL SYSTEM

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 707

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



This is advance information on a new introduction and specifications are subject to change without notice

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$)

Rating	Value	Unit
Power Supply Voltage	18	Volts
Power Dissipation (Package Limitation)	1800	mW
Derate above $T_A = +25^{\circ}\text{C}$	15	mW/ $^{\circ}\text{C}$
Operating Temperature Range (Ambient)	-40 to +85	$^{\circ}\text{C}$
Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$, $V_{CC} = 8\text{V DC}$)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	13	8		18	V DC
Supply Current (at Min Gain)			30		mA
(at Max Gain)			15		mA
Regulated Output Voltage ¹	5		5		V
Current				3	mA
Input Levels (at Max Gain) (with reduced gain) ³	12, 16		25	150	mV RMS mV RMS
Input Impedance	12, 16		100		k Ω
Output Impedance	2, 8		100		Ω
Tone Control Range (at 100Hz & 10kHz) ²					
with pins 3 & 4 at 0V	3, 4		-14		dB
with pins 3 & 4 at 2V			0		dB
with pins 3 & 4 at 4V			+14		dB
Balance Control Range (Constant Power Law) Voltage on pin 6 for balanced gain	6	-40		+3	dB V
Volume Control Range	7		80		dB
with pin 7 at 0V			+12		dB
with pin 7 at 2.5V			-18		dB
with pin 7 at 5V			-68		dB
Control Input Currents	3, 4, 6, 7			1	μA
Channel Separation		45			dB
Distortion (at 1kHz) at 100mV RMS output ³			0.1		%
Signal : Noise Ratio 50Hz to 15kHz, 12dB gain, tone controls flat			70		dB
Noise Level 50Hz to 15kHz, min gain			10		$\mu\text{V RMS}$

NOTES:

- 1 The control potentiometers should be connected to this point, see figure 5.
- 2 These figures are functions of the capacitors on pins 1, 9, 10, 11, 17 & 18. See the application diagram, figure 5.
- 3 The input level may be increased to 150mV RMS but the user controls must be adjusted to ensure that the output level does not exceed 100mV RMS.

FIGURE 2 — TONE CONTROLS
MAX BOOST, CUT / CONTROL VOLTAGE

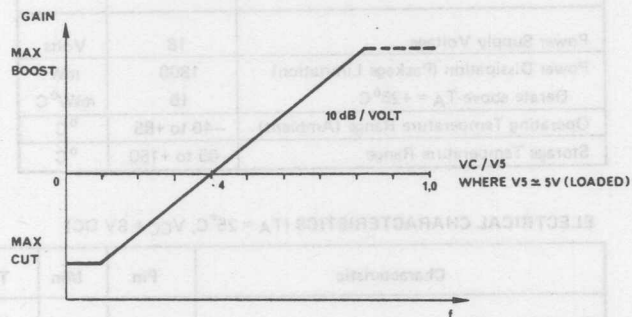
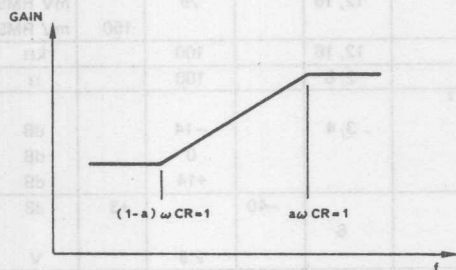


FIGURE 3 — TREBLE CONTROL LAW



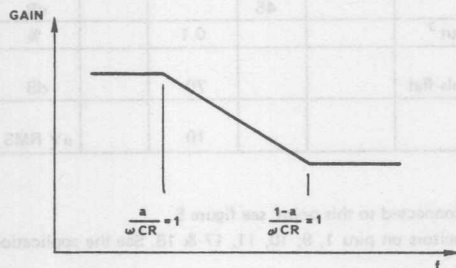
$$\text{Gain} = \frac{1 + (1-a)j\omega CR}{1 + aj\omega CR}$$

Where $R = 2.4k\Omega$ (on chip)
and $C = C$ pins 11 & 17

When $a = 0.1 = \text{max Treble boost}$

When $a = 0.8 = \text{max Treble cut}$

FIGURE 4 — BASS CONTROL LAW



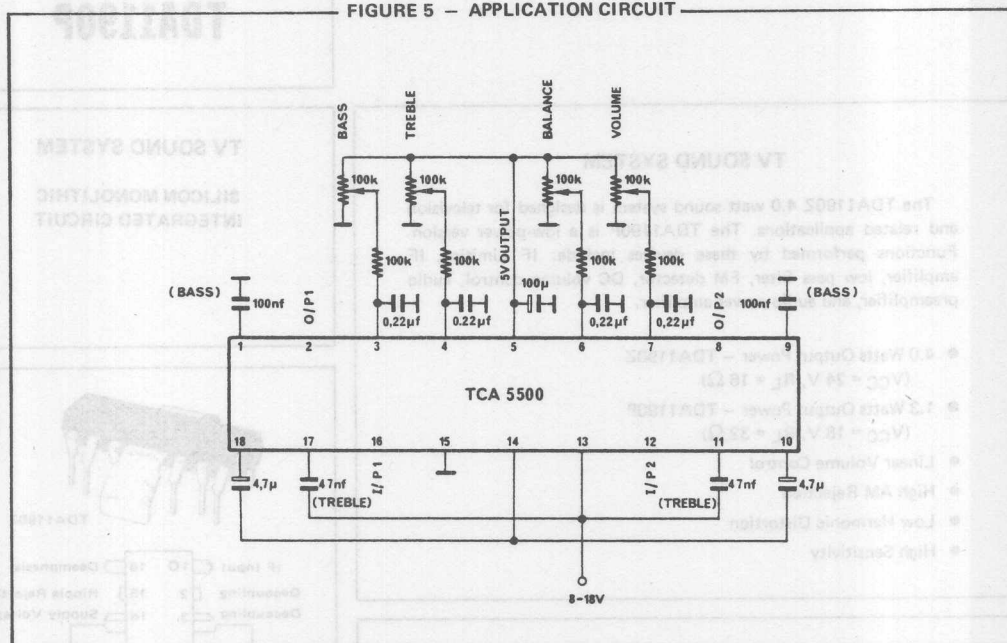
$$\text{Gain} = \frac{1 + \frac{1-a}{j\omega CR}}{1 + \frac{a}{j\omega CR}}$$

Where $R = 4k\Omega$ (on chip)
and $C = C$ pins 1 & 9

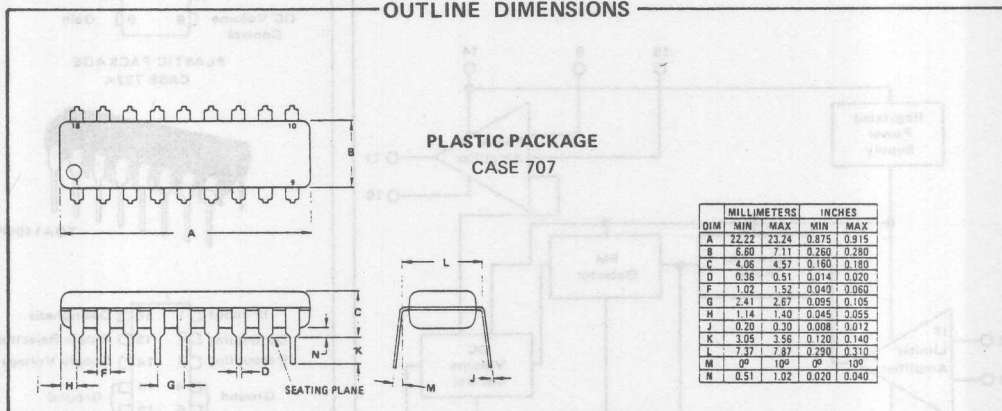
When $a = 0.1 = \text{max Bass boost}$

When $a = 0.8 = \text{max Bass Cut}$

FIGURE 5 — APPLICATION CIRCUIT



OUTLINE DIMENSIONS



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However,

no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

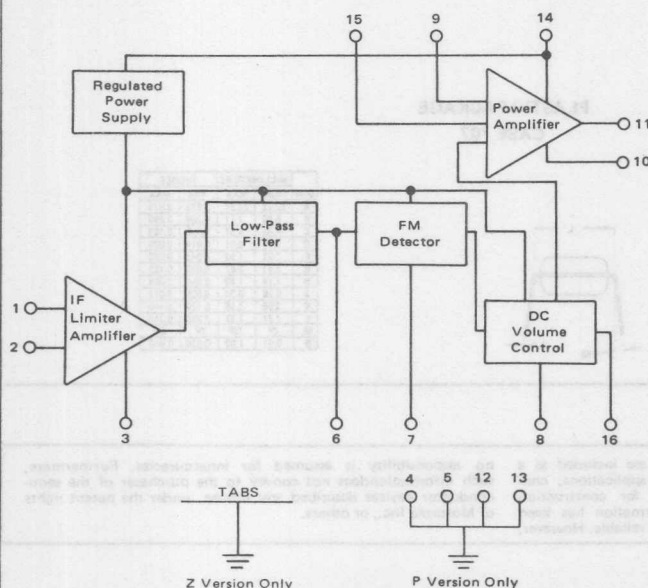
TDA1190Z TDA1190P

TV SOUND SYSTEM

The TDA1190Z 4.0 watt sound system is designed for television and related applications. The TDA1190P is a low-power version. Functions performed by these devices include: IF limiting, IF amplifier, low pass filter, FM detector, DC volume control, audio preamplifier, and audio power amplifier.

- 4.0 Watts Output Power – TDA1190Z
($V_{CC} = 24\text{ V}$, $R_L = 16\ \Omega$)
- 1.3 Watts Output Power – TDA1190P
($V_{CC} = 18\text{ V}$, $R_L = 32\ \Omega$)
- Linear Volume Control
- High AM Rejection
- Low Harmonic Distortion
- High Sensitivity

BLOCK DIAGRAM

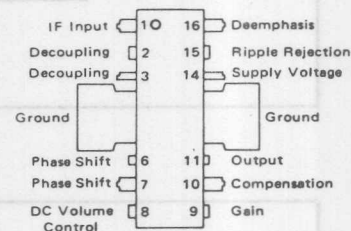


TV SOUND SYSTEM

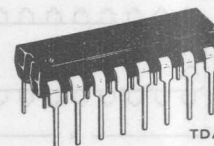
SILICON MONOLITHIC INTEGRATED CIRCUIT



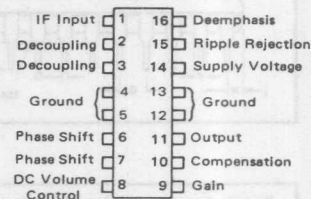
TDA1190Z



PLASTIC PACKAGE
CASE 722A



TDA1190P



PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

Device	Temperature Range	Package
TDA1190Z, P	0 to +75°C	Plastic

DS 9438 R1

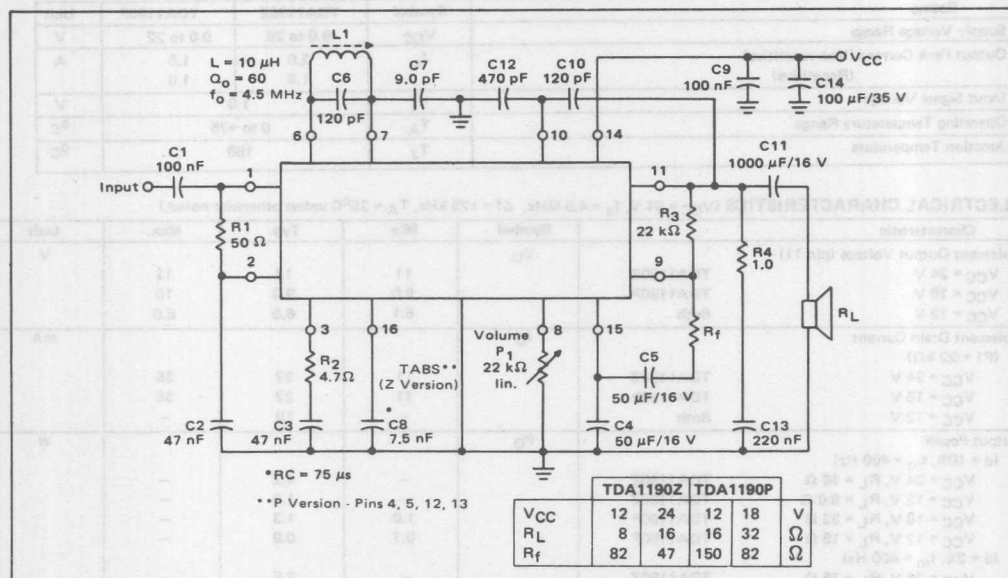
MAXIMUM RATINGS

Rating	Symbol	TDA1190Z	TDA1190P	Unit
Supply Voltage Range	V_{CC}	9.0 to 28	9.0 to 22	V
Output Peak Current (Non-repetitive) (Repetitive)	I_O	2.0 1.5	1.5 1.0	A
Input Signal Voltage	V_I	1.0		V
Operating Temperature Range	T_A	0 to +75		°C
Junction Temperature	T_J	150		°C

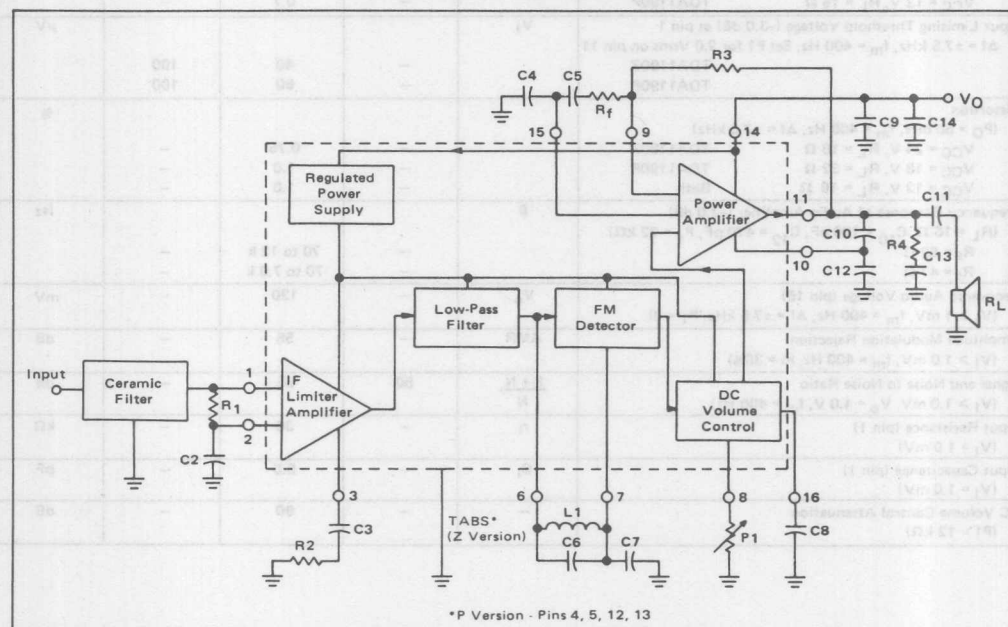
ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ V, $f_0 = 4.5$ MHz, $\Delta f = \pm 25$ kHz, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ.	Max.	Unit
Quiescent Output Voltage (pin 11) $V_{CC} = 24$ V $V_{CC} = 18$ V $V_{CC} = 12$ V	V_O TDA1190Z TDA1190P Both	11 8.0 5.1	12 9.0 6.0	13 10 6.9	V
Quiescent Drain Current ($P_1 = 22$ k Ω) $V_{CC} = 24$ V $V_{CC} = 18$ V $V_{CC} = 12$ V	I_D TDA1190Z TDA1190P Both	11 11 —	22 22 19	35 35 —	mA
Output Power ($d = 10\%$, $f_m = 400$ Hz) $V_{CC} = 24$ V, $R_L = 16$ Ω $V_{CC} = 12$ V, $R_L = 8.0$ Ω $V_{CC} = 18$ V, $R_L = 32$ Ω $V_{CC} = 12$ V, $R_L = 16$ Ω ($d = 2\%$, $f_m = 400$ Hz) $V_{CC} = 24$ V, $R_L = 16$ Ω $V_{CC} = 12$ V, $R_L = 8.0$ Ω $V_{CC} = 18$ V, $R_L = 32$ Ω $V_{CC} = 12$ V, $R_L = 16$ Ω	P_O TDA1190Z TDA1190Z TDA1190P TDA1190P TDA1190Z TDA1190Z TDA1190P TDA1190P	— — 1.0 0.7 — — — — —	4.2 1.5 1.3 0.9 3.5 1.4 1.0 0.7 —	— — — — — — — — —	W
Input Limiting Threshold Voltage (-3.0 dB) at pin 1 $\Delta f = \pm 7.5$ kHz, $f_m = 400$ Hz, Set P_1 for 2.0 Vrms on pin 11	V_I TDA1190Z TDA1190P	— —	40 60	100 100	μV
Distortion ($P_O = 50$ mW, $f_m = 400$ Hz, $\Delta f = \pm 7.5$ kHz) $V_{CC} = 24$ V, $R_L = 16$ Ω $V_{CC} = 18$ V, $R_L = 32$ Ω $V_{CC} = 12$ V, $R_L = 16$ Ω	B TDA1190Z TDA1190P Both	— — —	0.75 1.0 1.0	— — —	%
Frequency Response of Audio Amplifier (-3.0 dB) ($R_L = 16$ Ω , $C_{10} = 120$ pF, $C_{12} = 470$ pF, $P_1 = 22$ k Ω) $R_f = 82$ Ω $R_f = 47$ Ω	B	— — —	70 to 12 k 70 to 7.0 k	— —	Hz
Recovered Audio Voltage (pin 16) ($V_I \geq 1$ mV, $f_m = 400$ Hz, $\Delta f = \pm 7.5$ kHz, $P_1 = 0$)	V_O	—	120	—	mV
Amplitude Modulation Rejection ($V_I \geq 1.0$ mV, $f_m = 400$ Hz, $m = 30\%$)	AMR	—	55	—	dB
Signal and Noise to Noise Ratio ($V_I \geq 1.0$ mV, $V_O = 4.0$ V, $f_m = 400$ Hz)	$\frac{S+N}{N}$	50	65	—	dB
Input Resistance (pin 1) ($V_I = 1.0$ mV)	r_i	—	30	—	k Ω
Input Capacitance (pin 1) ($V_I = 1.0$ mV)	C_i	—	5.0	—	pF
DC Volume Control Attenuation ($P_1 = 12$ k Ω)	—	—	90	—	dB

TEST CIRCUIT

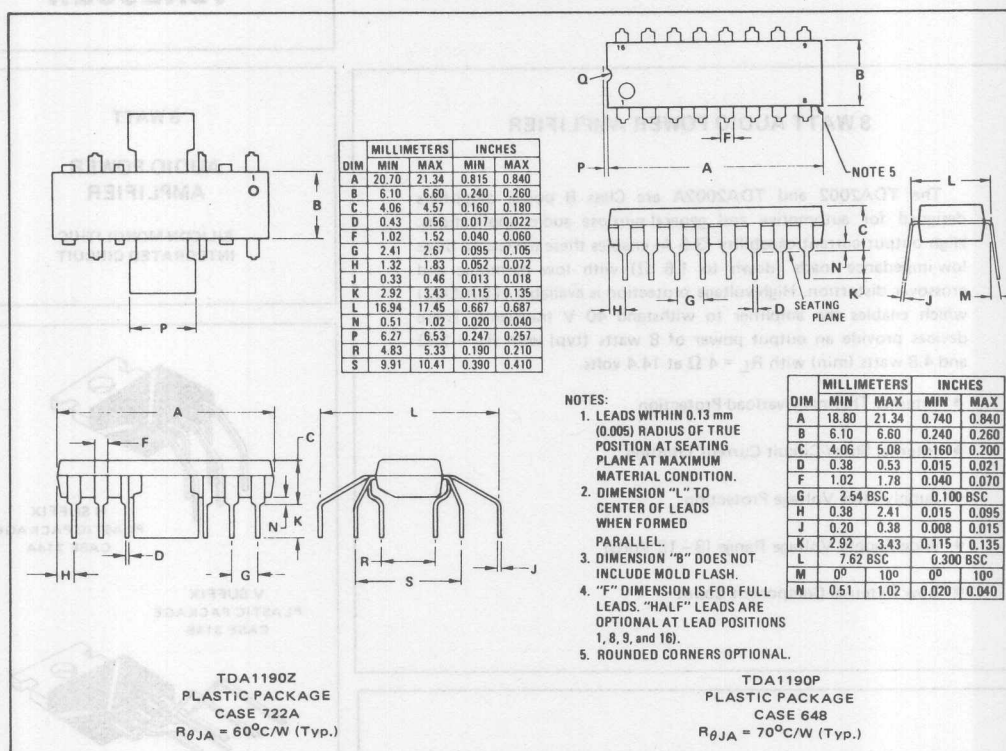


TYPICAL CIRCUIT CONFIGURATION



TDA1190Z, TDA1190P

OUTLINE DIMENSIONS



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_D(T_A) = \frac{T_J(\text{max}) - T_A}{R_{\theta JA}(\text{Typ})}$$

Where: $P_D(T_A)$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than

the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_J(\text{max})$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(\text{Typ})$ = Typical Thermal Resistance Junction to Ambient

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is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

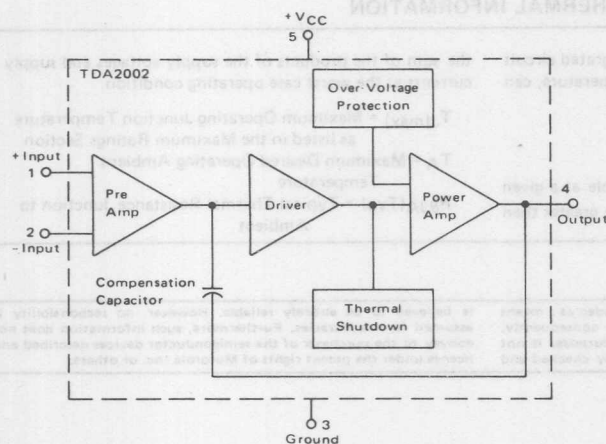
TDA2002 TDA2002A

8 WATT AUDIO POWER AMPLIFIER

The TDA2002 and TDA2002A are Class B power amplifiers designed for automotive and general-purpose audio applications. High output current capability (3.5 A) enables these devices to drive low-impedance loads (down to 1.6Ω) with low harmonic and crossover distortion. High-voltage protection is available (TDA2002) which enables the amplifier to withstand 40 V transients. These devices provide an output power of 8 watts (typ) with $R_L = 2 \Omega$ and 4.8 watts (min) with $R_L = 4 \Omega$ at 14.4 volts.

- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Supply Over Voltage Protection
- Wide Supply Voltage Range (8–18 Volts)
- Low External Component Count

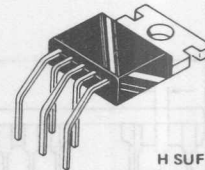
BLOCK DIAGRAM



8 WATT

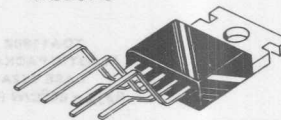
AUDIO POWER AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

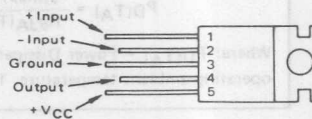


H SUFFIX
PLASTIC PACKAGE
CASE 314A

V SUFFIX
PLASTIC PACKAGE
CASE 314B



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Plastic Package
TDA2002H *	-40 to +85°C	Case 314A
TDA2002V *	-40 to +85°C	Case 314B
TDA2002AH	-40 to +85°C	Case 314A
TDA2002AV	-40 to +85°C	Case 314B

*High Voltage

TDA2002, TDA2002A

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$)

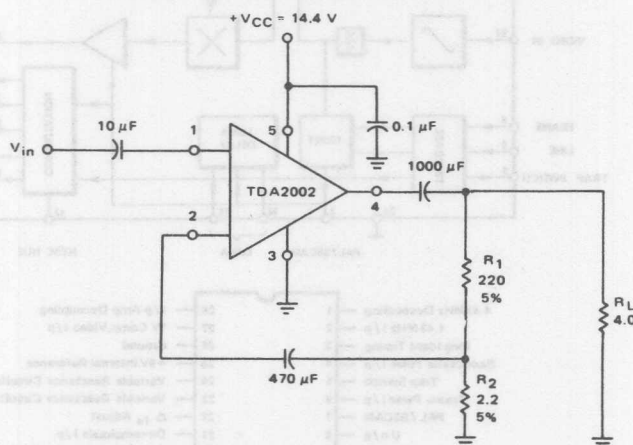
Rating	Value	Unit
Peak Supply Voltage		V
TDA2002 (Transients of 50 ms or less)	40	
TDA2002/2002A (Steady State)	28	
Operating Power Supply Voltage	18	V
Peak Output Current (Nonrepetitive)	4.5	A
(Repetitive)	3.5	
Junction Temperature	150	$^\circ\text{C}$
Storage Temperature Range	-65 to +150	$^\circ\text{C}$
Operating Temperature Range	-40 to +85	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 14.4\text{ Vdc}$, $R_L = 4.0\ \Omega$, $f = 1.0\text{ kHz}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)*

Characteristic	Symbol	Min	Typ	Max	Unit
Quiescent Drain Current ($V_{in} = 0$)	I_D	—	—	80	mA
Quiescent Output Voltage ($V_{in} = 0$)	V_O	6.4	7.2	8.0	V
Power Output — 10% Distortion ($V_{CC} = 14.4\text{ V}$, $R_L = 4.0\ \Omega$) ($V_{CC} = 14.4\text{ V}$, $R_L = 2.0\ \Omega$) ($V_{CC} = 16\text{ V}$, $R_L = 4.0\ \Omega$) ($V_{CC} = 16\text{ V}$, $R_L = 2.0\ \Omega$)	P_O	4.8 7.0 — —	5.2 8.0 6.5 10	— — — —	W
Input Resistance (Pin 1)	r_i	70	150	—	k Ω
Equivalent Input Noise Voltage ($R_S = 0$, Bandpass = 20 Hz to 15 kHz)	e_n	—	4	—	μV
Equivalent Input Noise Current ($R_S = 0$, Bandpass = 20 Hz to 15 kHz)	i_n	—	0.1	—	nA
Power Supply Rejection Ratio ($f_{\text{ripple}} = 100\text{ Hz}$)	P_{SRR}	30	35	—	dB

* See Test Circuit — Figure 1.

FIGURE 1 — APPLICATION AND TEST CIRCUIT



TDA 3030

ADVANCE INFORMATION

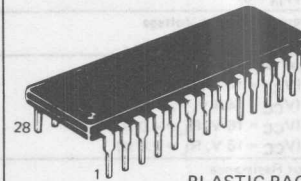
SECAM ADAPTER

The TDA3030 SECAM adapter is designed to expand the facilities offered by the TDA3300 PAL/NTSC colour processor to give a fully multistandard TV colour processing system.

- Expands the TDA3300 and enables it to accept all SECAM standards
- On-chip NTSC hue control
- Automatic, on-chip PAL-SECAM switching
- Low power dissipation, typically 450mW
- Single 12V supply
- Can be easily retrofitted without further adjustment

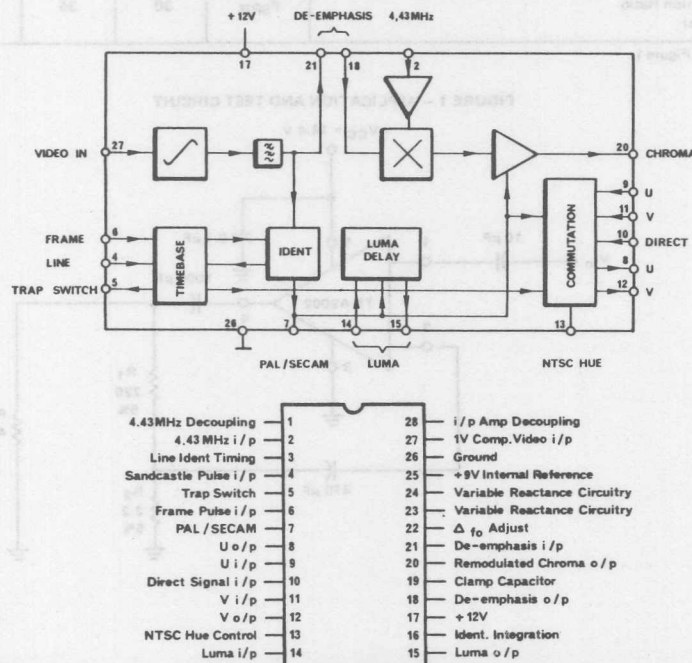
SECAM ADAPTER

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 710-02

FIGURE 1 — SIMPLIFIED BLOCK DIAGRAM AND PINOUT



This is advance information and specifications are subject to change without notice.

Issue 3 November 1980

MAXIMUM RATINGS (T_A = +25°C)

Rating	Value	Unit
Supply Voltage	14	V DC
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise stated)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	17	10.8	12	13.2	V DC
Supply Current		—	36	48	mA
Chroma Input: Voltage	27	30	—	300	mV p-p
Impedance		4	7	—	kΩ
4.43MHz Input: Voltage	2	30	—	300	mV
Impedance		4	7	—	kΩ
Luma Input: Voltage	14	—	1	2	V p-p
Gain	14, 15	-2	0	+1	dB
Bandwidth (-3 dB)	14, 15	6	10	—	MHz
Delay (SECAM)	14, 15	140	200	280	ns
Delay Enable	7	0.2	—	1	mA
Remodulator Output Voltage: DR	20	—	450	—	mV p-p
DB		—	350	—	mV p-p
Burst		65	75	85	mV p-p
DC Output Level: PAL Mode		—	2.0	—	V
SECAM Mode		—	8.0	—	V
Output Current		—	—	2	mA
Line-by-line Offset, if B-Y Line is Adjusted to Zero		—	—	10	kHz
Output Impedance (I ₂₀ = 1.0mA)		—	—	250	Ω
Commutator Gain: PAL		—	0	—	dB
SECAM DR	9, 10	5	6	7	dB
SECAM DB	11	2	3	4	dB
Ratio Error (DR: DB)		—	—	10	%
NTSC Line	8, 12	—	3	—	dB
NTSC Burst (at 0° Phase)		—	-0.5	—	dB
SECAM Subcarrier Output: Remodulator	20	—	1.5	—	mV p-p
(both with 100mV p-p chroma i/p) Commutator	8, 12	—	2.0	—	mV p-p
Sandcastle Pulse Input: Voltage	4	3	—	VCC	V
Resistance		10	—	—	kΩ
Frame Pulse Input: Voltage	6	7	—	VCC	V
Resistance		10	—	—	kΩ
NTSC Hue Control Voltage: PAL/SECAM	13	9	—	VCC	V
NTSC/SECAM		—	—	5	V
Hue Control Output Phase Burst/Line	8, 12	±45	—	—	Deg
Discriminator Output	21	—	1	—	V/MHz
Linearity ($m \frac{S_{min}}{S_{max}} \times 100\%$)		90	—	—	%
Ident Capacitor: Kill-level	16	—	7.0	—	V
Unkill-level		—	7.5	—	V
Internal Reference Voltage	25	—	9	—	V
Ident Timing Output Current	3	—	—	5	mA

CIRCUIT OPERATION

The circuit operation can be followed by reference to the block diagram, Figure 1. It must be stressed that the TDA3030 is a SECAM adapter for use with the TDA3300 PAL system and not a 'stand alone' device.

THE LUMA CHANNEL

The luma channel of the TDA3030 is an electronically controlled 0/200ns delay circuit. All luma signals pass through this circuit, but it is switched to the delay mode only when a SECAM transmission is identified, or if (for NTSC reception, for example) the PAL/SECAM output, pin 7, of the TDA3030 is forced high.

THE CHROMA CHANNEL

After passing through the cloche filter the frequency modulated SECAM signal is discriminated and fed to a low pass filter to remove any residual high frequency components. One output from the filter is de-emphasised and remodulated in a balanced modulator as sequential AM on a 4.43MHz subcarrier. In this stage, too, a 4.43MHz burst is added to the signal to allow for ACC action in the TDA3300. The remodulated chroma signal is fed to the chroma input of the TDA3300 where it passes through the saturation and contrast controls before being applied to the chroma delay line.

In a PAL/SECAM system the output of the chroma delay line is connected to the commutator of the TDA3300

which handles all signals and feeds them, appropriately processed, to the U and V inputs of the TDA3300.

The input signals are treated differently, depending on whether they are PAL, NTSC or SECAM.

In the PAL mode, i.e. when no SECAM identification is present, the commutator is inactive. Thus, signals arriving at the TDA3030's U and V inputs are steered directly to the respective outputs.

If a SECAM signal is identified the commutator is switched to act as such, alternately steering the delayed and direct signals to the U and V outputs. At the same time the circuit corrects the matrixing to the PAL ratio.

When the system is switched to NTSC the direct input is fed to both the U and V outputs. In this mode the phasing between the burst and the line can be varied according to the voltage applied to the hue control.

With the TDA3030 both line and frame SECAM identification are possible.

An output from the low pass filter is taken to the identification circuitry which is active during the line and frame blanking periods.

This circuit detects the sequence of the 4.40625MHz and 4.25MHz bursts, representing the R-Y and B-Y signals respectively, during the frame period or the sequence of 'bottles' transmitted during the frame blanking interval.

Given correct identification, the ident circuitry will activate the TDA3030's luma delay and remodulator output and set the commutation circuit to the SECAM mode.

INPUT/OUTPUT FUNCTIONS

4.43MHz — (pins 1 & 2) Pin 1 is decoupled to ground while the signal is fed to pin 2 via a phase advance network (see the application circuit, Figure 2)—this corrects the phase lag introduced in the TDA3030

LINE IDENT TIMING — (pin 3) This pin is used to control the timing of an internal timebase which, in its turn, controls the system during the 'back porch' of the transmitted signal. The pulse at the pin should end just before the active line time. The timing can be altered by changing the value of the 24k Ω resistor on the pin (see Figure 2).

SANDCASTLE INPUT — (pin 4) This input accepts a standard positive going 'sandcastle' pulse.

TRAP SWITCH — (pin 5) This output, which can be used to control the tracking filter (see Application Information and the circuit, Figure 2), is low impedance during lines with B-Y chroma and high impedance during R-Y lines.

FRAME PULSE INPUT — (pin 6) This pin accepts a positive going frame pulse of greater than 7V.

PAL/SECAM — (pin 7) This pin is low impedance when a SECAM signal is identified and is used to control the TDA3300.

U OUTPUT — (pin 8) This output is an emitter and is coupled to the U input of the TDA3300 via a capacitor

U, V and DIRECT INPUTS — (pins 9, 10 & 11) These are high impedance inputs which are coupled directly to the delay line outputs and the direct signal output.

V OUTPUT — (pin 12) This output is an emitter and is coupled to the TDA3300's V input via a capacitor.

NTSC HUE CONTROL — (pin 13) If this high impedance input is held between 0 and 5V it acts as the hue control when the commutator is in the NTSC mode. If it is taken to +12V it will switch the commutator to PAL or SECAM depending on the SECAM identification.

LUMA INPUT — (pin 14) The luma signal is fed to this high impedance input to the switched delay circuit. When a SECAM signal is identified the luma signal is delayed by

INPUT/OUTPUT FUNCTIONS (Continued)

200ns—to compensate for the delay of the SECAM discriminator. In PAL mode there is no delay.

LUMA OUTPUT — (pin 15) This is the output from the switched delay circuit.

IDENT INTEGRATION — (pin 16) The output of the ident phase detector is filtered at this point. A fairly long time constant is chosen for better noise immunity.

12V — (pin 17) This supplies the 12V for the circuit.

DE-EMPHASIS OUTPUT — (pin 18) The output of the de-emphasis network is fed to this pin.

CLAMP CAPACITOR — (pin 19) A capacitor on this pin stores the reference bias for the remodulator. A component of adequate quality should be used to avoid leakage problems during the 20ms storage time.

REMODULATED CHROMA OUTPUT — (pin 20) This is the output pin for the AM remodulated SECAM signal. A low voltage on this pin, about 2V, in the PAL mode allows simple signal path switching at the TDA3300's chroma input pin.

DE-EMPHASIS INPUT — (pin 21) This pin is the output from the discriminator from where it is fed to the de-emphasis network.

Δf_0 ADJUST — (pin 22) This pin is effectively the discriminator f_0 adjustment for the SECAM discriminator. The voltage applied to this pin provides fine tuning of f_0 in relation to 4.43MHz.

VARIABLE REACTANCE CIRCUITRY — (pins 23 & 24) These are part of the discriminator circuitry, with the quadrature tank circuit connected to pin 24.

9V INTERNAL REFERENCE — (pin 25) This is the output of an on-chip stabiliser. The DC bias for the discriminator tank and Δf_0 adjustment are derived from this circuit.

GROUND — (pin 26) This is the system ground and should have a low impedance path to the TDA3300's luma and chroma grounds.

SECAM CHROMA INPUTS — (pins 27 & 28) These are the chroma inputs to the system with pin 28 decoupled to ground, while pin 27 is fed with the composite video signal via the cloche filter.

APPLICATION INFORMATION

Tracking Filter

The application circuit illustrated in Figure 2 includes a tracking filter realised in discrete components. This circuit requires a low source impedance at the subcarrier frequency. This is supplied by an emitter follower biased by the TDA3030's 9V reference. A shunt tuned trap in series with the device's emitter has its centre frequency controlled by the discriminator and ident circuits so that the trap follows the modulation of the SECAM subcarrier. The frequency control is carried out by four transistors and the 56pF capacitor associated with L1, which together form a variable reactance circuit. If no SECAM signal is identified the trap frequency is about 5.5 to 6MHz.

Setting Up

Cloche Filter

Connect: An oscilloscope to pin 27.
Adjust: The cloche filter coil for a flat-topped chroma signal.

Discriminator Tuning

Connect: An oscilloscope to pin 18.
Observe: The frame blanking interval.
Adjust: The discriminator coil, on pin 24, to align the clamped lines at the beginning of the blanking period with subsequent lines.

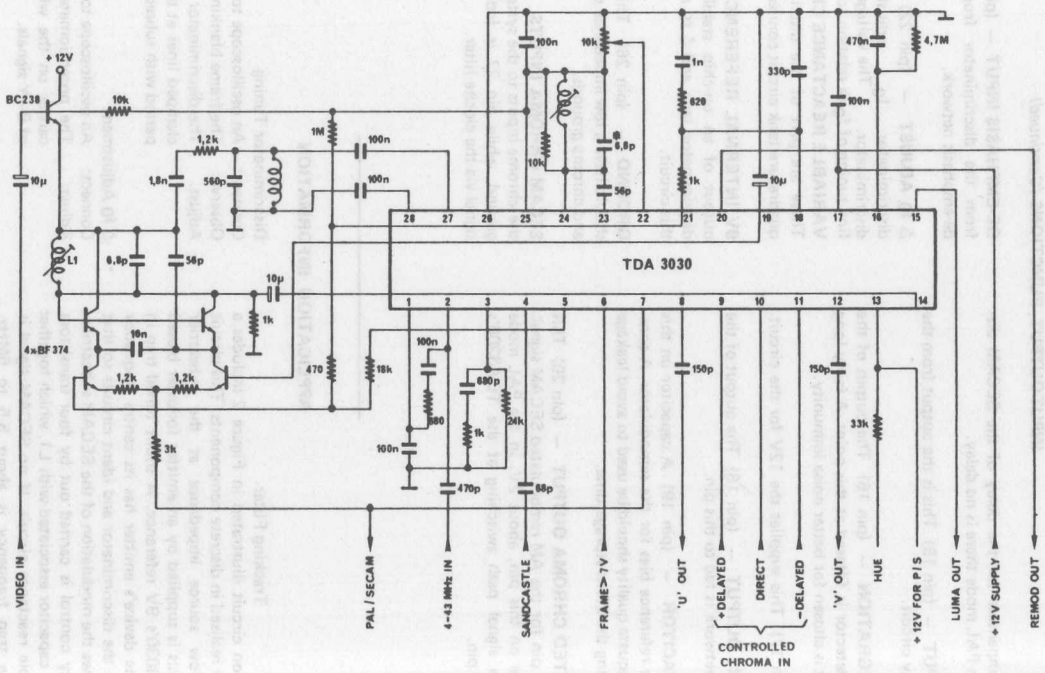
 Δf_0 Adjustment

Connect: An oscilloscope to pin 18.
Adjust: The potentiometer on pin 23 for zero subcarrier on the white and black bar portions of B-Y signals.

Tracking Filter

Connect: An oscilloscope to pin 15
Adjust: L1, see Figure 2, for minimum chroma content at pin 15.

FIGURE 2 — APPLICATION CIRCUIT



* Total capacitance, including socket, coil etc. should be no greater than 10pF

TDA3300B

TV COLOUR PROCESSING
SYSTEMMONOLITHIC SILICON
INTEGRATED CIRCUIT

ADVANCE INFORMATION

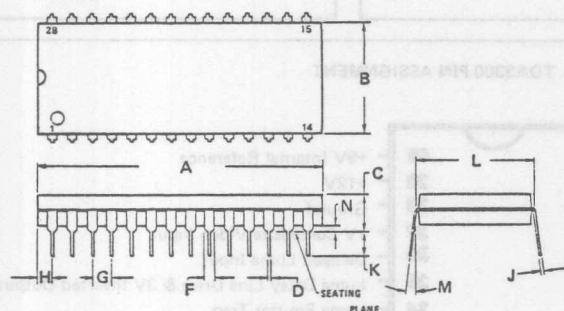
TV COLOUR PROCESSING SYSTEM

The TDA3030 is Motorola's first generation colour processing system. The device will accept a PAL or NTSC composite video signal and output the three colour signals—red, green and blue—driver signals to interface with the picture tube. There are also four inputs for On-Screen Display and the complementary bar blanking for use with related video TV games, camera etc.

MECHANICAL OUTLINES

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. 710-01 OBSOLETE, NEW STD 710-02.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

TDA 3300 B

ADVANCE INFORMATION

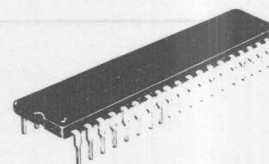
TV COLOUR PROCESSING SYSTEM

The TDA3300 is Motorola's third generation colour processing system. The device will accept a PAL or NTSC composite video signal and output the three colour signals—needing only a simple driver amplifier to interface with the picture tube. There are also four inputs for On-Screen Display and the complementary fast blanking for use with teletext, viewdata, TV games, cameras etc.

- Full multistandard capability
- On-Screen Display inputs + fast blanking
- Three DC, high impedance user controls
- Automatic Black Level set-up
- Beam Current Limiting
- Inexpensive 4.43/3.58MHz reference generation
- Single 12V supply
- Low dissipation—typically 600mW

TV COLOUR PROCESSING SYSTEM

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1 — TDA3300 PIN ASSIGNMENT

Chroma Input	1	40	+9V Internal Reference
ACC Capacitor	2	39	+12V
Chroma Delay Line Driver, emitter	3	38	Ground
Chroma Delay Line Driver, collector	4	37	1V Composite Video Input
Saturation Control	5	36	Delayed Luma Input
Ident Capacitor	6	35	Luma Delay Line Drive & 3V Inverted Output
V Input	7	34	Luma Emitter Trap
U Input	8	33	Luma Collector Trap
90° Loop Capacitor	9	32	Contrast Control
Oscillator Loop Filter	10	31	Black Level Clamp
Xtal Drive	11	30	Brightness Control
Xtal Feedback	12	29	Peak Beam Limiter Adjust
Ground	13	28	Frame Pulse Input
Blue Output	14	27	Sandcastle Pulse Input
Blue Output Clamp Capacitor	15	26	On-Screen Display Input Green
Blue Output Feedback	16	25	On-Screen Display Input Red
Green Output	17	24	On-Screen Display Input Blue
Green Output Clamp Capacitor	18	23	On-Screen Display Input Fast Blanking
Green Output Feedback	19	22	Red Output Feedback
Red Output	20	21	Red Output Clamp Capacitor

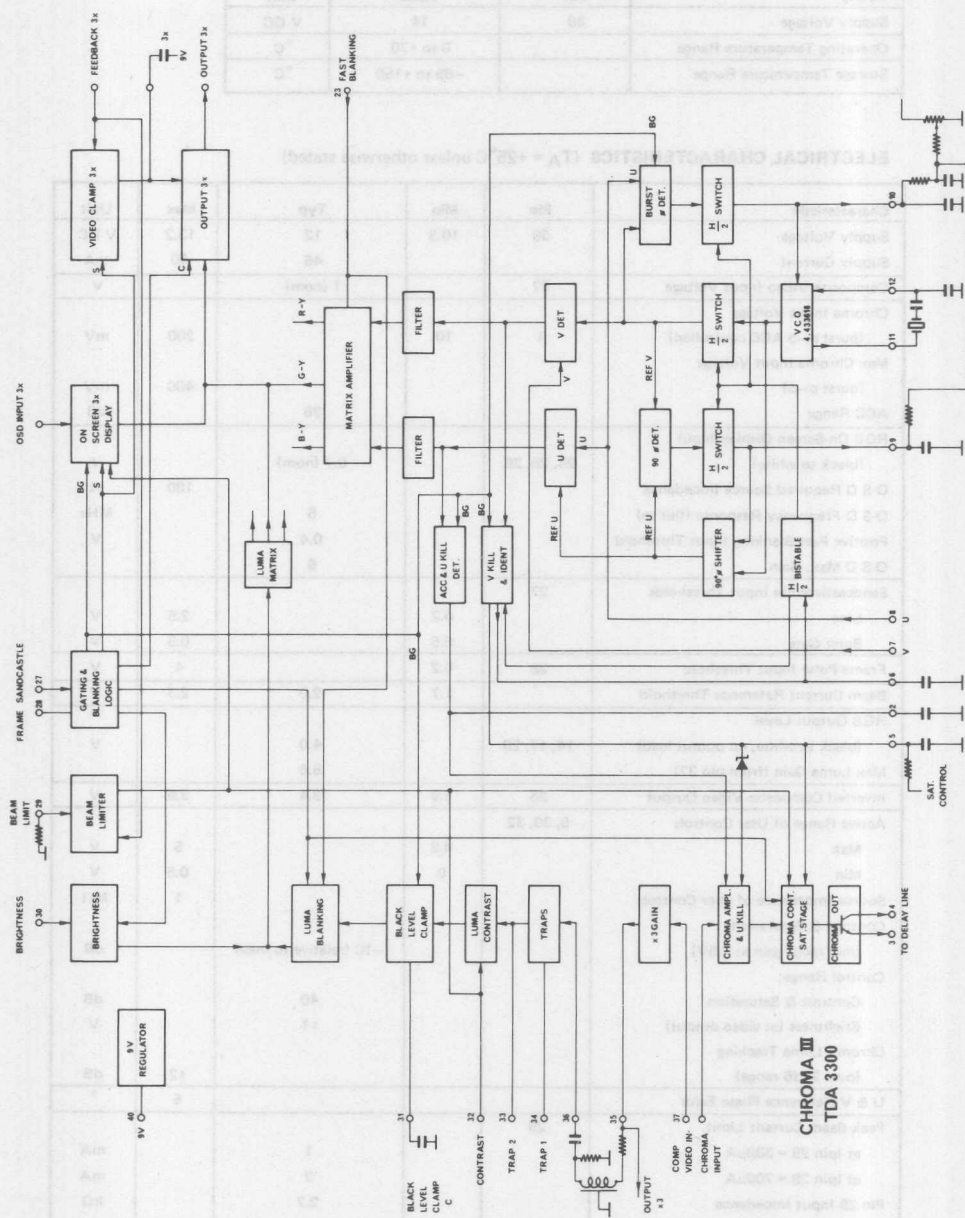
This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	39	14	V DC
Operating Temperature Range		0 to +70	$^\circ\text{C}$
Storage Temperature Range		-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise stated)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	39	10.8	12	13.2	V DC
Supply Current			45	60	mA
Composite Video Input Voltage	37		1 (nom)		V
Chroma Input Voltage (burst p-p ACC controlled)	1	10		200	mV
Max Chroma Input Voltage (burst p-p)				400	mV
ACC Range			26		dB
RGB On-Screen Display Input (black to white)	24, 25, 26		0.7 (nom)		V
O-S D Required Source Impedance				180	Ω
O-S D Frequency Response (flat to)			5		MHz
Positive Fast Blanking Input Threshold			0.4		V
O-S D Max. Gain			6		
Sandcastle Pulse Input Thresholds	27				
Line		0.2		2.5	V
Burst Gate		6.5		9.5	V
Frame Pulse Input Threshold	28	0.2		4	V
Beam Current Reference Threshold		1.7	2.0	2.3	V
RGB Output Level (black to white, no output load)	14, 17, 20		4.0		V
Max Luma Gain (from pin 37)			6.6		
Inverted Composite Video Output	35	2.9	3.4	3.9	V
Active Range of User Controls	5, 30, 32				
Max		4.2		5	V
Min		0		0.5	V
Source Impedance of User Controls				1	M Ω
Contrast & Saturation (mid range gain at 2.5V)			-10 (relative to max)		dB
Control Range:					
Contrast & Saturation			40		dB
Brightness (at video output)			± 1		V
Chroma/Luma Tracking (over 20dB range)				± 2	dB
U & V Reference Phase Error				5	$^\circ$
Peak Beam Current Limit	29				
at $I_{pin\ 29} = 330\mu\text{A}$			1		mA
at $I_{pin\ 29} = 700\mu\text{A}$			2		mA
Pin 29 Input Impedance			2.7		k Ω



CIRCUIT OPERATION

The circuit operation can be followed by referring to the block diagram, Figure 2.

THE LUMA CHANNEL

In order to ensure compatibility with standard video systems the luma channel input is high impedance, AC coupled and designed to accept a 1V composite video signal. After a X3 gain voltage amplifier the inverted luma signal is brought out to the luma delay line. The output is low impedance to facilitate matching the delay line and as the signal is inverted it is suitable for driving a sync separator.

Following the luma delay line the signal is fed to the chroma trap stage where external emitter and collector loads ensure accurate definition of the stage gain.

The contrast control is an electronic 'gain' control of the current sharing type with the black level clamp on the output. The action of the black level clamp has been designed for minimum interference on the video signal. This is achieved by comparing the output of the contrast control with an internal 5V reference. The signal from the comparator, which features a push-pull output for carrier or burst rejection, is then integrated by the external black level clamp capacitor.

The final interface between the luma channel and the luma matrix is the brightness control.

During the line and frame blanking periods a switching circuit effectively blanks the luma signal and inserts a nominal black level of an internally derived 5V reference level. However, the voltage source is modified by a current source; the latter based on the 'gain' control circuit described below—thus it becomes a controllable current source. This applies a variable offset between $\pm 1V$, to the nominal black level which is maintained during the frame blanking period, thus providing a brightness control.

The 'gain' control circuit for the three user controls is of the form shown in Figure 3.

This configuration gives a law which depends on the current ratios. The contrast and saturation controls have been designed to appear linear to the user, as can be seen from Figure 3.

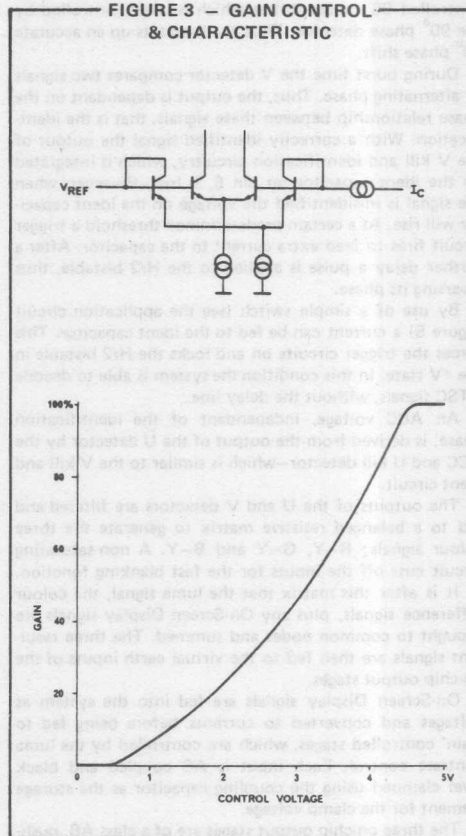
All the controls have an active range of 0.5 to 4.5V making them compatible with D/A converter derived control signals, such as those from remote control systems.

THE CHROMA CHANNEL

The chroma signal is fed via three gain controlled stages: automatic colour control (ACC), contrast (to track the luma signal) and saturation. The two latter controls are designed in the same way the luma contrast control, with the same law. One of these two stages is returned to full gain and the other to nominal (10dB down from max.) during the burst gate period to provide a standard burst level for the ACC.

The saturation control stage also provides the chroma kill function, which operates under two eventualities. Firstly the signal is removed in the event of prolonged misidentification or lack of identification. Secondly the saturation is reduced as the ACC voltage nears its zero level.

FIGURE 3 — GAIN CONTROL & CHARACTERISTIC



The chroma delay line drive is supplied by a transistor whose emitter and collector are brought out; the collector drives the delay line while the emitter supplies the direct signal for matrixing at the delay line output.

In the burst phase detector the system compares the constant phase burst of the U channel, at the delay line output, with the alternating reference drive to the V det-

CIRCUIT OPERATION (continued)

ector. A commutator converts the outputs to DC. At the same time any DC offsets are converted to alternating components, which are integrated to zero in the loop filter. Any resulting error voltage is applied to the 4.43MHz voltage controlled reference oscillator.

A similar arrangement, the 90° phase detector, compares the phase reference drive to the U detector with that of the reference drive to the V detector. The U detector drive comes from the reference oscillator via a voltage controlled 90° phase shifter which is itself controlled by the 90° phase detector. Thus the loop sets up an accurate 90° phase shift.

During burst time the V detector compares two signals of alternating phase. Thus, the output is dependant on the phase relationship between these signals, that is the identification. With a correctly identified signal the output of the V kill and identification circuitry, which is integrated by the ident capacitor on pin 6, is low. However, when the signal is misidentified the voltage on the ident capacitor will rise. At a certain predetermined threshold a trigger circuit fires to feed extra current to the capacitor. After a further delay a pulse is applied to the H/2 bistable, thus reversing its phase.

By use of a simple switch (see the application circuit Figure 5) a current can be fed to the ident capacitor. This forces the trigger circuits on and locks the H/2 bistable in the +V state. In this condition the system is able to decode NTSC signals, without the delay line.

An ACC voltage, independent of the identification phase, is derived from the output of the U detector by the ACC and U kill detector—which is similar to the V kill and ident circuit.

The outputs of the U and V detectors are filtered and fed to a balanced resistive matrix to generate the three colour signals; R-Y, G-Y and B-Y. A non-saturating circuit cuts off the inputs for the fast blanking function.

It is after this matrix that the luma signal, the colour difference signals, plus any On-Screen Display signals are brought to common nodes and summed. The three resultant signals are then fed to the virtual earth inputs of the on-chip output stages.

On-Screen Display signals are fed into the system as voltages and converted to currents before being fed to 'gain' controlled stages, which are controlled by the luma contrast control. Each input is AC coupled and black level clamped using the coupling capacitor as the storage element for the clamp voltage.

The three on-chip output stages are of a class AB, push-pull configuration with the gain defined by parallel feedback resistors.

Working with the output stages are two of the system's major features; beam current limiting and automatic black level set-up.

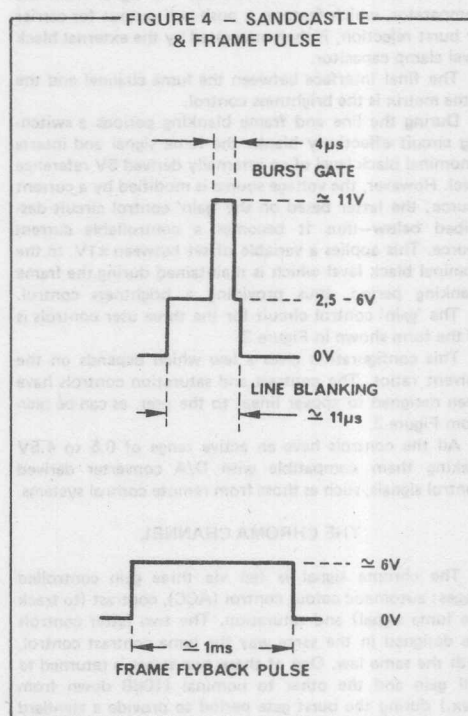
The beam current limiting is a peak detecting system designed to enhance the normal video or digital signal handling.

The beam current in each picture tube cathode is monitored by a high voltage PNP transistor (see the application circuit Figure 5). This is fed back to the TDA3300 where it is compared with an internal reference which is determined by the resistor on pin 29. The output of this comparison is fed to the contrast control.

The automatic black level set-up uses the same feedback input during the second complete line after the frame flyback.

At the same time an internal comparator compares an internal reference with the voltage developed across an external resistor by the picture tube beam current. The comparator's output controls the output stages to keep the beam current at the chosen level.

The internal line blanking and burst gate pulses are derived from a standard 'sandcastle' pulse, as shown in Figure 4, fed to pin 27. Frame blanking is derived from a frame flyback pulse applied to pin 28.





APPLICATION INFORMATION

Figure 5 is the external component diagram for the TDA3300 and shows resistor values which will result in nominal values, for peak beam limiting and beam current feedback of 2.6mA and 17 μ A per gun.

As for any picture tube the colour phosphors vary in efficiency, with blue generally being the most efficient, it is possible to scale the beam current feedback resistors (in Figure 5, 120k Ω in the collector of the BF493S) accordingly. The average needs for a typical tube to give Illuminant 'D' (6550°K) are as follows:

Red	\approx 120k Ω
Blue	\approx 150k Ω
Green	\approx 120k Ω

SETTING UP PROCEDURES

The Reference Oscillator PLL

Input Signal: PAL colour test signal with anti-PAL signal

Adjust: The PLL potentiometer, on pin 10, for minimum colour on the TV screen

Delay Line Balance

Setting up the PAL delay line follows the conventional procedure where the gain is adjusted by the delay line balance potentiometer and the phase by the input or output coils to the delay line. However, it should be noted that the adjustment of the phase can be effected by either the input or output tuning coil. And, as the line is in the ACC loop the tuning of either of these coils will not affect the signal amplitude.

The Chroma Trap

Input Signal: A PAL colour test signal
Connect: An oscilloscope to an output channel—preferably green
Adjust: The chroma trap for minimum 4.43MHz on the output waveform

Output Gain

There are two methods of adjusting the output gain: visually and by the use of a colorimeter.

Visually

Input Signal: Grey scale
Set: (a) Brightness for visual extinction of black.
(b) Contrast towards maximum
Adjust: Gain controls for the best apparent uniformity of the grey scale

Using a colorimeter

Input Signal: White field
Set: Contrast towards maximum
the exact setting is a matter of choice
Brightness to mid-scale or 3.1V
Adjust: Gain controls for a nominal colour point—normally Illuminant 'D'

ON-SCREEN DISPLAY

In a receiver not designed to be equipped with the On-Screen Display facility, it is recommended that the On-Screen Display and fast blanking inputs are grounded.

PRECAUTION

In those receivers using high frequency power supplies for the picture tube heaters it is recommended that the heaters be decoupled to prevent interference with the feedback from the PNP sampling transistor.

TOA3350A

CHROMINANCE
COMBINATION
MONOLITHIC SILICON
INTEGRATED CIRCUIT



Advance Information

CHROMINANCE COMBINATION

The TOA3350A is an integrated circuit designed to be used in PAL color decoding circuitry in color television receivers.

- Internal supply line regulation
- 10 to 12 MHz oscillator adjustment necessary
- 10 to 12 VDC Automatic Color Control range
- Accurate Bandwidth Pulse must gating input

OUTLINE DIMENSIONS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

P SUFFIX
PLASTIC PACKAGE
CASE 711-02

NOTES

1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

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TDA3950A

Advance Information

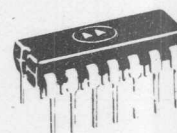
CHROMINANCE COMBINATION

The TDA3950A is an integrated circuit designed to be used in PAL colour decoding circuitry in colour television receivers.

- Internal supply line stabilisation
- No 4.43 MHz oscillator adjustment necessary
- 20 dB ACC (Automatic Colour Control) range
- Accepts Sandcastle pulse burst gating input

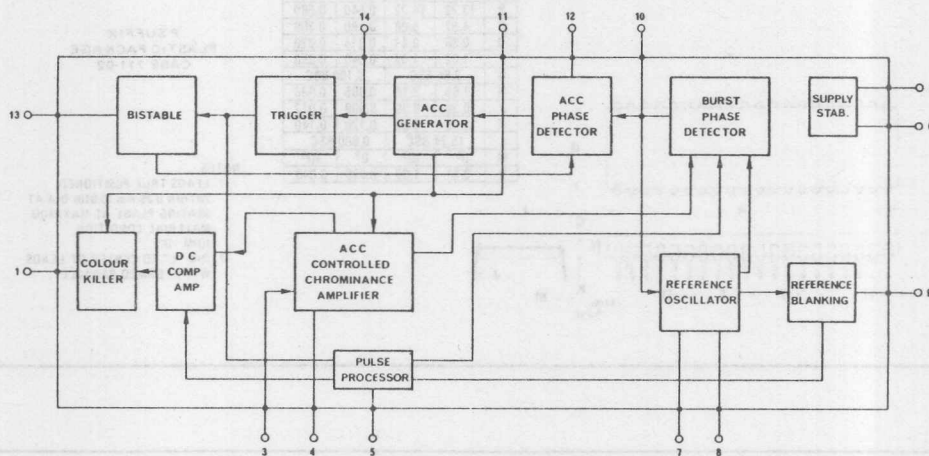
CHROMINANCE COMBINATION

MONOLITHIC SILICON
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646 TO-116

FIGURE 1 -- SYSTEM BLOCK DIAGRAM



Pin Connections

1	Chroma Output	8	Crystal connection	12	ACC Phase-Detector coupling
2	V _{CC}	9	Subcarrier reference output	13	PAL half line (H/2) output
3	Chroma Input	10	VCO Phse Detector output	14	Identification trigger capacitor
4	ACC Decoupling	11	ACC Detector filter		
5	Sandcastle Pulse Input				
6	Ground				
7	Crystal connection				

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MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise stated)

Rating	Pin	Value	Unit
Power Supply Current	2	80	mA
D.C. Current Capability of Reference Output	9	20	mA
Operating Temperature Range		0 to +70	$^\circ\text{C}$
Power Dissipation (Package Limitation)		1.25	W
Derate above $T_A = +25^\circ\text{C}$		10	mW/ $^\circ\text{C}$
Storage Temperature Range		65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise stated — Chroma input 250 mV p-p, 100% colour bars)

Characteristics	Pin	Min	Typ	Max	Unit
Supply Voltage	2	8.5	8.7	9.7	V _{dc}
Chrominance Output Voltage (RL pin 1 = 560 Ω)	1	250	400	500	mV p-p
Colour Killer Operation:					
Kill Level (Burst)	3	8.0	12	17	mV p-p
Unkill Level (Burst)		11	15	20	
Hysteresis			2.0		dB
Maximum Chrominance Input Voltage	3	250			mV p-p
Chrominance Output D.C. Current:					
Colour Killer Operating	1		0		mA
Colour Killer Off			1.0		
Change in Chrominance Output due to +6 dB, -12 dB change in Chrominance Input.	3, 1		2		dB
Chrominance Input Impedance	3		5.0		K Ω
Reference Output	9		2.2		V p-p
Reference Oscillator Pull-In Range		± 400	± 600		Hz
Phase Accuracy			2.3		$^\circ/100\text{ Hz}$
Reference Oscillator Temperature Drift (no burst pulse applied)	9		-2.0		Hz/ $^\circ\text{C}$
Burst Gate Operating Voltage	5	9.0		12	V
Burst Gate Input Impedance	5		7.0		K Ω
H/2 Bistable Output	13		8.0		V p-p
Identification Time			1.0		msec

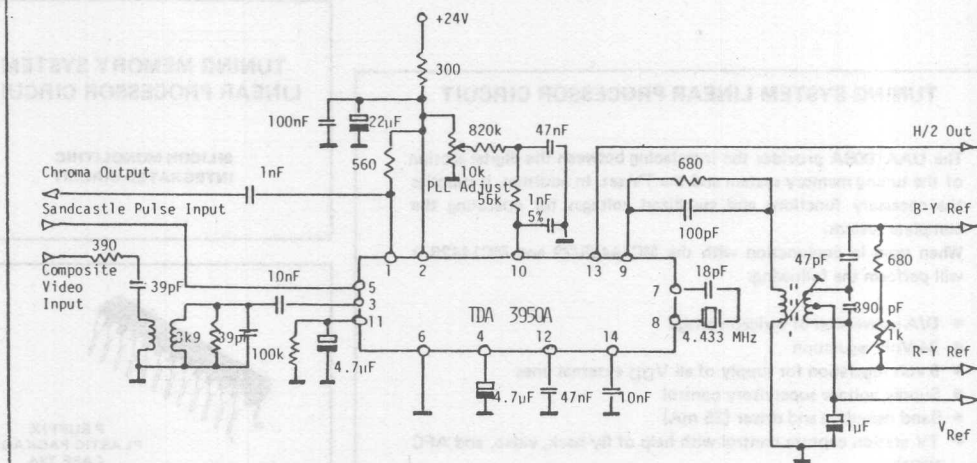
APPLICATION NOTES

1. Normal decoupling precautions must be taken. For example pin 2 must be decoupled closely to pin 6 (ground) thus preventing sub-carrier components leaking into sensitive areas of the circuit.
2. To prevent the radiation of sub-carrier harmonics, the connection from pin 9 (reference output) and pin 8 (crystal feedback) must be kept as short as possible.

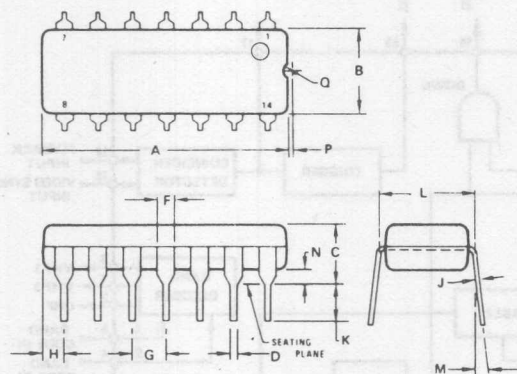
SETTING UP NOTES

Disconnect the burst gate pulses and adjust the P.L.L. potentiometer to give "Zero beat" from the sub-carrier reference oscillator. Reconnect the burst gate pulses.

FIGURE 3 - TYPICAL CIRCUIT CONFIGURATION



OUTLINE DIMENSIONS



NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	10°		10°	
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

CASE 646

PLASTIC PACKAGE

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UAA1008A-DP

TUNING MEMORY SYSTEM LINEAR PROCESSOR CIRCUIT

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 724

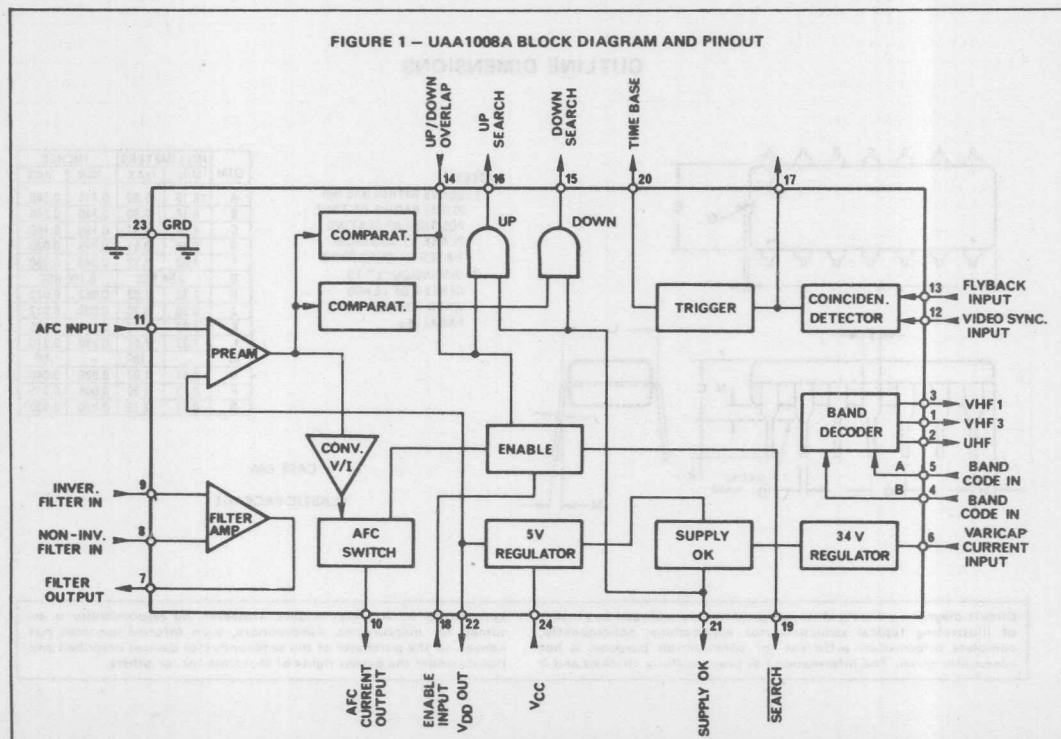
TUNING SYSTEM LINEAR PROCESSOR CIRCUIT

The UAA1008A provides the interfacing between the digital section of the tuning memory system and the TV set. In addition, it supplies the necessary functions and stabilized voltages for operating the complete system.

When used in conjunction with the MC14425/29 and MC14426 it will perform the following:

- D/A conversion of varicap voltage
- 34 Volt regulation
- 5 volt regulation for supply of all V_{DD} external lines
- Supply voltage supervisory control
- Band decoding and driver (35 mA)
- TV station capture control with help of fly-back, video, and AFC signals.

FIGURE 1 - UAA1008A BLOCK DIAGRAM AND PINOUT



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	Vdc
Varicap Supply Current	I_{VV}	10	mA
Continuous Band Switch Output Current ¹	I_b	35	mA
Filter/Amplifier Output Current	I_{fout}	+0.4 to -1	mA
Band Switch Output Voltage	V_b	V_{CC} to -2	Vdc
Output Current (pins 15, 16, 19, 20, 21)	I_o	1	mA
Pin 19 Output Voltage	V_o	18	Vdc
Pin 22 Output Current	I_{DD}	15	mA
Operating Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

¹ Upon request devices allowing a Max. Capacitive Load of 22 μF on band switch outputs can be supplied.

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C)

Characteristic	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Operating Voltage	24	V_{CC}		12		18	Vdc
Power Supply Current (@ $V_{CC} = 18\text{ V}$)	24	I_{CC}	Band driver current = 0			21	mA _{dc}
Varicap Voltage Supply	6	V_{VV}	$I_{VV} = 2\text{ mA}$	33.5		40.5	Vdc
Stabilized Voltage Output	22	V_{DD}	$I_{DD} = 10\text{ mA max.}$	4.95	5.2	5.45	Vdc
Input Signals:							
— Negative video modulation positive sync. pulses	(12)	V_{vid}	See typ. application		2		V P/P
— Positive flyback signal	(13)	V_{fly}	See typ. application		60		V P/P
— Video carrier discriminator negative going for Δf positive (Referenced to V_{DD})	11	V_{afc}			± 250		mV
Time Base Output Voltage	20	V_{OH}	$I_{OH} = 20\text{ }\mu\text{A}$ $I_{OL} = 500\text{ }\mu\text{A}$	4		1	V
Supply OK	21	V_{OH} V_{OL}	$I_{OH} = 500\text{ }\mu\text{A}$ $I_{OL} = 10\text{ }\mu\text{A}$	4		1	V
UP / DOWN Output Voltage	15, 16	V_{OH} V_{OL}	$I_{OH} = 20\text{ }\mu\text{A}$ $I_{OL} = 500\text{ }\mu\text{A}$	4		1	V
AFC Signal Processor							
— $G_m (I_{I0} / V_{I1})$	10	I_{afc}		0.9	1.2	1.37	mmhos
— Maximum AFC current	10			± 123	± 200	± 305	μA
— Comparator threshold			See Fig. 2		± 50		mV

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C) Contd.

Characteristics	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
Varicap Filter & Amplifier:							
– Input bias current	8, 9					0.7	μA
– Offset voltage	8, 9			–20		+20	mVdc
– Output voltage swing	7	V _{OL} V _{OH}		31		0.5	V
– Open loop voltage gain					60		dB
Band Switch Output:							
– Output current	1, 2, 3	I _{OH}	V _{OH} = V _{CC} – 1.6 V			35	mA
– Leakage current (open collector)	1, 2, 3	I _{OL}	V _{OL} = –2 V			1	μA
Binary Coded Band Input Voltage	4, 5	V _{IH} V _{IL}	I _{IH} = 300 μA I _{IL} = 300 μA	V _{DD} – 0.55		0.55	V
Enable Input Voltage	18	V _{IH} V _{IL} tristate	I _{IH} = 300 μA I _{IL} = 300 μA	V _{DD} – 0.55 2		0.55 3.15	V
Search Output	19	V _{OH} V _{OL}	Open collector I _{IL} = 500 μA			0.5	V

TUNING MEMORY SYSTEM ENABLE FUNCTIONAL TABLE

MODE	ENABLE IN	LINEAR AFC	MEMORY UPDATE	TIME BASE	UP/DOWN OVERLAP	SEARCH
Memory	L	ON	YES	X	NO	H
Memory	Tristate	OFF	NO	X	NO	H
Search	H	OFF	YES	X	YES	L
Verification	L	ON	YES	X	NO	L

X : don't care

FIGURE 2 – AFC TRANSFER FUNCTION

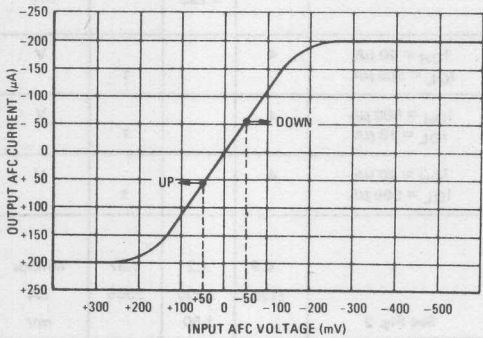
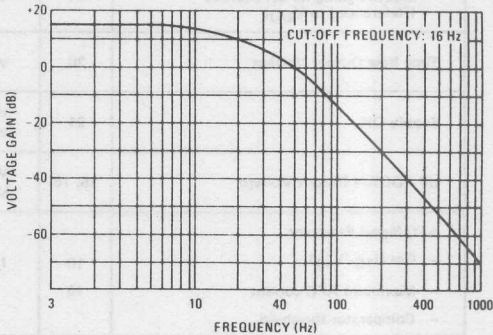


FIGURE 3 – FILTER/AMP FREQUENCY RESPONSE



INPUT/OUTPUT FUNCTIONS

AFC INPUT & OUTPUT — The AFC input (pin 11) generates UP & DOWN commands whenever the input level varies by more than $V_{DD} \pm 50$ mV.

At the same time the AFC voltage is converted into a proportional AFC output current (pin 10) limited to an excursion of $\pm 200 \mu A$ (see Fig. 2). The AFC output current source is gated by the Enable input function (pin 18). See enable functional table.

UP & DOWN — The UP output (pin 16) changes to high whenever the AFC input (pin 11) is higher than $V_{DD} + 50$ mV, the DOWN output (pin 15) when lower than $V_{DD} - 50$ mV.

For pin 11 voltage included between $V_{DD} - 50$ mV and $V_{DD} + 50$ mV no UP or DOWN commands will be generated. By means of an RC time constant on pin 14 it is possible to delay the falling edge of the UP command to make it overlap with the DOWN command provided that ENABLE IN (pin 18) is high.

Should it be necessary to defeat the UP and/or DOWN commands, the correspondent pin 16 and 15 can be grounded.

FILTER & AMPLIFIER — (Inverting input: pin 9; non-inverting input: pin 8; output: pin 7.) This operational amplifier provides the integration of the MC14425/9 binary rate multiplier output and the amplification of the same (usually around 6.5 times) to cover the required varicap tuning voltage range, according to the typical configuration of Fig 4.

Under these conditions only the critical components R_1 and R_2 are used to determine the voltage gain of the integrator. It is recommended to use good stability resistors with tracking temperature coefficient. (See Fig. 3 and 4.)

BAND DRIVER — Fully decoded outputs for tuner band switching are provided at outputs VHF 1 (pin 3), VHF III (pin 1), UHF (pin 2) according to the following logic table. See also MC14425/9 data sheet.

Input Code		Decoded Output		
Pin 4	Pin 5	Pin 3	Pin 1	Pin 2
0	0	X	X	H
1	0	X	H	X
0	1	H	X	X
1	1	X	X	X

NOTES:

¹ X state correspond to an open PNP collector.

² The control circuit supplying the coded band information can be looped-back to skip the following codes: (11) for three band only and (11) (10) for two band only.

FLYBACK — (pin 13.) This input is driven by the positive line flyback signal commonly available in TV sets. In conjunction with the SYNC signal controls TIME BASE output.

It is recommended to differentiate the flyback pulse to insure that coincidence between sync pulses and flyback occurs only when the picture is actually synchronised (see Fig. 4).

SYNC — (pin 12.) This input is driven by the video signal (negative modulation/positive going sync) through the sync separator network of Fig. 4.

Should separate positive sync pulses be available they can be used to drive pin 12 directly.

TIME BASE — (pin 20.) This output goes to high whenever coincidence is detected between flyback and sync signals, it is an indication of the presence of a valid TV signal.

It is possible to activate time base output also in absence of the above signals by grounding pin 17 via a 10K resistor. Presence of Time Base is checked at the end of the verification time in the control circuit MC14425/9 to definitely activate the AFC output at pin 10.

SUPPLY OK — (pin 21.) Purpose of this function is to protect the memory contents in case of failure or discontinuity of any supply voltage.

Should the 34 V varicap supply fail or the power supply V_{CC} fall below 10 V, SUPPLY OK output, normally at V_{DD} (5.2 V) will immediately drop to zero volts.

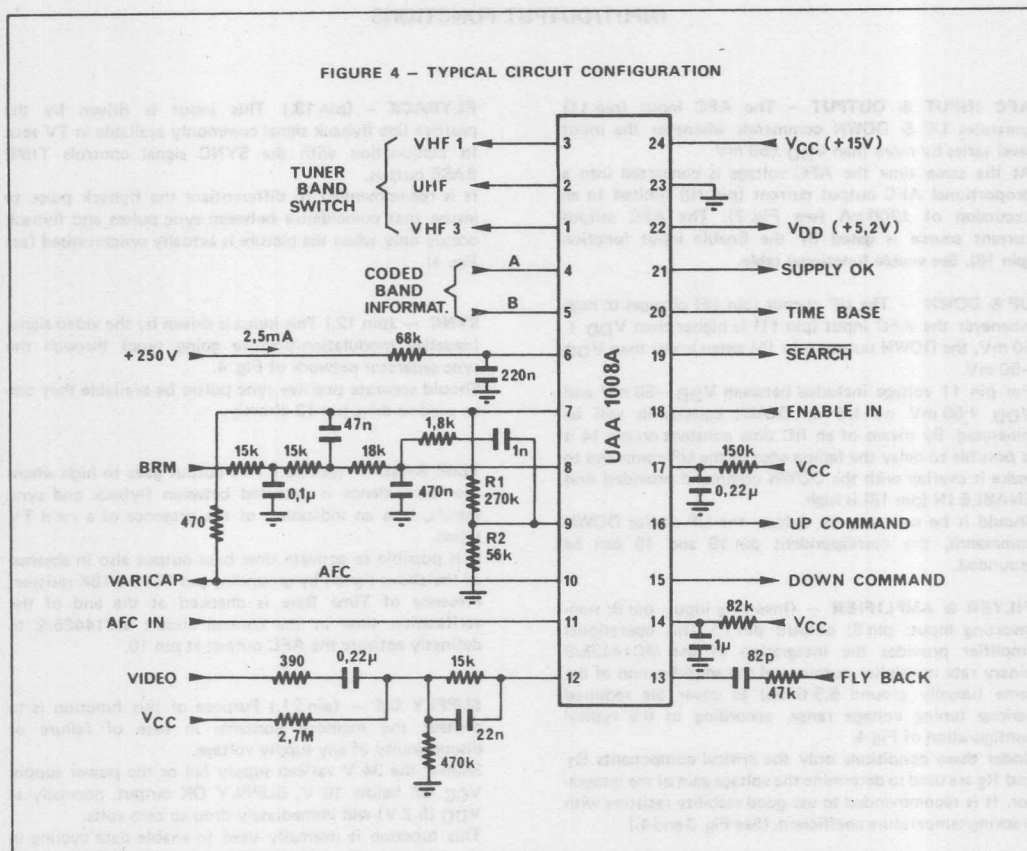
This function is normally used to enable data cycling in the memory circuit MC14426 and the UP/DOWN counter in the control circuit MC14425/9.

ENABLE IN — (pin 18.) This function is provided by the control circuit MC14425/9 and is primarily used to turn off and on the AFC output in conjunction with TIME BASE, as shown in the enable functional table.

Enable-in goes high whenever a ramp is started and returns to low as soon as an UP/DOWN overlap is detected. It also insures that following an UP/DOWN overlap the UP delay is removed.

SEARCH — (pin 19) this output goes to low whenever the system is in the search mode and can be used to control external functions as necessary.

FIGURE 4 - TYPICAL CIRCUIT CONFIGURATION



ENABLE IN - Pin 18. This function is provided in the control circuit MCM-100 and is primarily used to turn off the AFC output in conjunction with TIME BASE at shutdown in the single functional mode. Enable in goes high whenever a card is started and returns to low as soon as an UP/DOWN command is detected. It also returns low following an UP/DOWN command. The UP/DOWN is returned.

SEARCH - Pin 19. This output goes to low whenever the system is in the search mode and can be used as control external functions as necessary.

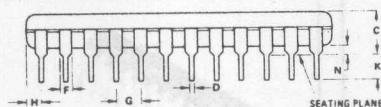
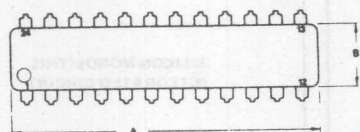
Pin	Pin	Pin	Pin	Pin
Pin 1	Pin 2	Pin 3	Pin 4	Pin 5
1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20

NOTES

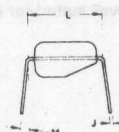
1. This schematic is for the UAA1008A-DP only. The UAA1008A-DP is a dual in-line package (DIP) and is not a surface mount device (SMD). The UAA1008A-DP is a dual in-line package (DIP) and is not a surface mount device (SMD). The UAA1008A-DP is a dual in-line package (DIP) and is not a surface mount device (SMD).

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 724



NOTE:
1. LEADS, TRUE POSITIONED WITHIN
0.25 mm (0.010) DIA AT SEATING
PLANE AT MAXIMUM MATERIAL
CONDITION (DIM. "D").



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.13	1.269	1.269
B	6.10	6.80	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.35	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040

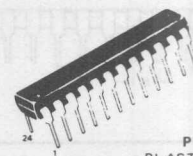
Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

UAA 2000A

PHASE LOCKED LOOP SYNTHESISER & DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



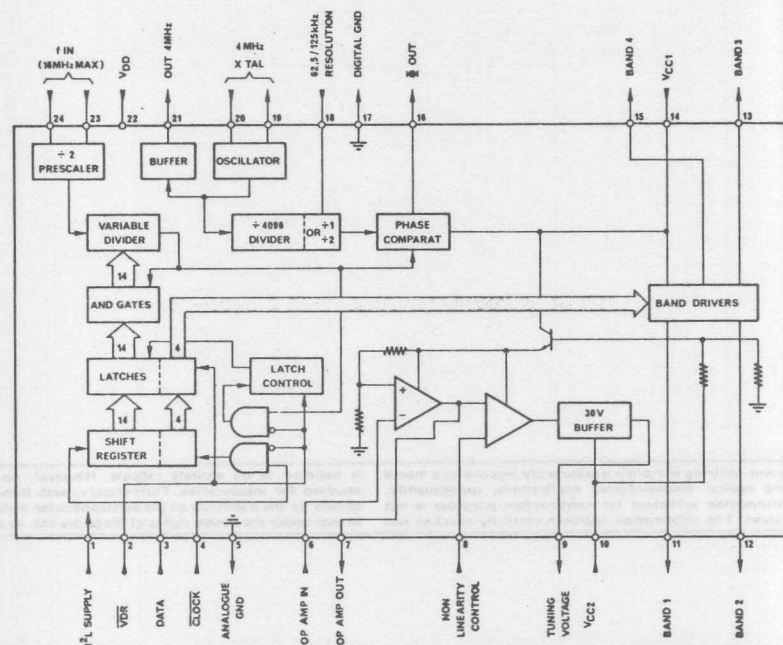
P SUFFIX
PLASTIC PACKAGE
CASE 724

PHASE LOCKED LOOP SYNTHESISER & DRIVER

The UAA2000 is designed to control the phase locked loops in frequency synthesisers as used in TV applications. Realised in I²L/EFL bipolar technology it contains all the necessary digital and linear functions. It uses an input data format which makes it well suited for use with microprocessor control.

- 14-bit variable divider & 4-bit band select
- PLL with phase and frequency comparator
- Filter and tuning voltage amplifier
- 16 MHz max input frequency
- Pin option for 125 kHz or 62.5 kHz resolution
- 4 band driver outputs

Figure 1 — UAA2000 Block Diagram and Pinout



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$) All voltages are referenced to ground (pins 5 & 17, when connected externally)

Rating	Pin	Symbol	Value	Unit
I ² L Supply Current	1	I _S	200	mA
Logic input Voltages	2, 3, 4	V _{LOG}	15	V
Filter Amplifier				
Input Voltage Range	6		0 to 15	V
Output Short Circuit				
Duration (protected from 0 to 10 V)	7	t _s	continuous	
Nonlinearity Control Voltage	8	V _{NL}	0 to 15	V
Tuning Voltage Output	9			
Short Circuit Duration		t _{st}	continuous	
(protected from 0 to V _{CC2})				
Analogue Supply Voltage	10	V _{CC2}	35	V
Band Buffers				
Output Current at any Buffer ¹	11, 12	I _{BBF}	30	mA
Short Duration (1 ms) Peak	13, 15			
Current (Current has been		I _{BBP}	300	mA
limited externally) ²				
Max capacitance which can				
be switched without				
External Current Limit			5	μF
Minimum Voltage in OFF				
State V _{CC1} = 12 to 15 V		V _N	-5	V
Supply Voltage	14	V _{CC1}	20	V
Phase Buffer Output Current	16	I _{PM}	10	mA
(has to be externally limited)				
F _{ref} Selection	18			
Input Voltage		V _{RI}	0.9	V
Input Current		I _{RI}	10	mA
Crystal Oscillator				
Output Current (has to be	19	I _{OC}	5	mA
externally limited)				
Input Voltage	20	V _{CI}	V _{DD} + 0.5	V
Buffer Output Current (has				
to be externally limited)	21	I _{OB}	20	mA
Logic Supply Voltage	22	V _{DD}	10	V
Input Common Mode Voltage	23, 24	V _{ICM}	2.5	V
Input Differential Voltage	23, 24	V _{IO}	± 2.5	V
Storage Temperature		T _{STG}	-55 to +150	°C
Operating Ambient Temperature		T _A	0 to 70	°C
Functional Temperature Range			0 to 85	°C
(No parameters guaranteed)				

NOTES

¹ All Buffers ON

² Only One Buffer Switching

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Voltage ($I_S = 60\text{ mA}$)	1	V_S	0.5	0.83	1	V
I ² L Supply Current ($f_{in} = 16\text{ MHz}$)	1	I_S	40	60	80	mA
Logic Input Levels: VDR, Data, Clock	2, 3, 4	V_{LOG}	-0.3		1	V
Low State			3.5		10	V
Logic Input Currents		I_{LOG}			-100	μA
Low State					10	μA
High State						
Filter Amplifier						
Input Current	6	I_{FI}		1	20	nA
Output Current	7					
Sourcing		I_{FOS}			3	mA
Sinking		I_{FOQ}			400	μA
Non Linear Amplifier						
Input Current	8	I_{NI}			-150	μA
Tuning Voltage ($V_{CC2} = 30 - 33\text{ V}$, Highest Level $I_{TS} = 50\text{ }\mu\text{A}$)	9	V_{TH}	28			V
Lowest Level		V_{TL}	200		500	mV
Output Current						
Sourcing		I_{TS}			2	mA
Sinking		I_{TQ}	200		350	μA
Peak Noise						mV
Analogue Supply Voltage	10	V_{CC2}	30		33	V
Analogue Supply Current ($V_{CC2} = 30 \dots 33\text{ V}$ $I_{TS} = 0$)		I_{CC2}	0.6	1.3	3	mA
Band Buffers	11, 12					
Output Voltages — ON (at 20 mA) (at 40 mA)	13, 15	V_{BBO}	$V_{CC1}-1.3\text{V}$ $V_{CC1}-1.5\text{V}$	$V_{CC1}-1\text{V}$	$V_{CC1}-0.8\text{V}$	
Leakage Currents — OFF (at -5 V)		I_{BBL}			10	μA
Supply Voltage	14	V_{CC1}	11.4		12.6	V
Supply Current ($I_S = 0$, $I_{TS} = 0$, $V_{CC1} = 12 \dots 15\text{ V}$, $V_{CC2} = 30 - 33\text{ V}$, $I_{FOQ} = 0$, pin 16 = open)		I_{CC1}	1.3		10	mA
Phase Comparator (Tri-state Output)	16					
Output Voltage						
Low at 2 mA		V_{PL}			0.5	V
High at 2 mA		V_{PH}	$V_{CC1}-1.2\text{V}$			
Leakage Current (High Impedance)		I_{LP}			20	nA

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C) Contd.

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
F_{ref} Selection, Input Voltage Low Level ($F_{ref} = 488\text{ Hz}$) High Level ($F_{ref} = 977\text{ Hz}$)	18	V_{RL} V_{RH}		floating	0.3	V
Crystal Oscillator Input Voltage (also 4 MHz input without crystal) Output Voltage — Buffer Low Level (30pF/470 Ω load) High Level (30pF/470 Ω load)	20 21	V_{CI} V_{COL} V_{COH}	200 0 3.0		1000 0.5 4.0	mV p-p V V
Logic Supply Voltage Logic Supply Current ($V_{DD} = 4.75 - 5.25\text{ V}$, $I_{OB} = 0$)	22	V_{DD} I_{DD}	4.75 20	5.0 28	5.25 56	V mA
Input Voltage Swing (each input) (Coupling capacitance $\geq 1\text{ nF}$, slewing $\geq 5\text{ V}/\mu\text{s}$) Input Frequency	23, 24	V_{IN} F_{IN}	0.1		1 16	V p-p MHz
Thermal Resistance — chip to ambient					60	$^\circ\text{C}/\text{W}$
Power Dissipation: $V_{CC1} = 12\text{ V}$, $V_{DD} = 5\text{ V}$, band buffers OFF, $I_{OB} = 0$, $V_{CC2} = 31.5\text{ V}$, $I_s = 60\text{ mA}$				290	530	mW

All voltages are referenced to ground (pins 5 & 17 when connected externally)

SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C) see figure 6

Characteristic	Symbol	Min	Max	Unit
Clock Frequency	f_{ck}	0	100	kHz
Clock Low Time	t_{CL}	3		μs
Neg. going VDR edge to 1st Clock edge	t_{LVC}	20		μs
Last Clock edge to Pos going VDR edge	t_{LCV}	1		μs
Data change to Pos going Clock edge	t_{LOC}	1		μs
Pos going Clock edge to Data change	t_{LCD}	1		μs
Rise times of digital inputs: VDR, CLOCK, Data	t_{RC} t_{RV} t_{RD}		2	μs
Fall times of digital inputs: VDR, CLOCK, Data	t_{FC} t_{FV} t_{FD}		2	μs

CIRCUIT OPERATION

The circuit operation can be followed by reference to figure 1, the UAA2000 block diagram, and figure 2, a phase locked loop using the UAA2000, a microprocessor and a TV tuner.

The tuner's local oscillator output is divided, in an external prescaler, by 64 and then fed to the $\div 2$ prescaler inputs of the UAA2000. This feed may be either via both inputs or single ended using pin 23 or pin 24. The output from this is, in turn, fed to the variable divider where it is further divided by a number determined by the microprocessor. The variable divider output frequency, consisting of narrow pulses, called preset pulses, see the timing diagram figure 5, is compared with a reference frequency. The result of this comparison is used as the control voltage for the local oscillator varicap.

The UAA2000 also receives band switching information from the microprocessor and applies it to the tuner. To ensure loop stability the filter response is flat around the frequency where the overall loop gain is unity, see figure 3.

The digital circuitry of the UAA2000 is realised in 1^2L and EFL integrated logic.

The data controlling the division ratio of the variable divider and the band buffers is moved serially into a shift register by means of the three logical inputs, $\overline{\text{VDR}}$, Data and CLOCK, see figures 1, 2 and 7. The $\overline{\text{VDR}}$ input enables the circuit when the data and clock inputs are operated from busses.

Data are transferred from the shift register into latches which, by means of logic, are isolated from the shift register during a shift operation.

The variable divider is, essentially, a presettable synchronous counter. Once all stages are at a logical 0 a preset pulse is generated, this opens the AND gates and presets the variable divider to the number stored in the latches.

The reference frequency, f_{ref} , is generated on-chip by binary division of a 4MHz crystal oscillator signal, alternatively it can be applied externally to pin 20. A buffer stage permits external circuitry to be driven by the 4MHz source.

To provide operation at two different frequency resolutions the system's division ratio of the reference frequency divider can be changed by the use of pin 18; 125 or 62.5kHz steps. With the pin grounded the 62.5

kHz resolution results. The division ratios resulting are 4096 and 8192.

The phase comparator is phase and frequency sensitive with a buffered tristate output. The states of the outputs are defined in the following page, Input/Output Functions.

Figure 5 shows the timing diagram for the situation when the TV channel is changed. With the negative going $\overline{\text{VDR}}$ edge, t_1 , the latches are disconnected and the clock input to the shift register is released, allowing access to new data. Since the $\overline{\text{VDR}}$ signal and the preset pulses occur asynchronously, the variable divider latches have to be reconnected on the negative edge of the preset pulse, t_4 .

Thus at t_3 the variable divider is preset to the old division ratio. The new division ratio is loaded with the second preset pulse after the positive going $\overline{\text{VDR}}$ edge, t_5 . Band information, which is signalled to the UAA2000 by the MPU changes at t_6 . This allows a periodic refresh of the division ratio when the TV channel is unchanged.

The filter amplifier is an operational amplifier, designed for a very low input bias current, with the positive input internally biased. The standard filter set up is shown in figures 2 and 8 with the frequency response shown in figure 3. However, the filter may be set up around the op amp only (see figure 9) to allow use of the non-linear amplifier which compensates for the characteristics of the tuner's varicaps. The degree of compensation can be controlled from pin 8, between two extremes, see figure 4. If pin 8 is connected to pin 7 the transfer function is linear, if however pin 8 is grounded the function takes on its extreme non-linear form. Intermediate shapes can be achieved by controlling pin 8 with a potentiometer.

The 30V output buffer supplies the varicap tuning voltage. The analogue outputs, pins 7 and 9, are short circuit protected. To minimise interference the ground and supply lines of the digital and analogue sections of the system are brought out on separate pins.

To guarantee optimum operation, the analogue supply voltage, between pins 10 and 5, has to be sufficiently free of ripple in the range of about 5Hz to 1kHz, since any interference on this line is transferred to the varicap output, pin 9, at approximately the same amplitude.

INPUT/OUTPUT FUNCTIONS

I²L SUPPLY — (pin 1) This is the current supply for the I²L injectors. The characteristic of the pin is that of a forward biased diode to pin 17.

\overline{VDR} — (pin 2) This pin is the chip select and is active when low, = 0.

DATA — (pin 3) Data is entered into the device, serially via this pin, and passed directly into the shift register. In its turn this controls the variable divider and the band buffers.

CLOCK — (pin 4) This pin delivers the clock signal to the shift register, which accepts data on the positive going edge. It should be noted that within the \overline{VDR} window, when \overline{VDR} = low, the clock has to be high at the beginning and the end of the clock pulse train.

OP. AMP IN — (pin 6) This pin is the inverting input to the operational amplifier. The non-inverting input is internally biased.

OP. AMP OUT — (pin 7) This pin is the output of the operational amplifier and the input to the non-linear amplifier.

NON-LINEARITY CONTROL — (pin 8) This pin controls the input of the non-linear amplifier. It gives a linear transfer characteristic between pins 7 and 9 when pin 8 is connected to pin 7 and non-linear performance when pin 8 is grounded.

TUNING VOLTAGE — (pin 9) This is the tuning voltage output ready for direct control of the varicap diode.

VCC2 — (pin 10) This is the supply voltage for the linear section of the circuit. The external supply must have a current limit lower than 20mA when shorted to ground.

BAND DRIVER OUTPUTS — (pins 11, 12, 13 & 15) These outputs, which get their information from the data line, are able to drive the tuner directly and can deliver up to 40mA.

VCC1 — (pin 14) This pin supplies the voltage for the band buffers.

PHASE COMPARATOR OUTPUT — (pin 16) This is a tristate output. The output is in the tristate condition, i.e. high impedance, when the divided input frequency is in phase with the on-chip reference. When the divided input frequency phase leads that of the on-chip reference the output is a series of 'high' going pulses — the high state — with reference to the tristate condition. When the divided input frequency phase lags that of the on-chip reference the output is a series of 'low' going pulses — the low state — again with reference to the tristate condition.

62.5/125kHz RESOLUTION — (pin 18) This pin serves to change the division ratio of the reference divider. It is an I²L gate input, which means that its characteristic is that of a diode to ground. The resolution is 62.5kHz if the pin is grounded.

4MHz XTAL OUT — (pin 19) This is a low impedance output which drives the crystal of the 4MHz oscillator in the series resonance mode.

4MHz XTAL IN — (pin 20) The oscillator input with an input impedance of 20k Ω .

f IN — (pins 23 & 24) These are the inputs for the frequency to be divided by the variable divider. Both inputs may be driven in antiphase or only one input, with the unused input decoupled via a 1nF capacitor to ground. If driven in the single ended mode the minimum voltage is 200mV peak to peak.

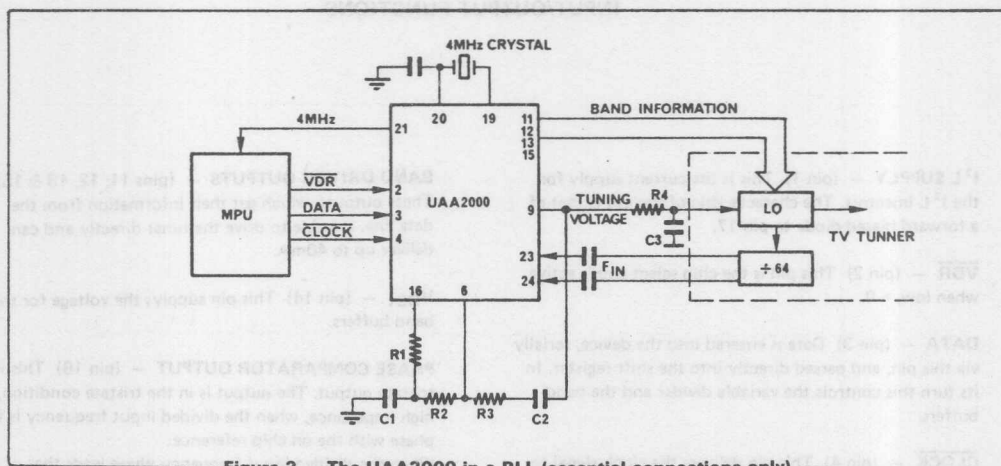


Figure 2 — The UAA2000 in a PLL (essential connections only)

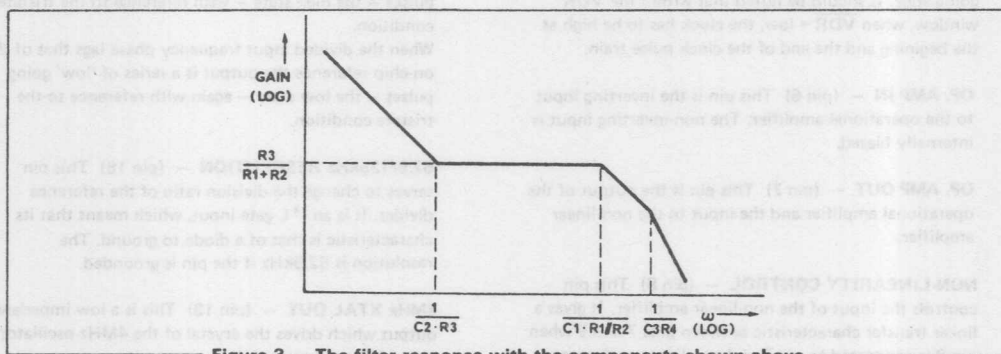


Figure 3 — The filter response with the components shown above

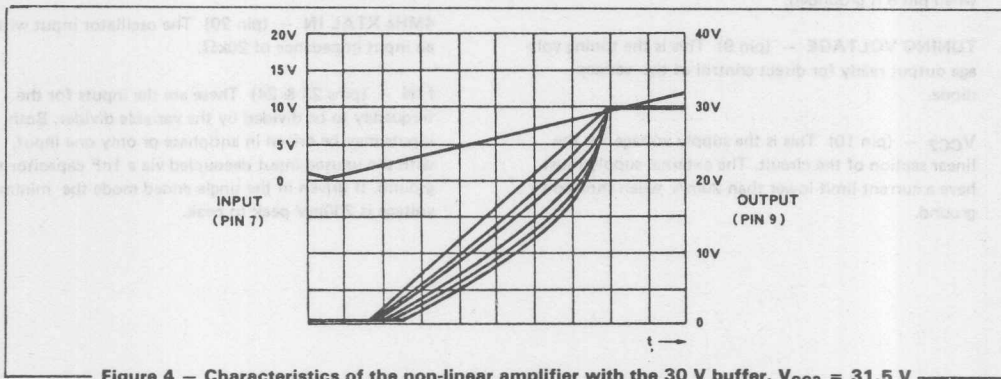


Figure 4 — Characteristics of the non-linear amplifier with the 30 V buffer. $V_{cc2} = 31.5 \text{ V}$

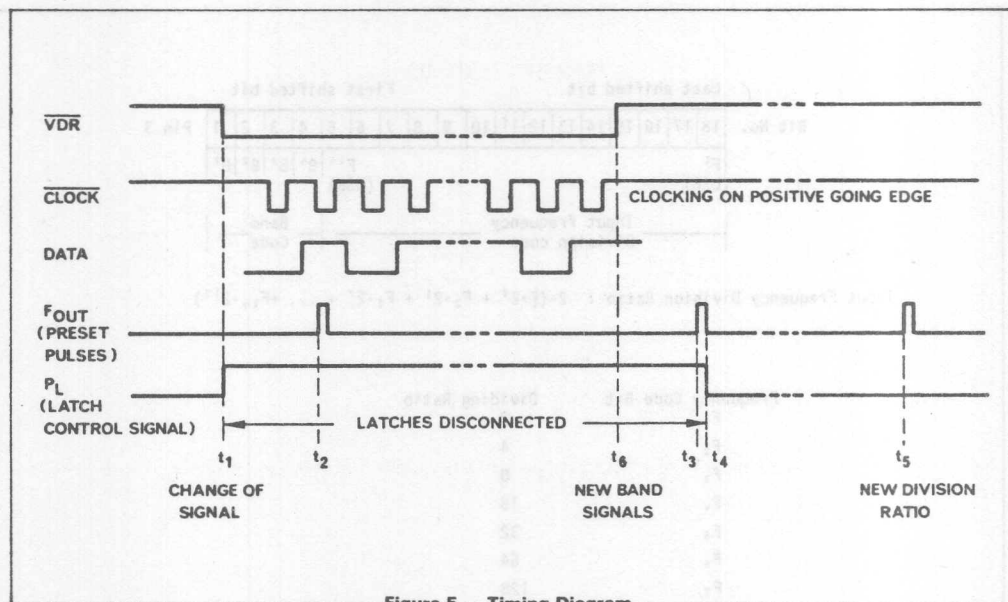


Figure 5 - Timing Diagram

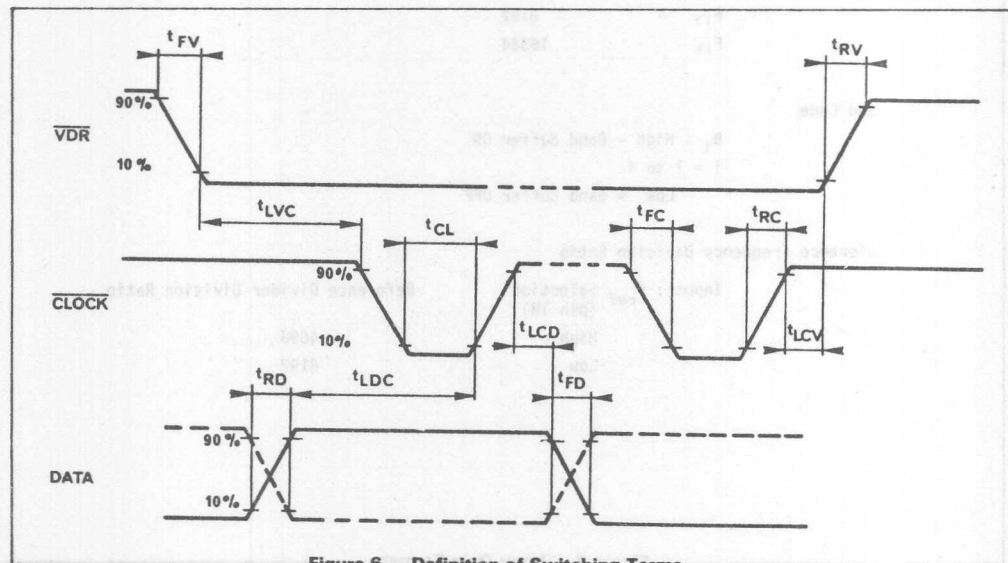


Figure 6 - Definition of Switching Terms

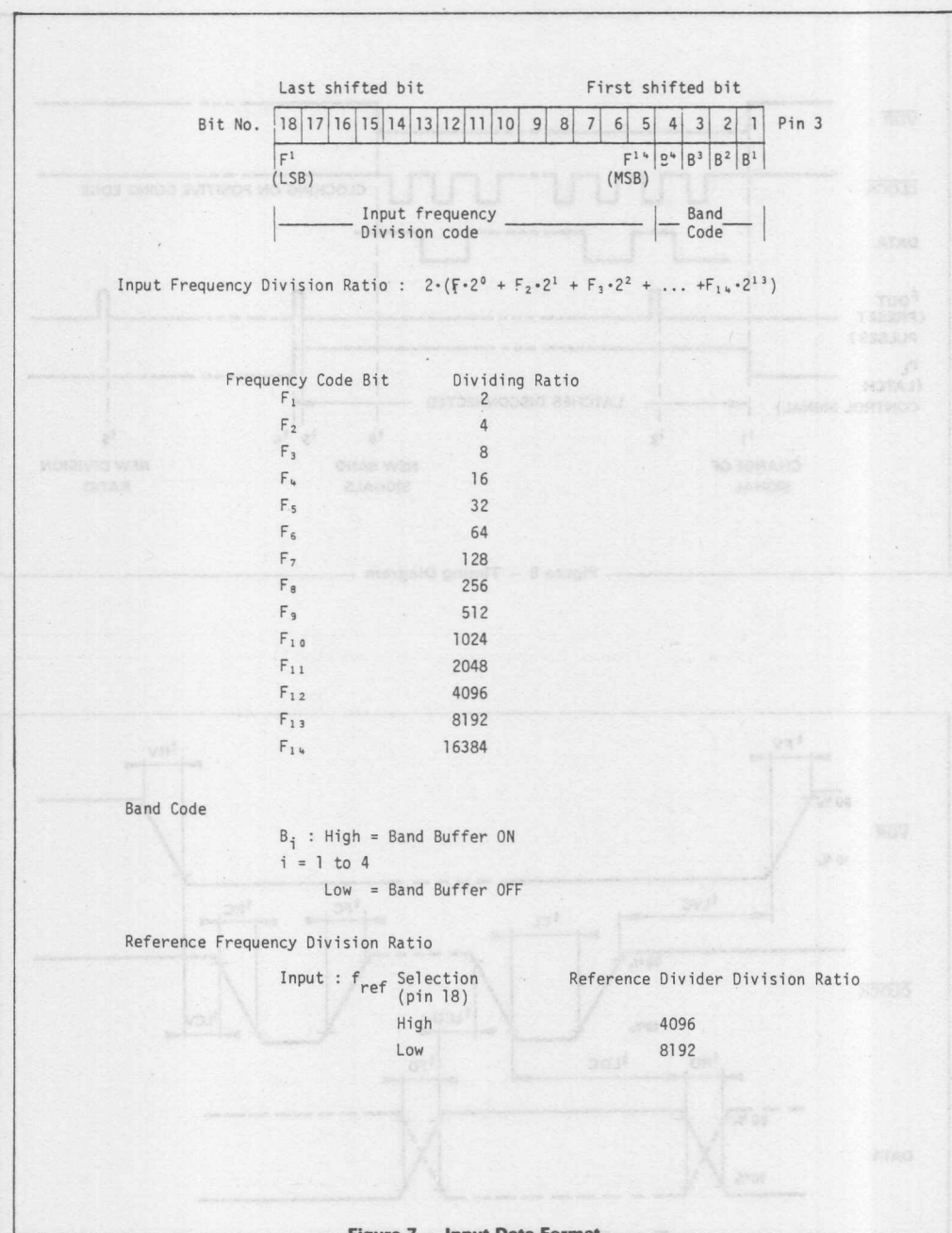


Figure 8 — External Components

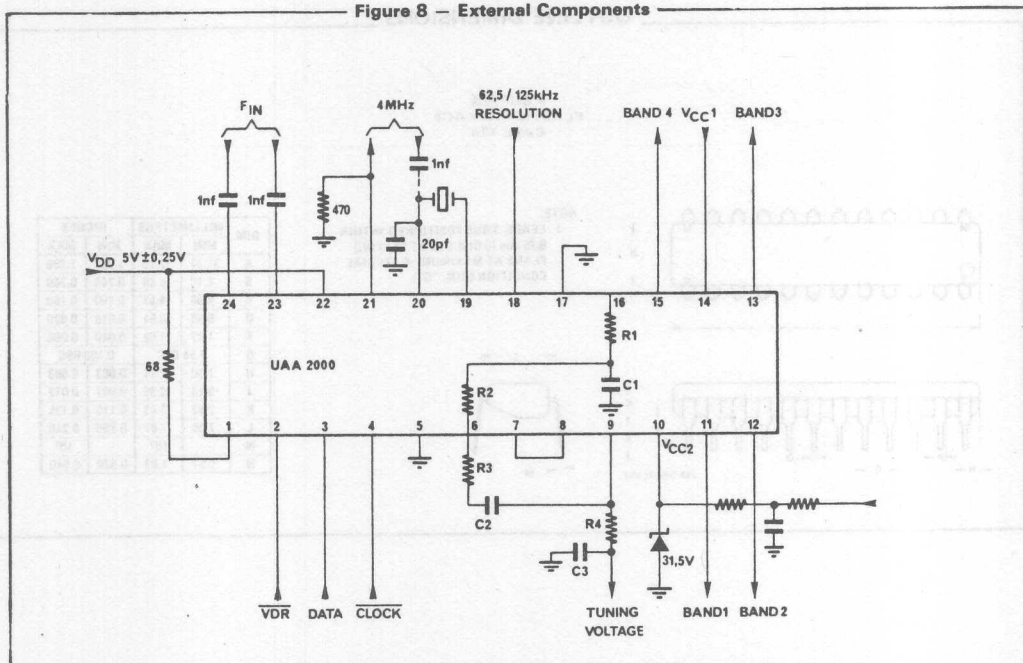
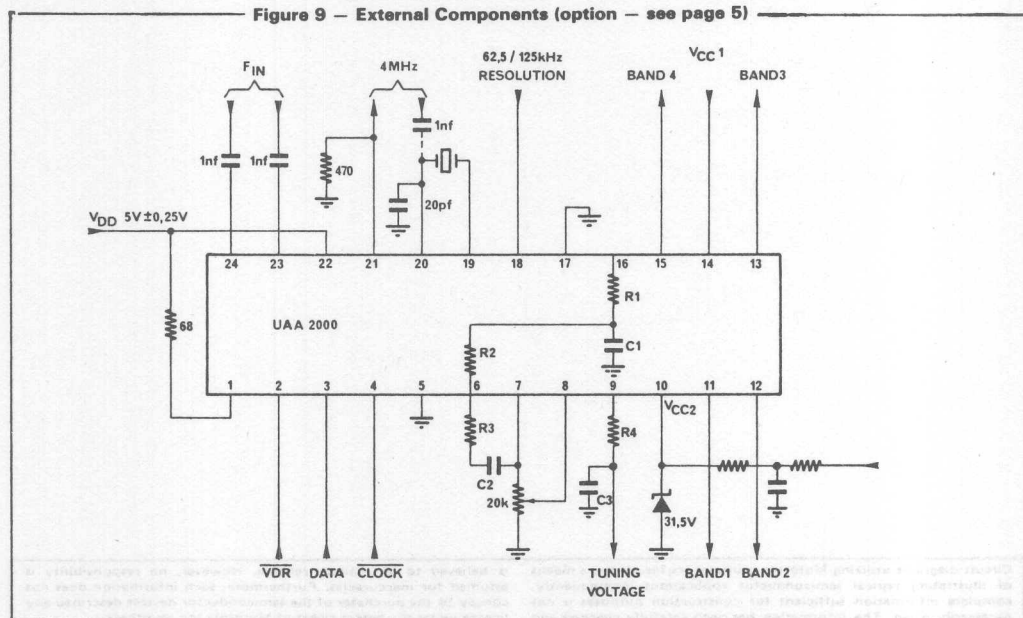
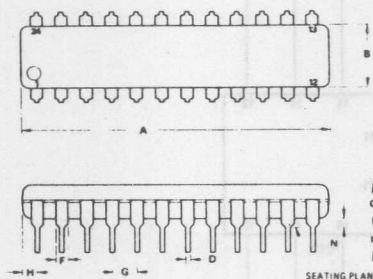


Figure 9 — External Components (option — see page 5)



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NOTE:
1. LEADS, TRUE POSITIONED WITHIN
0.25 mm (0.010) DIA AT SEATING
PLANE AT MAXIMUM MATERIAL
CONDITION (DIM. "D").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.13	1.260	1.286
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.35	7.87	0.290	0.310
M	10°		10°	
N	0.51	1.02	0.020	0.040

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications, consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

UAA 2001

Advance Information

SYNTHESIZER AMPLIFIER & DRIVER

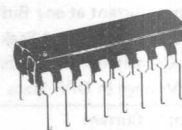
The UAA 2001 is designed for use in frequency synthesizers where it sets up the phase locked loop. It is particularly suitable for use with the MC6805T2 microprocessor (MPU) in a TV synthesizer where it forms the interface between the tuner and the MPU. The circuit is realised in bipolar I² L technology.

- Direct tuner drive from 4 band drivers
- 60mA band driver capability
- Direct control of the tuner's varicap diode

SYNTHESIZER

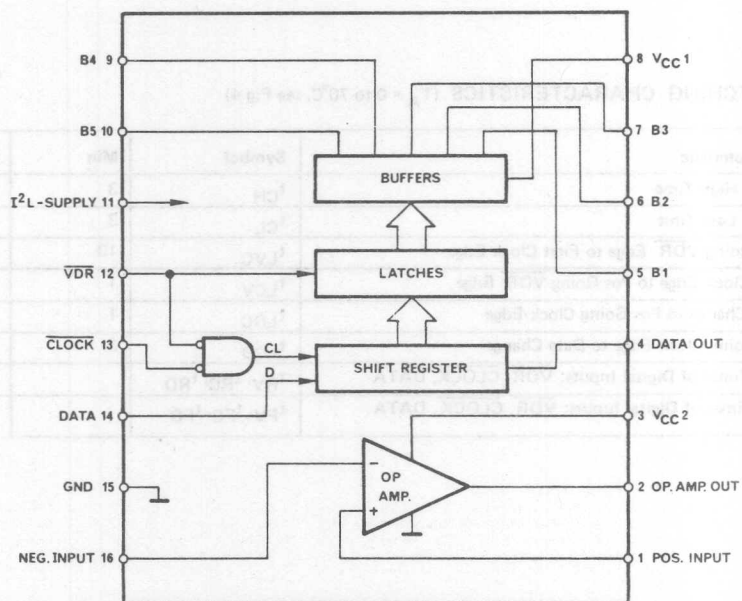
AMPLIFIER & DRIVER

MONOLITHIC SILICON
INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

FIGURE 1 - BLOCK DIAGRAM



UAA2001

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Pin	Symbol	Value	Unit
Logic Input Voltages	12,13,14	V_{LOG}	15	V
Operational Amplifier: Input Voltage Range Short Circuit Duration (protected from 0 to V_{CC2})	16,1 2	t_s	0 to 15 continuous	V
Analogue Supply Voltage	3	V_{CC2}	35	V
Buffer Supply Voltage	8	V_{CC1}	18	V
Data Out, max Voltage ($I_D = 1\text{mA}$)	4		10	V
Buffer B1 Output Voltage at Logical '0' Output Current at Logical '1' (needs external current limit)	5		20 7	V mA
Buffers B2, B3, B4 & B5 Output Current at any Buffer (all buffers on) Short Duration (1ms) Peak Current (needs external limit) Max Capacitance switchable without external current limit Min Voltage in OFF State	6,7, 9,10	I_{BBF} I_{BBP}	70 300 5 $V_{\text{CC1}} - 20\text{V}$	mA mA μF
$I^2\text{L}$ Supply Current	11	I_S	30	mA
Storage Temperature		T_{STG}	-50 to +150	$^\circ\text{C}$
Operating Ambient Temperature		T_A	0 to 70	$^\circ\text{C}$

All Voltages Referenced to Ground — pin 15

SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C , see Fig 4)

Characteristic	Symbol	Min	Max	Unit
Clock High Time	t_{CH}	3		μs
Clock Low Time	t_{CL}	3		μs
Neg Going $\overline{\text{VDR}}$ Edge to First Clock Edge	t_{LVC}	10		μs
Last Clock Edge to Pos Going $\overline{\text{VDR}}$ Edge	t_{LCV}	1		μs
Data Change to Pos Going Clock Edge	t_{LDC}	1		μs
Pos Going Clock Edge to Data Change	t_{LCD}	3		μs
Rise Times of Digital Inputs: $\overline{\text{VDR}}$, CLOCK, DATA	t_{RV} , t_{RC} , t_{RD}		2	μs
Fall Times of Digital Inputs: $\overline{\text{VDR}}$, CLOCK, DATA	t_{FV} , t_{FC} , t_{FD}		2	μs

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC1} = 15\text{V} \pm 5\%$, $V_{CC2} = 30\text{ to }33\text{V}$) unless otherwise noted.

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Logic Input Levels, $\overline{\text{VDR}}$, $\overline{\text{CLOCK}}$, DATA	12, 13	V_{LOG}				
Low State	14		0		0.8	V
High State			2		6	V
Logic Input Currents		I_{LOG}				μA
Low State					-100	μA
High State					10	μA
Operational Amplifier						
Input Current	16, 1	I_{FI}		1	20	nA
Input Voltage		V_{CM}	2.2		12	V
Output Voltage ($V_{CC2} = 30\text{ to }33\text{V}$, $I = 50\mu\text{A}$)	2					V
Highest Level		V_{TH}	28	$V_{CC2}-2$	V_{CC2}	V
Lowest Level		V_{TL}	100		500	mV
Output Current Limitation						
Sourcing		I_{TS}		1.5	2	mA
Sinking		I_{TQ}	200	1	500	mA
Peak Noise						mV
Analogue Supply Voltage	3	V_{CC2}	30		33	V
Analogue Supply Current ($V_{\text{OUT}} = V_{\text{TL}}$) ($V_{CC2} = 30\text{ to }33\text{V}$ ($V_{\text{OUT}} = V_{\text{TH}}$))		I_{CC2}	0.5	2 1.5	4	mA
Supply Voltage	8	V_{CC1}	10		15	V
Supply Current ⁽²⁾ ($I_{\text{LOG}} = 0$)		I_{CC1}	0.5		3	mA
Data Out (open collector)						
Output Saturation Voltage ⁽¹⁾ at 1mA	4	V_{DO}			0.8	V _A
Leakage Currents for Logic '0' ($V_{\text{OUT}} = 6\text{V}$)		I_{DL}			1	μA
Buffer B1						
Output Saturation Voltage ⁽¹⁾ at 2.5mA	5	V_{BO}			0.8	V
Leakage Current for Logic '0' at 15V		I_{BL}			5	μA
Buffers B2, B3, B4, B5	6, 7, 9, 10	V_{BBO}	$V_{CC1}-1.3$ $V_{CC1}-1.5$	$V_{CC1}-1$ $V_{CC1}-1.1$	$V_{CC1}-0.7$ $V_{CC1}-0.8$	V V mA μA
Output Voltages - ON, at 40mA at 60mA						
Sum of all Buffer Currents (B2 to B5) ⁽¹⁾					80	mA
Leakage Currents - OFF at $V_{CC1}-20\text{V}$					10	μA
$I^2\text{L}$ Supply Current	11	I_{S}	4	7	10	mA
$I^2\text{L}$ -Supply Voltage ($I_{\text{S}} = 7\text{mA}$)	11	V_{S}	0.7	1.2	1.7	V
Power Dissipation ($I_{\text{S}} = 7\text{mA}$, $V_{CC1} = 12\text{V}$, $V_{CC2} = 31.5\text{V}$)		P_{D}		90 ⁽²⁾ 150 ⁽³⁾		mW
Thermal Resistance, Chip to Ambient					80	$^\circ\text{C/W}$

All voltages are referred to Ground (pin 15)

- NOTES : 1) Current has to be limited externally
2) Band Buffers B₂ to B₅ OFF
3) One Band Buffer ON at 40mA

CIRCUIT DESCRIPTION

The circuit operation can be followed by reference to fig 1, the UAA 2001 block diagram, and fig 2, a phase locked loop using the UAA 2001, the MC6805T2 MPU and a TV tuner.

The tuner's local oscillator output frequency is divided in an external prescaler by 64 and then fed to the MC6805T2, which includes a variable divider, controlled by the processor, a reference divider and a phase comparator. By means of this circuitry the local oscillator frequency is further divided by a number determining the TV channel and compared to a fixed reference frequency inside the MPU. The output voltage of the phase comparator is filtered by using the operational amplifier of the UAA 2001 and then serves as the control voltage for the local oscillator varicap.

To facilitate filtering of the reference frequency the op amp is designed for a very low input bias current (1nA typ). The standard filter set up is shown in fig 2 with the frequency response shown in fig 3. To ensure loop stability the response is flat around the frequency where the overall loop gain is unity.

The UAA 2001 also receives band switching information from the MPU and applies it to the tuner by means of a shift register, latches, and buffers. The 5-bit band switching information is transferred by the signals DATA,

CLOCK and VDR (chip select); these inputs are designed to accept TTL levels. The CLOCK and DATA lines can be shared with other systems having other I/O devices.

Fig 4 shows the circuit's timing diagram. On the negative going VDR edge the latches are disconnected from the shift register and new information is shifted in. On the

positive going VDR edge the latches are reconnected thus transferring new band information to the buffers and the tuner.

The shift register also has a data output, this allows the MPU to pass data through the UAA 2001 and drive further circuits from the same DATA and chip select pins. The UAA 2001 shifts and outputs data on the positive going clock edge where the following circuits are intended to shift data on the negative going edge. For reliable data transfer the UAA 2001 should always be the first circuit in line as the clock signal consists of negative going pulses.

The latches control five buffers. Buffer B1 has an open collector output (see fig 5) and may be used to output any information from the MPU. Buffers B2 to B5 are band buffers specially designed to drive the tuner. Their drive capability is 60mA.

INPUT/OUTPUT FUNCTIONS

POS. INPUT — (pin 1) This is the non-inverting input to the operational amplifier and needs an external reference bias.

OP. AMP. OUT — (pin 2) This is the tuning voltage output, designed for direct control of the tuner's varicap.

V_{CC2} — (pin 3) This is the op amp supply voltage.

DATA OUT — (pin 4) This pin is the data output of the shift register. The output is designed to allow cascading other circuits using the same VDR signal.

B1 — (pin 5) This pin is an open collector buffer output of the first shifted bit. When shifting a logic '1' the output transistor is ON.

BAND DRIVER OUTPUTS — (pins 6, 7, 9, 10) These outputs can directly drive the tuner and deliver up to 60mA. When shifting a logic '1' the appropriate band buffer is ON.

V_{CC1} — (pin 8) This is the supply voltage for the band buffers.

I² L SUPPLY — (pin 11) This pin needs an external resistance to set up the I² L injector currents. The characteristic of the pin is that of a forward biased diode to pin 15 (ground) plus a series resistance of about 60Ω.

VDR — (pin 12) This is the chip select and is active when low.

CLOCK — (pin 13) This pin delivers the clock signal to the shift register, which accepts shifts and outputs data on the positive going edge. It should be noted that within the VDR window, when VDR is low, the clock has to be high at the beginning and end of the clock pulse train.

DATA — (pin 14) Data is entered serially into the circuit via this pin and passed directly to the shift register. In turn this controls the latches and band buffers.

NEG. INPUT — (pin 16) This is the inverting input of the op amp with a typical input bias current of 1nA, reducing with increasing temperature.

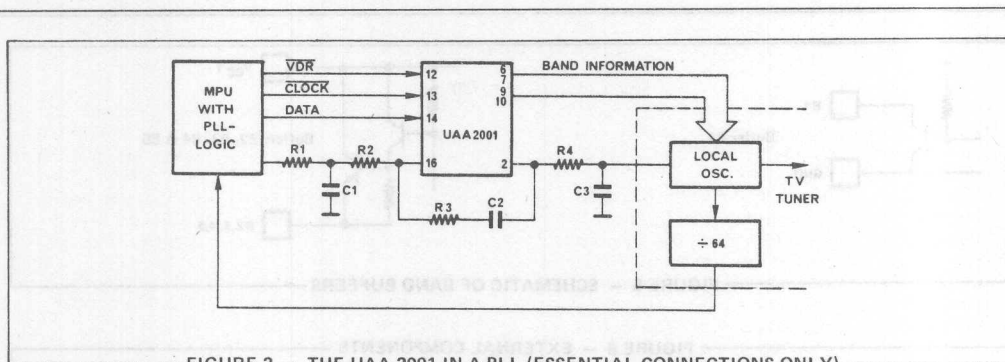


FIGURE 2 — THE UAA 2001 IN A PLL (ESSENTIAL CONNECTIONS ONLY)

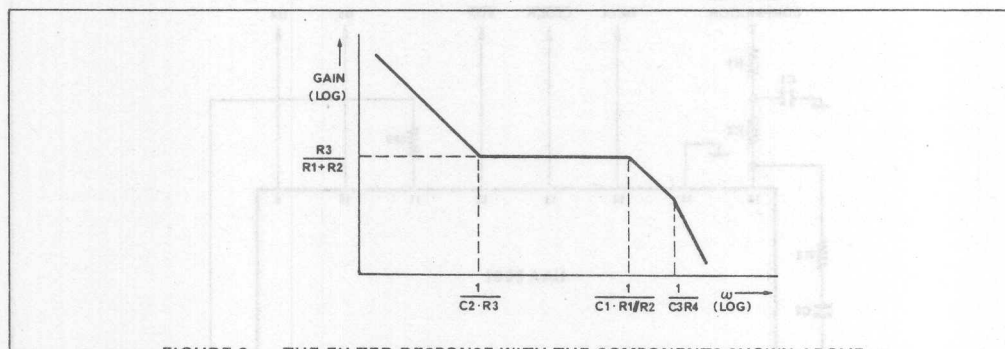
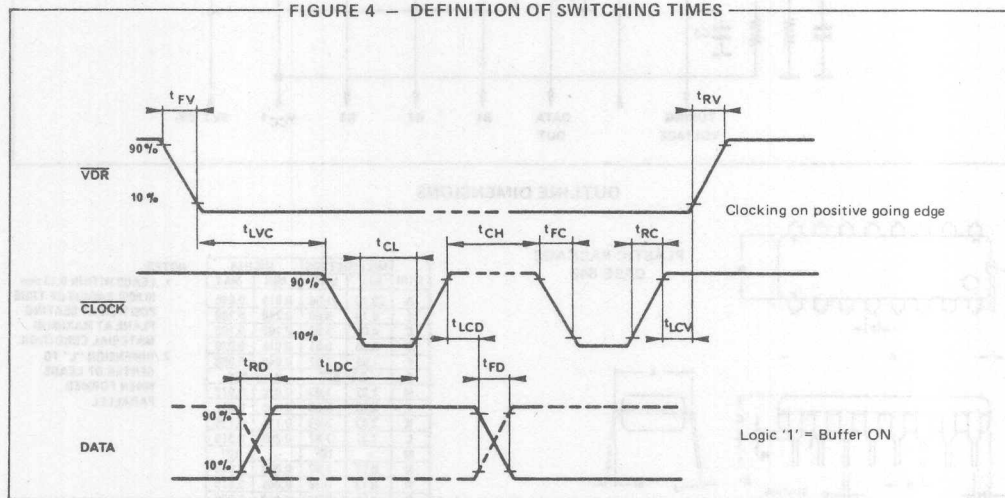


FIGURE 3 — THE FILTER RESPONSE WITH THE COMPONENTS SHOWN ABOVE

FIGURE 4 — DEFINITION OF SWITCHING TIMES



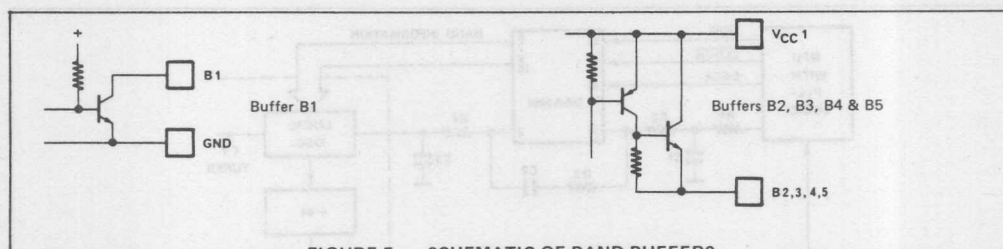


FIGURE 5 — SCHEMATIC OF BAND BUFFERS

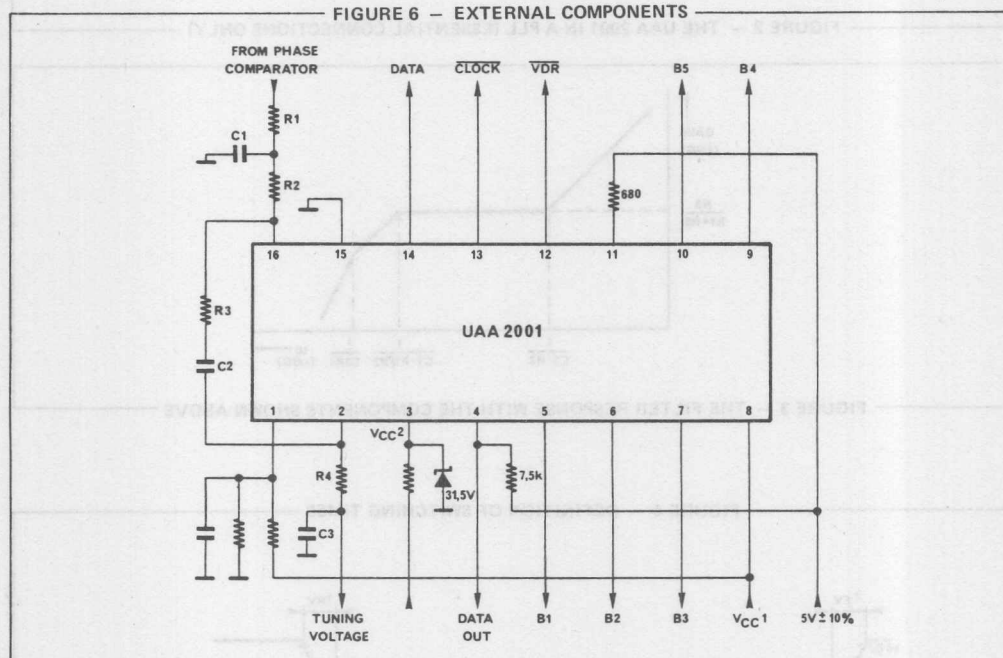
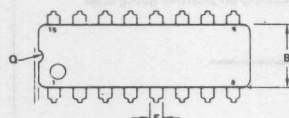
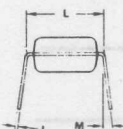
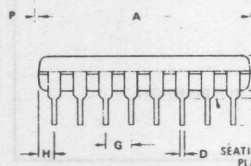


FIGURE 6 — EXTERNAL COMPONENTS

OUTLINE DIMENSIONS



PLASTIC PACKAGE
CASE 648



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

UAA2010

Advance Information

SYNTHESIZER AMPLIFIER & DRIVER

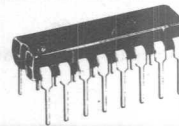
The UAA 2010 is designed for use in frequency synthesizers. It is particularly suitable for use with the MC 6805T2 microprocessor (MPU) in a TV synthesizer where it forms the interface between the tuner and the MPU. The circuit is realised in bipolar and I²L Technology.

- Direct tuner drive from 4 band drivers
- Direct control of the tuner's varicap diode
- Interface for external open collector band drivers
- Extremely low input current (1nA typical)

SYNTHESIZER

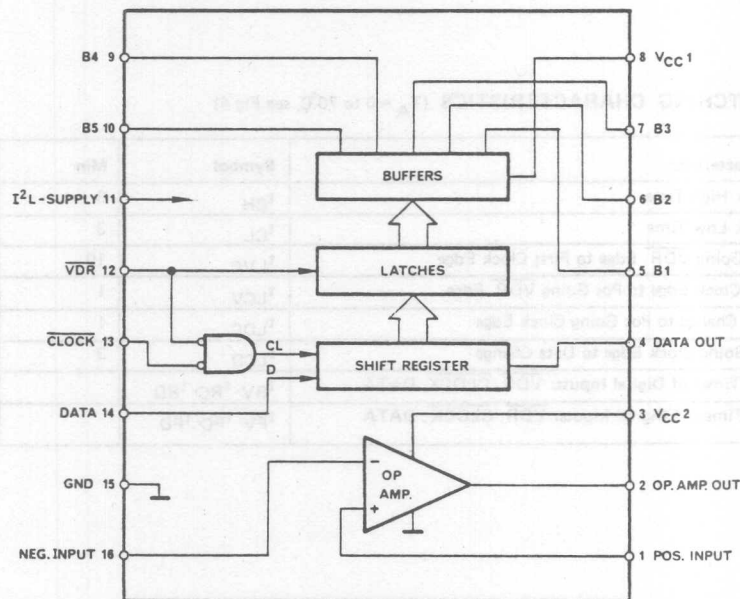
AMPLIFIER & DRIVER

MONOLITHIC SILICON
INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

FIGURE 1 - BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Pin	Symbol	Value	Unit
Logic Input Voltages	12,13, 14	V_{LOG}	15	V
Operational Amplifier:				
Input Voltage Range	16,1		0 to 15	V
Short Circuit Duration (protected from 0 to V_{CC2})	2	t_s	continuous	
Analogue Supply Voltage	3	V_{CC2}	35	V
Buffer Supply Voltage	8	V_{CC1}	18	V
Data Out, max Voltage ($I_D = 1\text{mA}$)	4		10	V
Buffer B1	5			
Output Voltage at Logical '0'			20	V
Output Current at Logical '1' (needs external current limit)			7	mA
Buffers B2, B3, B4 & B5	6,7, 9,10			
Short Circuit Duration (protected from 0 to V_{CC1})			continuous	
$I^2\text{L}$ Supply Current	11	I_S	30	mA
Storage Temperature		T_{STG}	-50 to +150	$^\circ\text{C}$
Operating Ambient Temperature		T_A	0 to 70	$^\circ\text{C}$

All Voltages Referenced to Ground — pin 15

SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C , see Fig 4)

Characteristic	Symbol	Min	Max	Unit
Clock High Time	t_{CH}	3		μs
Clock Low Time	t_{CL}	3		μs
Neg Going $\overline{\text{VDR}}$ Edge to First Clock Edge	t_{LVC}	10		μs
Last Clock Edge to Pos Going $\overline{\text{VDR}}$ Edge	t_{LCV}	1		μs
Data Change to Pos Going Clock Edge	t_{LDC}	1		μs
Pos Going Clock Edge to Data Change	t_{LCD}	3		μs
Rise Times of Digital Inputs: $\overline{\text{VDR}}$, $\overline{\text{CLOCK}}$, DATA	t_{RV} , t_{RC} , t_{RD}		2	μs
Fall Times of Digital Inputs: $\overline{\text{VDR}}$, $\overline{\text{CLOCK}}$, DATA	t_{FV} , t_{FC} , t_{FD}		2	μs

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC1} = 12\text{V} \pm 10\%$, $V_{CC2} = 30$ to 33V) unless otherwise specified.

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Logic Input Levels, $\overline{\text{VDR}}$, $\overline{\text{CLOCK}}$, DATA	12, 13 14	V_{LOG}	0		0.8	V
Low State			2		6	V
High State						
Logic Input Currents		I_{LOG}			-100	μA
Low State					10	μA
High State						
Operational Amplifier						
Input Current	16, 1	I_{FI}		1	20	nA
Input Voltage		V_{CM}	2.2		12	V
Output Voltage ($V_{\text{CC2}} = 30$ to 33V , $I = 50\mu\text{A}$)	2					
Highest Level		V_{TH}	28		V_{CC2}	V
Lowest Level		V_{TL}	200		500	mV
Output Current						
Sourcing		I_{TS}		1.5	2	mA
Sinking		I_{TQ}	200	1	500	μA
Peak Noise						
Analogue Supply Voltage	3	V_{CC2}	30		33	V
Analogue Supply Current ($V_{\text{OUT}} = V_{\text{TL}}$)		I_{CC2}		2	4	mA
($V_{\text{OUT}} = V_{\text{TH}}$)			0.5	1.5		mA
Supply Voltage	8	V_{CC1}	10		15	V
Supply Current ⁽²⁾ ($I_{\text{LOG}} = 0$)		I_{CC1}	0.5		3	mA
($I_{\text{S}} = 0$, $V_{\text{CC1}} = 10$ to 15V)						
Data Out (open collector)						
Output Saturation Voltage ⁽¹⁾ at 1mA	4	V_{DO}			0.8	V
Leakage Currents for Logic '0'		I_{DL}			1	μA
(Output Voltage = 6V)						
Buffer B1						
Output Saturation Voltage ⁽¹⁾ at 2.5mA	5	V_{BO}			0.8	V
Leakage Current for Logic '0' at 15V		I_{BL}			5	μA
Buffers B2, B3, B4, B5	6, 7, 9, 10					
Output Current for Logic '1' at $V_{\text{CC1}} - 0.8\text{V}$		I_{BBO}	1	2.8	6	mA
$I^2\text{L}$ Supply Current						
$I^2\text{L}$ -Supply Voltage ($I_{\text{S}} = 7\text{mA}$)	11	V_{S}	0.7	1.2	1.7	V
Power Dissipation ($I_{\text{S}} = 7\text{mA}$, $V_{\text{CC1}} = 12\text{V}$, $V_{\text{CC2}} = 31.5\text{V}$)				90 ⁽²⁾ 110 ⁽³⁾		mV mW
Thermal Resistance, Chip to Ambient					80	$^\circ\text{C/W}$

All voltages are referred to Ground (pin 15)

- NOTES : 1) Current has to be limited externally
 2) Band Buffers B₂ to B₅ OFF
 3) One Band Buffer ON at $V_{\text{CC1}} - 0.8\text{V}$

CIRCUIT DESCRIPTION

The circuit operation can be followed by reference to fig 1, the UAA 2010 block diagram, and fig 2, a phase locked loop using the UAA 2010, the MC6805T2 MPU and a TV tuner.

The tuner's local oscillator output frequency is divided in a prescaler by 64 and then fed to the MC6805T2, which includes a variable divider, controller by the processor, a reference divider and a phase comparator. By means of this circuitry the local oscillator frequency is further divided by a number determining the TV channel and compared to a fixed reference frequency inside the MPU. The output voltage of the phase comparator is filtered by using the operational amplifier of the UAA 2010 and then serves as the control voltage for the local oscillator varicap.

To facilitate filtering of the reference frequency the op amp is designed for a very low input bias current (1nA typ). The standard filter set up is shown in fig 2 with the frequency response shown in fig 3. To ensure loop stability the response is flat around the frequency where the overall loop gain is unity.

The UAA 2010 also receives band switching information from the MPU and applies it to the tuner by means of a shift register, latches, and buffers. The 5-bit band switching information is transferred by the signals DATA,

CLOCK and VDR (chip select); these inputs are designed to accept TTL levels. The CLOCK and DATA lines can be shared with other systems having other I/O devices.

Fig 4 shows the circuit's timing diagram. On the negative going VDR edge the latches are disconnected from the shift register and new information is shifted in. On the positive going VDR edge the latches are reconnected thus transferring new band information to the buffers and the tuner.

The shift register also has a data output, this allows the MPU to pass data through the UAA 2010 and drive further circuits from the same DATA and chip select pins. The UAA 2010 shifts and outputs data on the positive going clock edge where the following circuits are intended to shift data on the negative going edge. For reliable data transfer the UAA 2010 should always be the first circuit in line as the clock signal consists of negative going pulses.

The latches control five buffers. Buffer B1 has an open collector output (see fig 5) and may be used to output any information from the MPU. Buffers B2 to B5 are band buffers specially designed to control external PNP drive transistors.

INPUT/OUTPUT FUNCTIONS

POS. INPUT — (pin 1) This is the non-inverting input to the operational amplifier and needs an external reference bias.

OP. AMP. OUT — (pin 2) This is the tuning voltage output, designed for direct control of the tuner's varicap.

V_{CC2} — (pin 3) This is the op amp supply voltage.

DATA OUT — (pin 4) This pin is the data output of the shift register. The output is designed to allow cascading other circuits using the same VDR signal.

B1 — (pin 5) This pin is an open collector buffer output of the first shifted bit. When shifting a logic '1' the output transistor is ON.

BAND DRIVER OUTPUTS — (pins 6, 7, 9 & 10) These outputs control external PNP transistors for band switching. When shifting a logic '1' the appropriate band buffer (external PNP) is ON.

V_{CC1} — (pin 8) This is the supply voltage for the band buffers.

I²L SUPPLY — (pin 11) This pin needs an external resistance to set up the I²L injector currents. The characteristic of the pin is that of a forward biased diode to pin 15 (ground) plus a series resistance of about 60Ω.

VDR — (pin 12) This is the chip select and is active when low.

CLOCK — (pin 13) This pin delivers the clock signal to the shift register, which accepts shifts and outputs data on the positive going edge. It should be noted that within the VDR window, when VDR is low, the clock has to be high at the beginning and end of the clock pulse train.

DATA — (pin 14) Data is entered serially into the circuit via this pin and passed directly to the shift register. In turn this controls the latches and band buffers.

NEG. INPUT — (pin 16) This is the inverting input of the op amp with a typical input bias current of 1nA, reducing with increasing temperature.

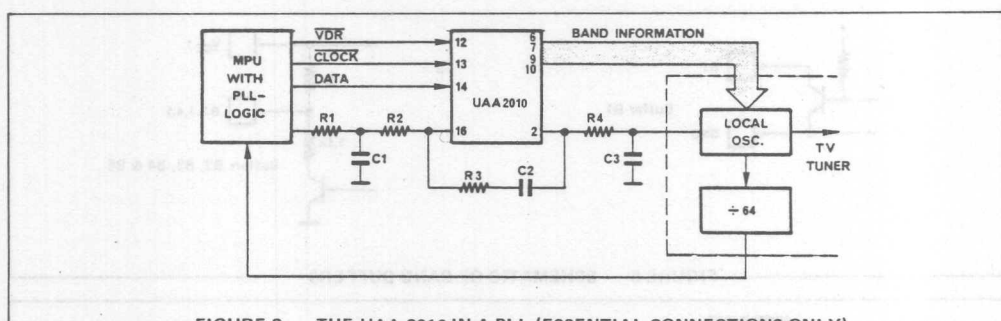


FIGURE 2 — THE UAA 2010 IN A PLL (ESSENTIAL CONNECTIONS ONLY)

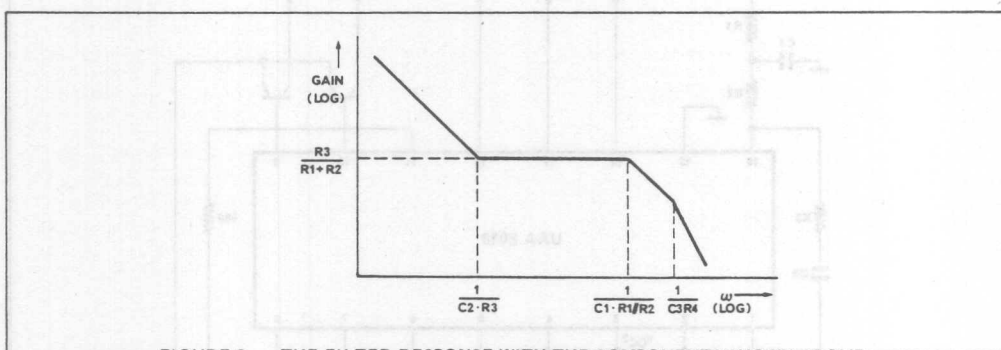


FIGURE 3 — THE FILTER RESPONSE WITH THE COMPONENTS SHOWN ABOVE

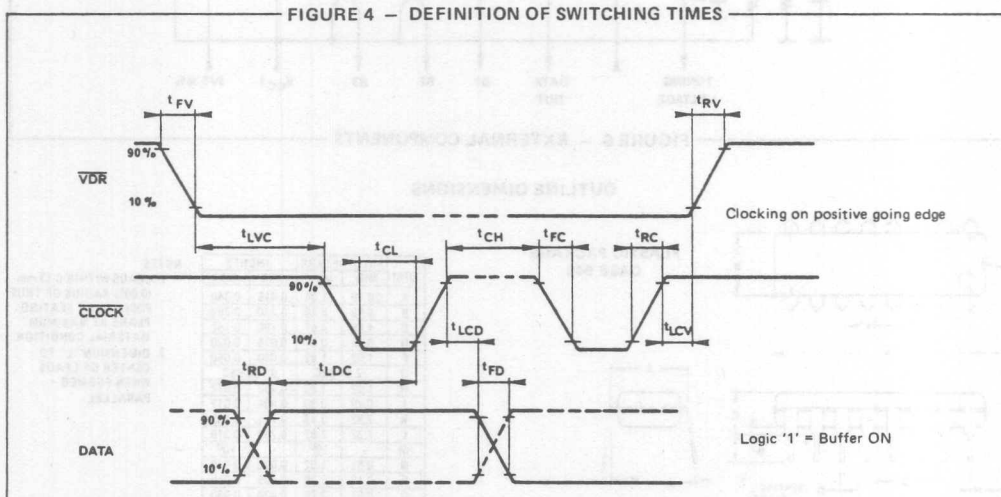


FIGURE 4 — DEFINITION OF SWITCHING TIMES



FIGURE 5 — SCHEMATIC OF BAND BUFFERS

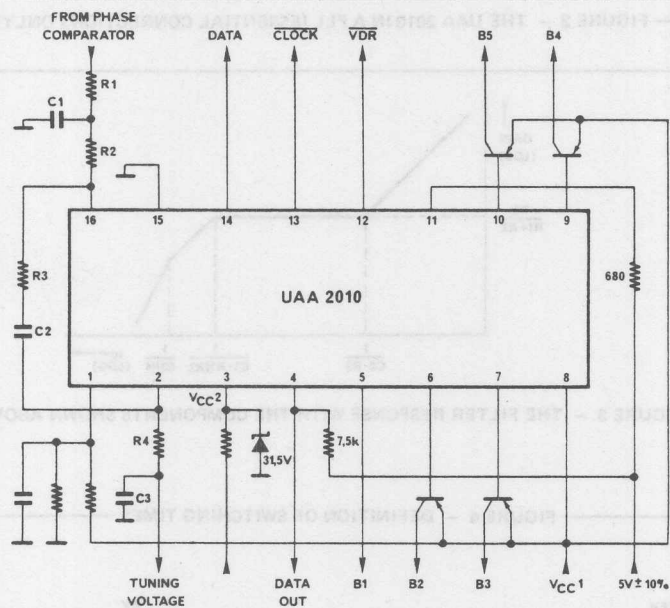
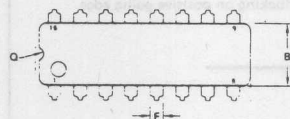
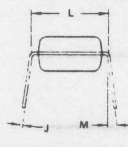
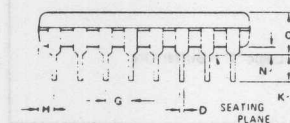


FIGURE 6 — EXTERNAL COMPONENTS

OUTLINE DIMENSIONS

PLASTIC PACKAGE
CASE 648

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.54 BSC		0.100 BSC	
G	1.32	1.83	0.052	0.072
H	0.20	0.30	0.008	0.012
I	2.92	3.43	0.115	0.135
J	7.37	7.87	0.290	0.310
K	—	10 ⁰	—	10 ⁰
L	0.51	1.02	0.020	0.040
M	0.13	0.38	0.005	0.015
N	0.51	0.76	0.020	0.030

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

SSOSAAU

UAA2011

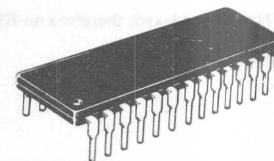
Product Preview

TV TIME BASE CIRCUIT

The UAA2011 is a dual loop time base with the line oscillator running at 125 KHz, followed by a divide by 8 counter for line frequency. Frame frequency is derived by counting down from the line oscillator.

- Phase comparison between sync pulse and oscillator
- Phase comparison between oscillator and flyback or scan
- Lock detector on filter switch
- Adjustable burstgate width
- Output stage for darlington drive
- Adjustable output duration allows "Wessel Power Supply"
- Countdown operation for 625 or 525 lines with output for driving colour system switch
- Height control compensated for 625/525 operation
- Blanking output starts prior to vertical sync. pulse and has accurate length

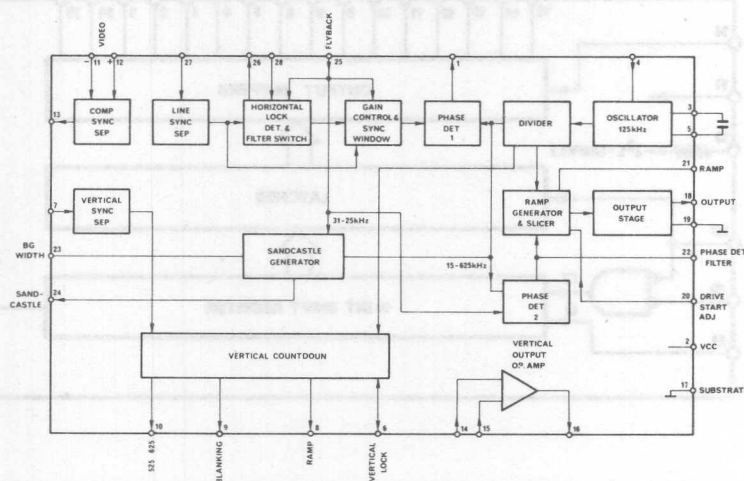
TV TIME BASE PROCESSOR



Case 710.02

3

BLOCK DIAGRAM



UAA 2022

Advance Information

16 SEGMENT LED DRIVER

The UAA 2022 is a 16-bit serial data input to a 16-segment LED driver. Brightness control of common anode LED's from an external control voltage is possible. The UAA 2022 is particularly suitable for Hi-Fi applications and is implemented in I^2L linear technology.

- LED brightness control voltage
- Current source segment driver outputs
- No external resistors for segment currents
- Non-multiplexed, therefore no RFI
- Cascadable

- LED brightness control voltage
- Current source segment driver outputs
- No external resistors for segment currents
- Non-multiplexed, therefore no RFI
- Cascadable

16 SEGMENT LED DRIVER

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

P-SUFFIX
PLASTIC PACKAGE
CASE 724

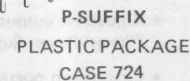
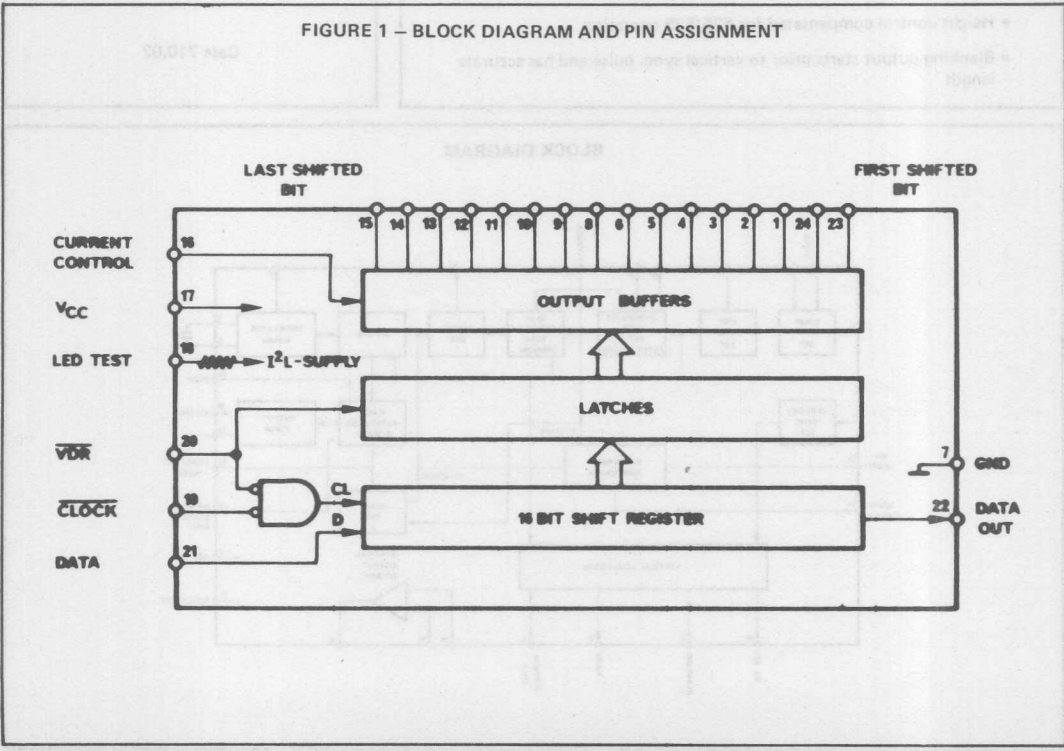


FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT

The block diagram illustrates the internal structure of the 74VHC04, showing a 16-bit shift register, latches, and output buffers. The shift register is clocked by the CLOCK pin (pin 19) and receives data from the DATA pin (pin 21). The latches are controlled by the CURRENT CONTROL pin (pin 16) and the LED TEST pin (pin 18). The output buffers output the data from the latches to the 16-bit shift register outputs (pins 15 to 0). The pin assignment shows pins 16, 17, 18, 20, 19, 21, 7, and 22.



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Pin	Symbol	Value	Unit
Logic Input Voltages	19, 20, 21	V_{LOG}	10	V
Control Voltage	16	V_{CO}	10	V
Supply Voltage	17	V_{CC}	10	V
Control Voltage	18	V_{LE}	10	V
Data Out, max. Voltage ($I_D = 2\text{mA}$)	22	V_D	10	V
Buffers Output Voltage ($V_{\text{CC}} = V_{\text{CO}} = 5.5\text{V}$) All Buffers ON	1 to 6 8 to 15 23, 24	V_{BB}	6	V
Storage Temperature		T_{STG}	-50 to +150	$^\circ\text{C}$
Operating Ambient Temperature		T_A	0 to 70	$^\circ\text{C}$

All voltages referenced to ground (Pin 7)

SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C , see figure 3)

Characteristic	Symbol	Min	Max	Unit
Clock "High"-Time	t_{CH}	3		μs
Clock "Low"-Time	t_{CL}	3		μs
Negative going $\overline{\text{VDR}}$ Edge to first Clock Edge	t_{LVC}	10		μs
Last Clock Edge to positive going $\overline{\text{VDR}}$ Edge	t_{LCV}	1		μs
Data Change to positive going Clock Edge	t_{LDC}	1		μs
Positive going Clock Edge to Data Change	t_{LCD}	3		μs
Rise Times of Digital Inputs $\overline{\text{VDR}}$, Clock, Data	$t_{\text{RV}}, t_{\text{RC}}, t_{\text{RD}}$		2	μs
Fall Times of Digital Inputs $\overline{\text{VDR}}$, Clock, Data	$t_{\text{FV}}, t_{\text{FC}}, t_{\text{FD}}$		2	μs

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Logic Input Levels, VDR, Clock, Data	19, 20, 21	V_{LOG}				
Low State			0		0.8	V
High State			2		6	V
Logic Input Currents		I_{LOG}				
Low State					-100	μA
High State					10	μA
Control Voltage Range ¹⁾	16	V_{CO}	0		V_{CC}	
Supply Voltage	17	V_{CC}	4.5		5.5	V
Control Current	16	I_{CO}			1	mA
Control Voltage, LED Test	18	V_{LE}				
Low Level (no Logic Supply, all Buffers ON)			0		0.5	V
High Level (normal Operation)			4.5V		V_{CC}	
Data Out (figure 2)						
Output Voltage, Logic "0" (1mA)		V_D			0.5	V
Internal Pull-Up Resistor					15	k Ω
Buffers	1 to 6, 8 to 15, 23, 24					
Mean Value of min. and max. Buffer Currents ($V_{CO} = V_{CC}$, $V_{LE} = 0$)		I_{BB}	9	11	13	mA
Buffer Current Variation around I_{BB}			-7 %		+7 %	
Saturation Voltage		V_S		1.2	1.8	V
Output Impedance		r_{out}		100		k Ω
Leakage Current ($V_{BB} = 5V$)		I_{BL}			10	μA
Supply Current LED-Test ($V_{LE} = 5V$)	18	I_{LE}	3	4.3	6	mA
Supply Current	17	I_{CC}	18		50	mA
Power Dissipation, all Buffers ON ($V_{CO} = V_{LE} = V_{CC}$) at $V_{BB} = 2.9V$				650		mW
Ambient Temperature		T_A	0		70	$^\circ C$
Package Thermal Resistance		R_{th}		70		$^\circ C/W$

All Voltages referenced to ground (Pin 7)

1) Brightness goes to zero at 2V

CIRCUIT DESCRIPTION

The UAA2022 is intended to control common anode LED's and allows brightness variation from an external control voltage. Since it is not multiplexed it is particularly suited for hi-fi applications etc.

The circuit receives 16 bit serial data by means of the digital inputs VDR (chip select), Clock and Data (TTL-levels). The information is fed into a shift-register, and then is stored in latches which in turn control the output buffers. These output buffers (segment drivers) have current source characteristics (see figure 2a), thus no external resistors are needed to set up the segment currents (for 100 % luminosity).

Figure 3 shows the timing diagram of the circuit. On the negative going VDR-edge the latches are disconnected

from the shift register and new information is shifted in. On the positive VDR-edge the latches are reconnected, thus transferring new information to the outputs. (See figure 2b.)

The shift register also has a data output. (See figure 2b.) This allows the microprocessor to pass data through the UAA 2022, and thus drive further circuits from the same data and chip-select pins. The UAA 2022 shifts and outputs data on the positive going clock edge. Thus for reliable data transfer, it has to be the first circuit in the line, when connected in series with circuits which shift on the negative going clock edge. The circuit is cascadable and can be cascaded with the UAA2000 and UAA2001/2010.

INPUT/OUTPUT FUNCTIONS

BUFFER OUTPUTS – (pins 1 to 6, 8 to 15, 23, 24)

These outputs have current source characteristics to drive the LED segments without external resistances.

CURRENT CONTROL – (pin 16)

Serves to vary the output currents of the buffers. This pin has to be connected to V_{CC} (pin 17) for maximum luminosity. The buffer currents decrease linearly with the control voltage, going down to zero at about 2V.

LED – TEST – (pin 18)

This pin supplies the logic section of the circuit, when connected to ground all output buffers are switched on.

CLOCK – (pin 19)

This pin delivers the clock signal to the shift register,

which accepts shifts and outputs data on the positive going edge. It should be noted that within the VDR-window, when VDR is low, the clock has to be high at the beginning and the end of the clock pulse train.

VDR – (pin 20)

This pin is the chip select and is active when low.

DATA – (pin 21)

Data is entered into the device serially via this pin and passed directly into the shift register. In turn, this controls the latches and output buffers. (Logic "1" = Buffer ON)

DATA OUT – (pin 22)

Is the data output of the shift register. Allows cascading with circuits operating on the same VDR and clock signals.

FIGURE 2 - CIRCUIT CONFIGURATIONS

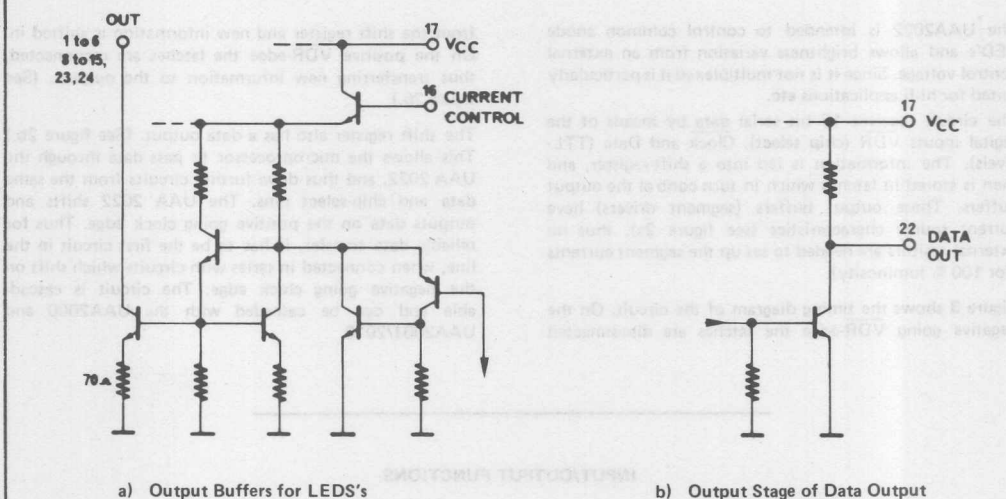
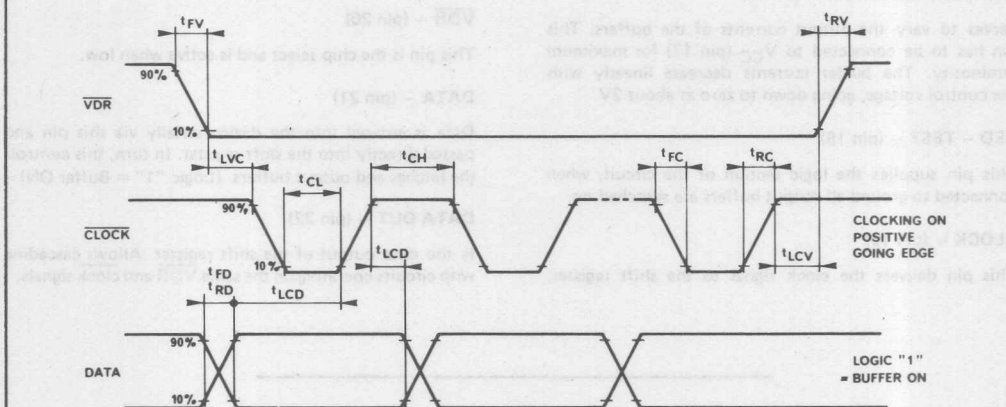
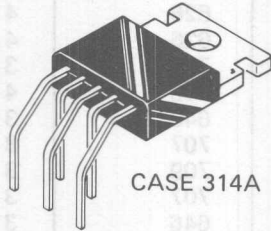


FIGURE 3 - DEFINITION OF SWITCHING TIMES



RADIO INTEGRATED CIRCUITS

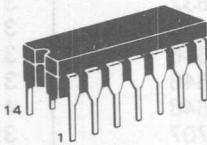
Section 4—Packages



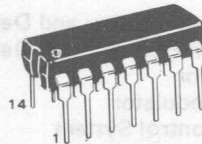
CASE 314A



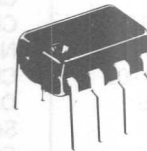
CASE 314B



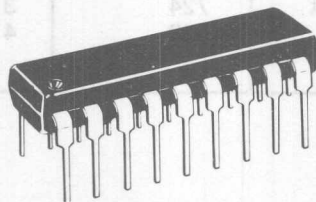
CASE 632 (TO116)



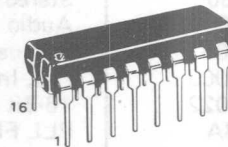
CASE 646 (TO116)



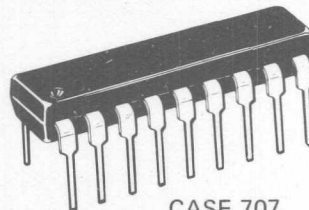
CASE 626



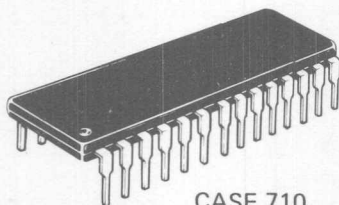
CASE 701



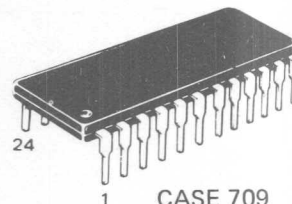
CASE 648



CASE 707



CASE 710



CASE 709

RADIO INTEGRATED CIRCUITS

Device	Designation	Package	Page
MC1306P	1/2-Watt Audio Amplifier	626	4 - 3
MC1309	FM Stereo Demodulator	646	4 - 8
MC1310	FM Stereo Demodulator	646	4 - 10
MC3357	Low Power FM/IF	648	4 - 18
MC3359	High Gain Low Power FM/IF	701	4 - 22
MC3393P	Two Modulus Prescaler	626	4 - 25
MC3396P	Divide by 20 Prescaler	626	4 - 27
MC6203	Remote Control Receiver	710	3 - 23
MC6220	MCU with PLL	710	4 - 29
MC14430	Input Address Encoder	648	3 - 47
MC14497P	CMOS PCM Remote Control Transmitter	707	3 - 55
MC144100	CMOS Duplex Mode 32-Segment LED Driver	709	3 - 67
MC144110	CMOS Hex Static D/A Converter	707	3 - 74
MC144111	CMOS Quad Static D/A Converter	646	3 - 74
MC144115	CMOS 2-Digit/16-Segment LCD Driver	709	3 - 80
MCM2801	NMOS 16 x 16 Electrically Erasable PROM	632	3 - 86
MCM144102	CMOS 16/16 Word-Static Ram	626	3 - 98
SAA1006	Diode Matrix Encoder	648	3 - 103
SMA2001	See MCM2801	632	3 - 86
TBA120C	FM/IF Amplifier + Limiter and Detector	646	3 - 105
TBA120D	FM/IF Amplifier + Limiter and Detector	646	3 - 105
TBA2110	FSK Demodulator	646	3 - 121
TCA4500A	FM Stereo Demodulator	648	4 - 31
TCA5500	Stereo Sound Control System	707	3 - 124
TDA2002, A	Audio Power Amplifier	314A/314B	3 - 132
UAA2002	Frequency Synthesizer Prescaler	646	4 - 38
UAA2003	PLL Interface	648	4 - 43
UAA2022	16-Bit LED Driver/or MPU Interface Unit	724	3 - 182
μA758A	PLL FM Stereo Demodulator	648	4 - 47

MC1306P

1/2-WATT AUDIO AMPLIFIER



PLASTIC PACKAGE
CASE 626

1/2-WATT AUDIO AMPLIFIER

The MC1306P is a monolithic complementary power amplifier and preamplifier designed to deliver 1/2-Watt into a loudspeaker with a 3.0 mV(rms) typical input. Gain and bandwidth are externally adjustable. Typical applications include portable AM-FM radios, tape recorder, phonographs, and intercoms.

- 1/2-Watt Power Output (12 Vdc Supply, 8-Ohm Load)
- High Overall Gain – 3.0 mV(rms) Sensitivity for 1/2-Watt Output
- Low Zero-Signal Current Drain – 4.0 mA @ 9.0 V typ
- Low Distortion – 0.5% at 250 mW typ

TYPICAL APPLICATIONS

FIGURE 1 – AM-FM RADIO, AUDIO SECTION

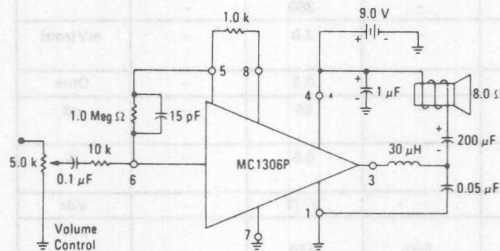
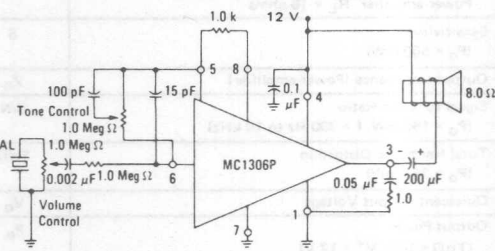
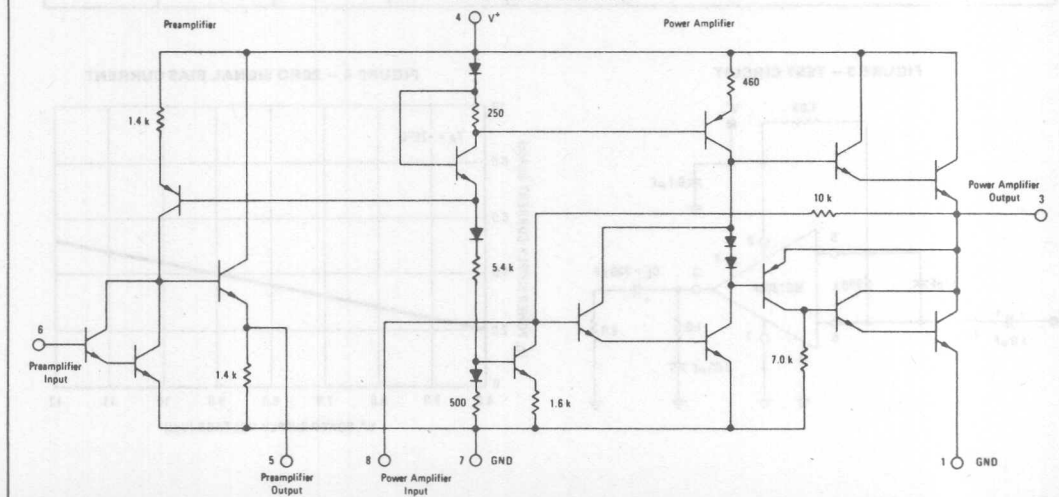


FIGURE 2 – PHONOGRAPH AMPLIFIER
(CERAMIC CARTRIDGE)



CIRCUIT SCHEMATIC



MC1306P

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	15	Vdc
Load Current	I_L	400	mA dc
Power Dissipation (Package Limitation) $T_A = +25^\circ\text{C}$	P_D	625	mW
Derate above $T_A = +25^\circ\text{C}$	$1/\theta_{JA}$	5.0	mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	0 to $+75$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$	$^\circ\text{C}$

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS ($V^+ = 9.0\text{ V}$, $R_L = 8.0\text{ ohms}$, $f = 1.0\text{ kHz}$, (using test circuit of Figure 3), $T_A = +25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Open Loop Voltage Gain Pre-amplifier $R_L = 1.0\text{ k ohm}$ Power-amplifier $R_L = 16\text{ ohms}$	A_{VOL}	—	270 360	—	V/V
Sensitivity ($P_O = 500\text{ mW}$)	S	—	3.0	—	mV(rms)
Output Impedance (Power-amplifier)	Z_O	—	0.5	—	Ohm
Signal to Noise Ratio ($P_O = 150\text{ mW}$, $f = 300\text{ Hz to }10\text{ kHz}$)	S/N	—	55	—	dB
Total Harmonic Distortion ($P_O = 250\text{ mW}$)	THD	—	0.5	—	%
Quiescent Output Voltage	V_O	—	$V^+/2$	—	Vdc
Output Power (THD $\leq 10\%$, $V^+ = 12\text{ V}$)	P_O	500	570	—	mW
Current Drain (zero signal)	I_D	—	4.0	—	mA
Power Dissipation (zero signal)	P_D	—	36	—	mW

FIGURE 3 — TEST CIRCUIT

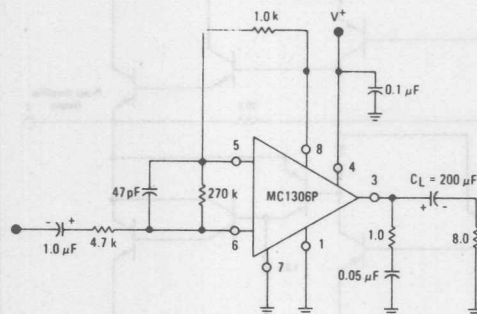
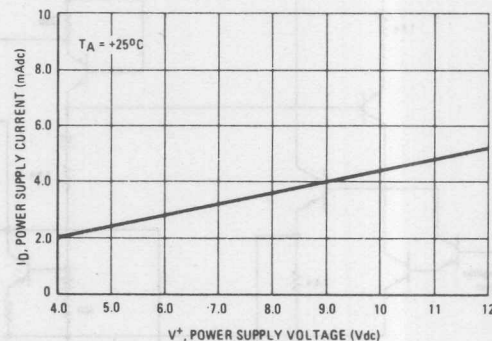


FIGURE 4 — ZERO SIGNAL BIAS CURRENT



TYPICAL CHARACTERISTICS

(V⁺ = 9.0 V, f = 1.0 kHz, T_A = +25°C unless otherwise noted)

FIGURE 5 - EFFICIENCY

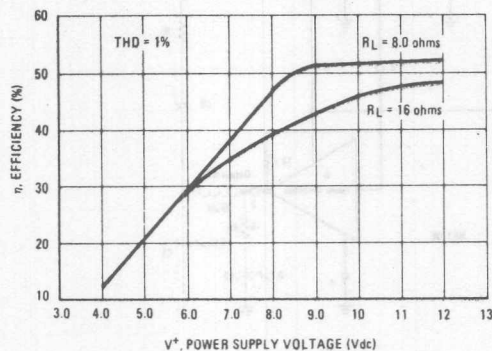


FIGURE 6 - OUTPUT POWER

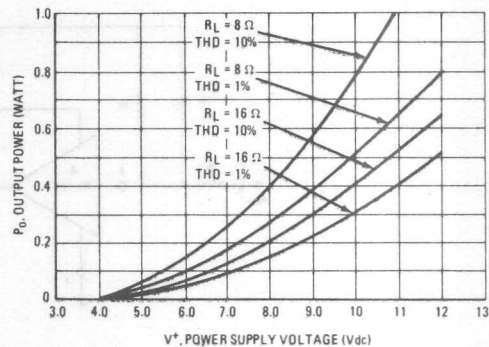


FIGURE 7 - TOTAL HARMONIC DISTORTION

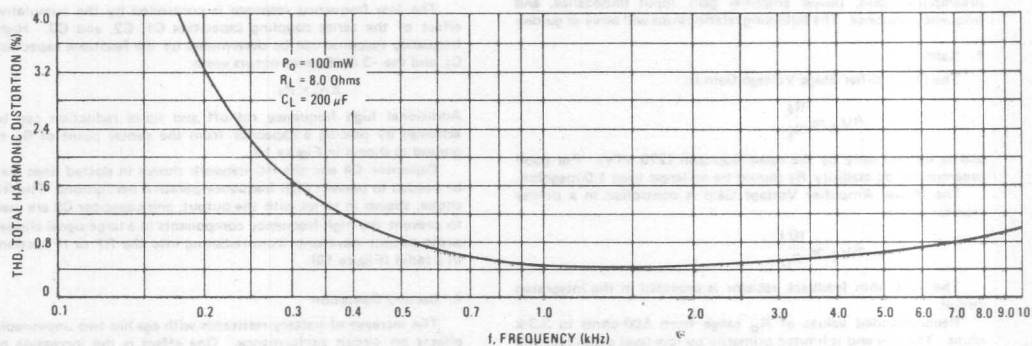
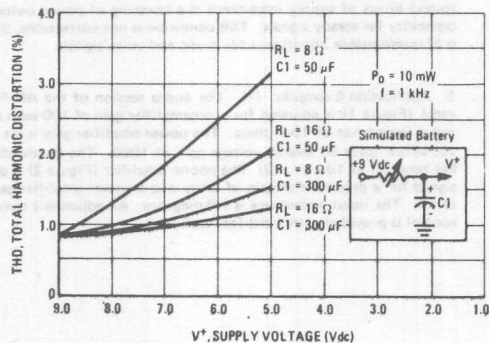
FIGURE 8 - EFFECT OF BATTERY AGING
ON LOW-LEVEL DISTORTION

FIGURE 9 - DISTORTION

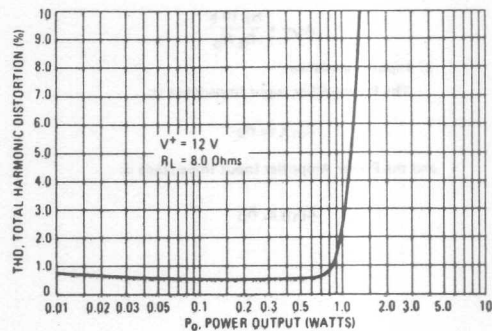
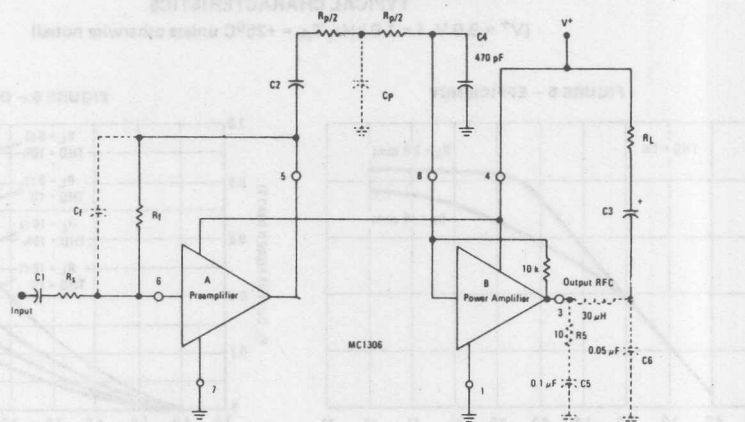


FIGURE 10 – TYPICAL CIRCUIT CONNECTION



DESIGN CONSIDERATIONS

The MC1306P provides the designer with a means to control preamplifier gain, power amplifier gain, input impedance, and frequency response. The following relationships will serve as guides.

1. Gain

The Preamplifier Stage Voltage Gain is:

$$A_{V_A} \approx \frac{R_f}{R_s}$$

and is limited only by the open-loop gain (270 V/V). For good preamplifier dc stability R_f should be no larger than 1.0-megohm.

The Power Amplifier Voltage Gain is controlled in a similar manner where:

$$A_{VB} \approx \frac{10 \text{ k}}{R_D}$$

The 10-k ohm feedback resistor is provided in the integrated circuit.

Recommended values of R_p range from 500-ohms to 3.3-k-ohms. The low end is limited primarily by low-level distortion and the upper end is limited due to the voltage drive capabilities of the pre-amplifier. (A resistor can be added in the dc feedback loop, from pin 6 to ground, to increase this drive). The Overall Voltage Gain, then, is:

$$A_{VT} = \frac{R_f}{R_s} \frac{10\text{ k}}{R_D}$$

2. Input Impedance

The Preamplifier Input Impedance is:

$$Z_{inA} \approx R_s$$

and the Power Amplifier Input Impedance is:

$$Z_{inB} \approx R_p$$

3. Frequency Response

The low frequency response is controlled by the cumulative effect of the series coupling capacitors C1, C2, and C3. High-frequency response can be determined by the feedback capacitor, C_f, and the -3.0 dB point occurs when

$$X_{C_f} = R_f$$

Additional high frequency roll-off and noise reduction can be achieved by placing a capacitor from the center point of R_P to ground as shown in Figure 10.

Capacitor C4 and the RC network shown in dotted lines may be needed to prevent high frequency parasitic oscillations. The RF choke, shown in series with the output, and capacitor C6 are used to prevent the high-frequency components in a large-signal clipped audio output waveform from radiating into the RF or IF sections of a radio (Figure 10).

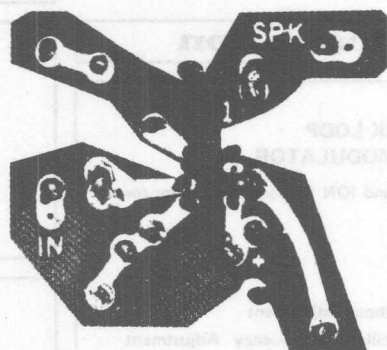
4. Battery Operation

The increase of battery resistance with age has two undesirable effects on circuit performance. One effect is the increasing of amplifier distortion at low signal levels. This is readily corrected by increasing the size of the filter capacitor placed across the battery (as shown in Figure 8; a 300- μ F filter capacitor gives distortions at low-tonal levels that are comparable to the 'stiff' supply). The second effect of supply impedance is a lowering of power output capability for steady signals. This condition is not correctable, but is of questionable importance for music and voice signals.

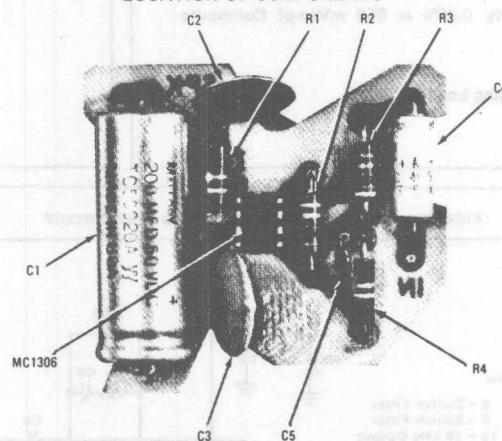
5. Application Examples: (1) The audio section of the AM-FM input (Figure 1) is adjusted for a preamplifier gain of 100 with an input impedance of 10-k ohms. The power amplifier gain is set at 10, which gives an overall voltage gain of 1000. The bandwidth has been set at 10-kHz. (2) The phono amplifier (Figure 2) is designed for a preamplifier gain of unity and a power amplifier gain of 10. The input impedance is 1.0-megohm. An adjustable treble control is provided within the feedback loop.

MC1306P

TYPICAL PRINTED CIRCUIT BOARD LAYOUT



LOCATION OF COMPONENTS



See Figure 3 for schematic diagram.

PARTS LIST

Component	Value
C1	200 μ F
C2	0.1 μ F
C3	0.05 μ F
C4	1.0 μ F
C5	47 pF
R1	1 ohm
R2	1 k ohm
R3	4.7 k ohms
R4	270 k ohms
MC1306	—
PC Board	—

MC1309

Advance Information

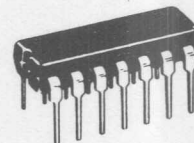
PHASE LOCK LOOP FM STEREO DEMODULATOR

... a monolithic device using I²L and ION Implant technology for use in solid-state stereo receivers.

- Requires No Inductors
- Low External Part Count
- Excellent Channel Separation Without Adjustment
- Only Single Potentiometer Oscillator Frequency Adjustment Necessary
- 50 mA Lamp or LED Driving Capability With Current Limiting
- Automatic, Transient-Free Stereo/Mono Switching
- Wide Dynamic Range: 0.25-1.7 V(p-p) Composite Input Signal
- Wide Supply Range: 4.5-16 Vdc
- Low Distortion: Typically 0.08% at 850 mV(p-p) Composite Input Signal
- Excellent SCA Rejection
- Gain Adjustable By Changing Load Resistors

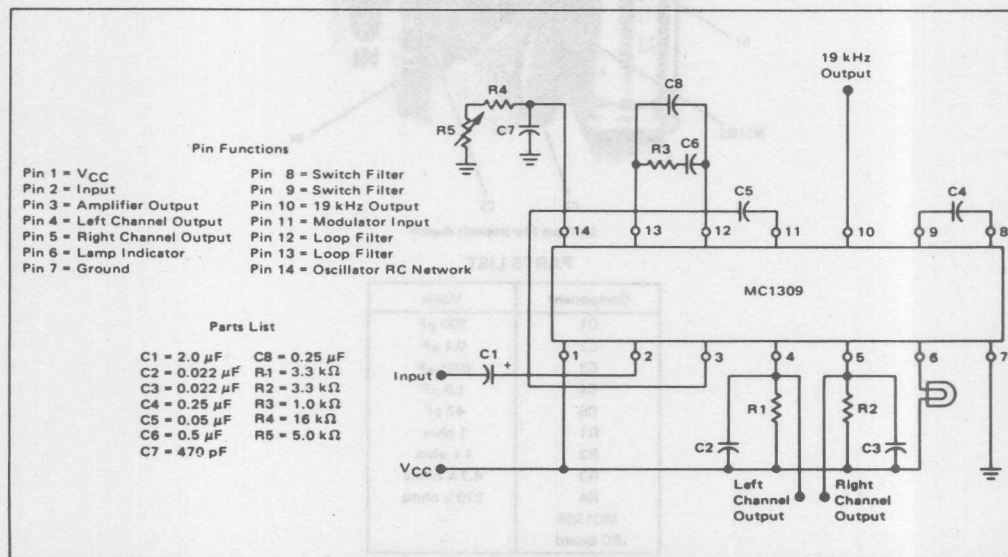
PHASE LOCK LOOP FM STEREO DEMODULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

FIGURE 1 - TYPICAL APPLICATION AND TEST CIRCUIT



This is advance information and specifications are subject to change without notice.

MC1309

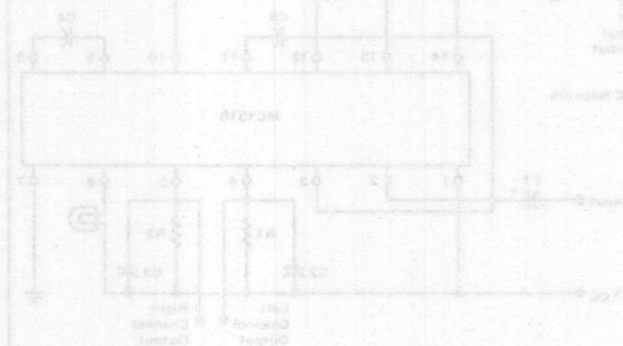
MAXIMUM RATINGS ($T_A = +25^\circ$ unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	16	Volts
Lamp Current	50	mA
Junction Temperature	150	$^\circ\text{C}$
Operating Temperature Range (Ambient)	-20 to +75	$^\circ\text{C}$
Storage Temperature Range	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS Unless otherwise noted; $V_{CC} = +9\text{ Vdc}$, $T_A = +25^\circ\text{C}$, 1.7 V(p-p) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level for stereo tests: 1.7 V(p-p) 1 kHz input signal for monaural tests; using circuit in Figure 1.

Characteristic	Min	Typ	Max	Unit
Current Drain	—	11	—	mA _{dc}
Maximum Standard Composite Input Signal (0.5% THD)* ($V_{CC} = 9.0\text{ V}$) ($V_{CC} = 6.0\text{ V}$)	1.7 0.85	2.1 1.7	—	V(p-p)
Maximum Monaural Input Signal (1.0% THD)* ($V_{CC} = 9.0\text{ V}$) ($V_{CC} = 6.0\text{ V}$)	1.7 0.85	2.2 1.7	—	V(p-p)
Channel Balance	—	0	1.0	dB
Stereo THD ($V_{in} = 0.85\text{ V(p-p)}$)	—	0.06	—	%
Monaural THD ($V_{in} = 0.85\text{ V(p-p)}$)	—	0.08	—	%
Channel Separation ($f = 100\text{ Hz}$) ($f = 1.0\text{ kHz}$) ($f = 10\text{ kHz}$)	— 30 —	45 47 40	—	dB
Monaural Gain	0.6	0.9	—	V/V
Input Impedance	15	30	—	k Ω
Ultrasonic Frequency Rejection 19 kHz 38 kHz	— —	35 45	—	dB
SCA Rejection	—	75	—	dB
Stereo Switch Level Lamp "On" Lamp "Off"	— 2.0	9.0 4.5	12 —	mV
Mono/Stereo Switching Transient — No Lamp	—	0	—	mV
Capture Range (Pilot = 60 mV(RMS))	—	± 7.0	—	%

*THD and Channel Separation are measured after a Bandpass Filter (200 Hz–10 kHz), unless otherwise specified.



MC1310

FM STEREO DEMODULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



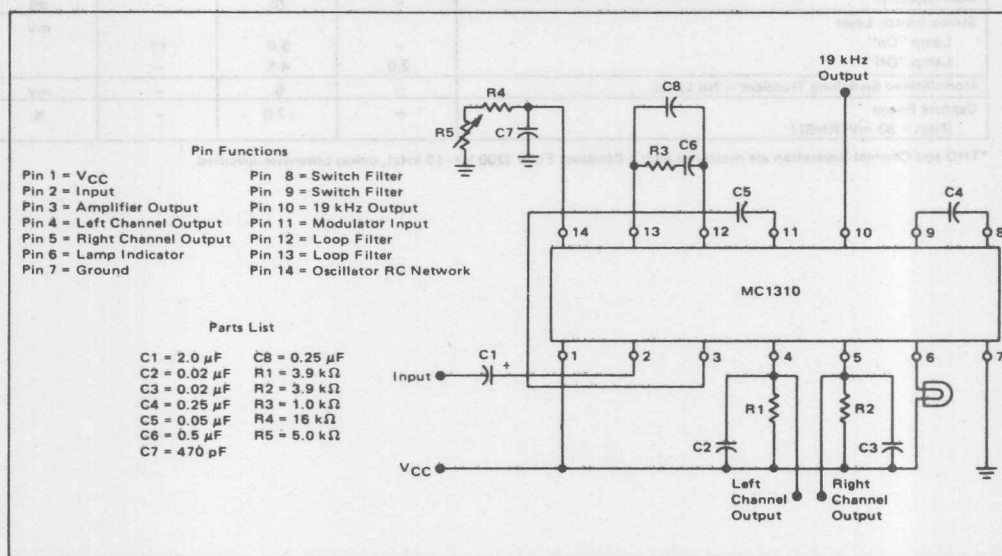
CASE 646

FM STEREO DEMODULATOR

... a monolithic device designed for use in solid-state stereo receivers.

- Requires no Inductors
- Low External Part Count
- Only Oscillator Frequency Adjustment Necessary
- Integral Stereo/Monaural Switch 75 mA Lamp Driving Capability
- Wide Dynamic Range: 0.5–2.8 V(p-p) Composite Input Signal
- Wide Supply Range: 8–14 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range
- Low Distortion: Typically 0.3% THD at 560 mV (RMS) Composite Input Signal
- Excellent SCA Rejection

FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT



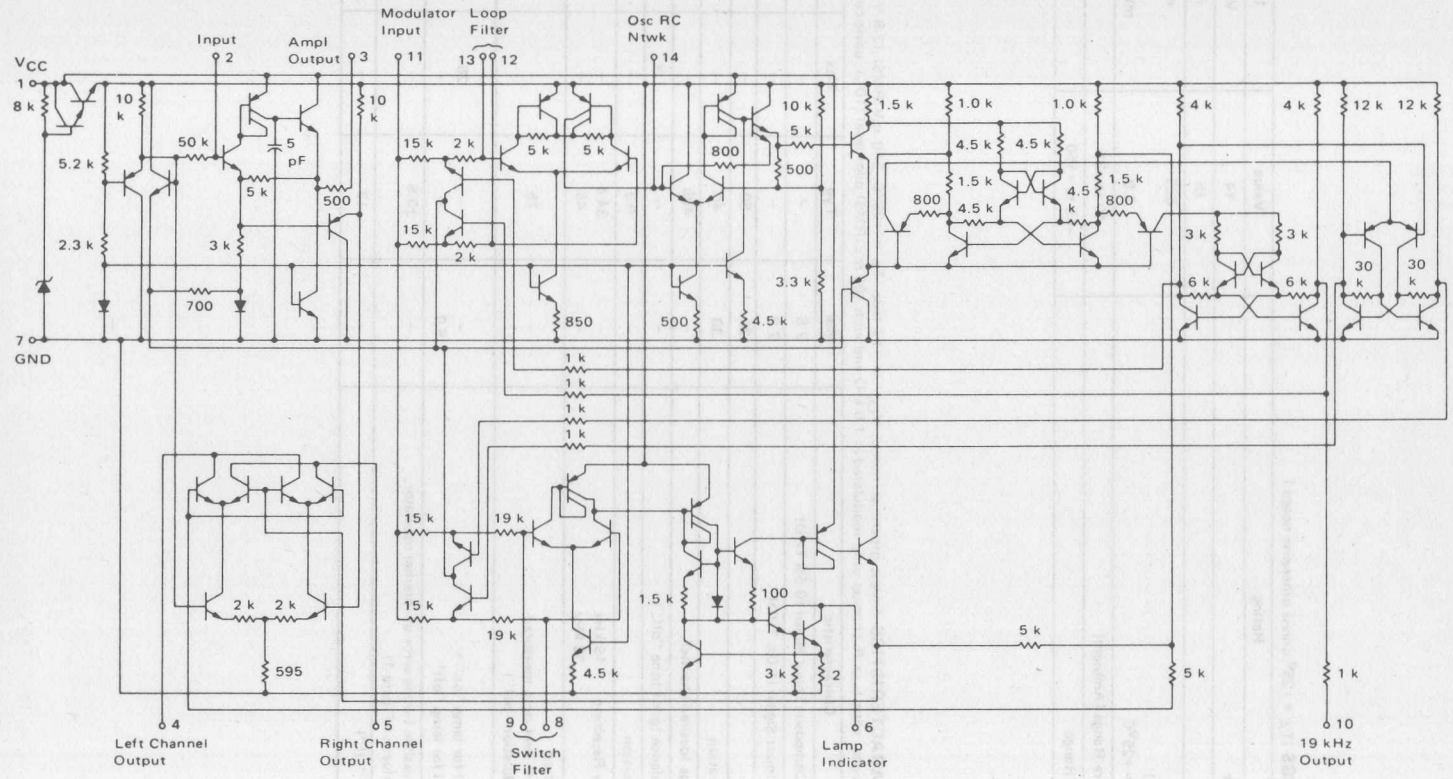
MAXIMUM RATINGS ($T_A = +25^\circ$ unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	14	Volts
Lamp Current	75	mA
Power Dissipation (Package limitation)	625	mW
Derate above $T_A = +25^\circ\text{C}$	5.0	mW/ $^\circ\text{C}$
Operating Temperature Range (Ambient)	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS Unless otherwise noted; $V_{CC} = +12\text{ Vdc}$, $T_A = +25^\circ\text{C}$, 560 mV(RMS) (2.8 V_(p-p)) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

Characteristic	Min	Typ	Max	Unit
Maximum Standard Composite Input Signal (0.5% THD)	2.8	—	—	V _(p-p)
Maximum Monaural Input Signal (1.0% THD)	2.8	—	—	V _(p-p)
Input Impedance	20	50	—	k Ω
Stereo Channel Separation	30	40	—	dB
Audio Output Voltage (desired channel)	—	485	—	mV(RMS)
Monaural Channel Balance (pilot tone "off")	—	—	1.5	dB
Total Harmonic Distortion	—	0.3	—	%
Ultrasonic Frequency Rejection	19 kHz	34.4	—	dB
	38 kHz	45	—	dB
Inherent SC A Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation "off")	—	75	—	dB
Stereo Switch Level				mV(RMS)
19 kHz input level for lamp "on"	—	—	20	
19 kHz input level for lamp "off"	5.0	—	—	
Capture Range (permissible tuning error of internal oscillator, reference circuit values of Figure 1)	—	± 3.5	—	%
Current Drain (lamp "off")	—	13	—	mAdc

FIGURE 2 - CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

Unless otherwise noted: $V_{CC} = +12 \text{ Vdc}$, $T_A = +25^\circ\text{C}$; 560 mV(RMS) (2.8 V_[p-p]) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

FIGURE 3 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

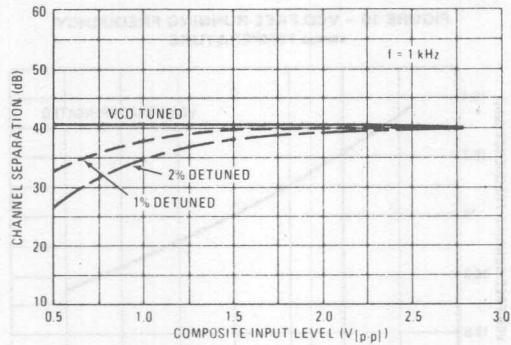


FIGURE 4 – CHANNEL SEPARATION versus FREQUENCY

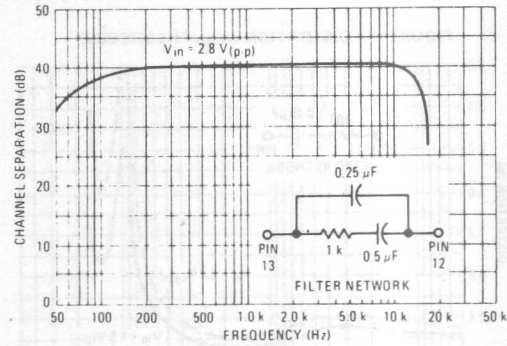


FIGURE 5 – CHANNEL SEPARATION versus VCO FREE RUNNING FREQUENCY

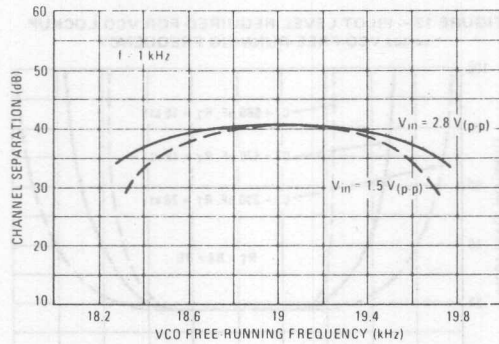


FIGURE 6 – CHANNEL SEPARATION versus SUPPLY VOLTAGE

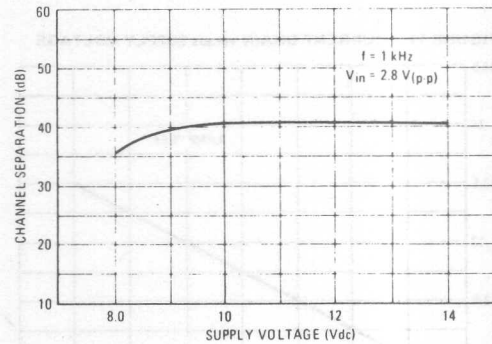


FIGURE 7 – THD versus COMPOSITE INPUT LEVEL *

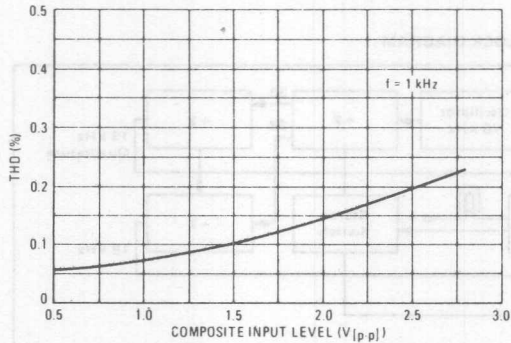
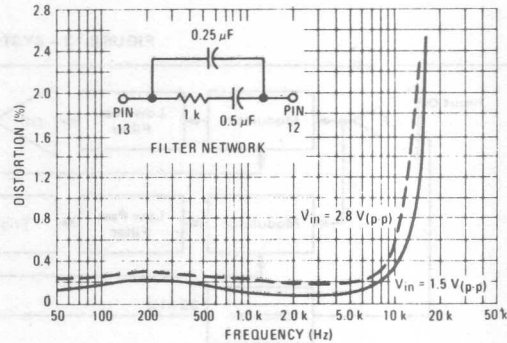


FIGURE 8 – DISTORTION versus FREQUENCY *



*Measured with Low Pass Filter (BW = 15 kHz).

TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DISTORTION versus FREQUENCY*

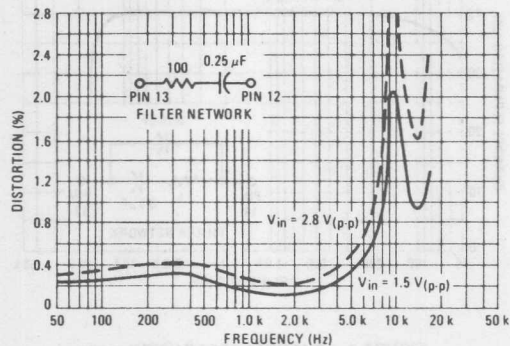


FIGURE 10 – VCO FREE-RUNNING FREQUENCY versus TEMPERATURE

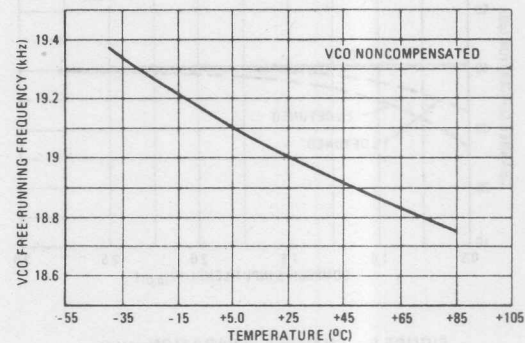
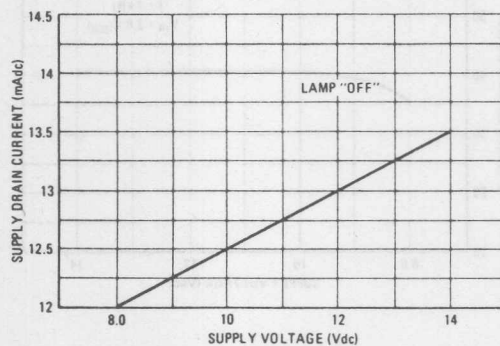


FIGURE 11 – CURRENT DRAIN versus SUPPLY VOLTAGE



*Measured with Low Pass Filter (BW = 15 kHz)

FIGURE 12 – PILOT LEVEL REQUIRED FOR VCO LOCKUP versus VCO FREE-RUNNING FREQUENCY

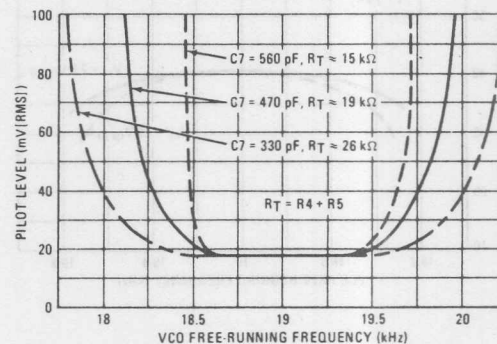
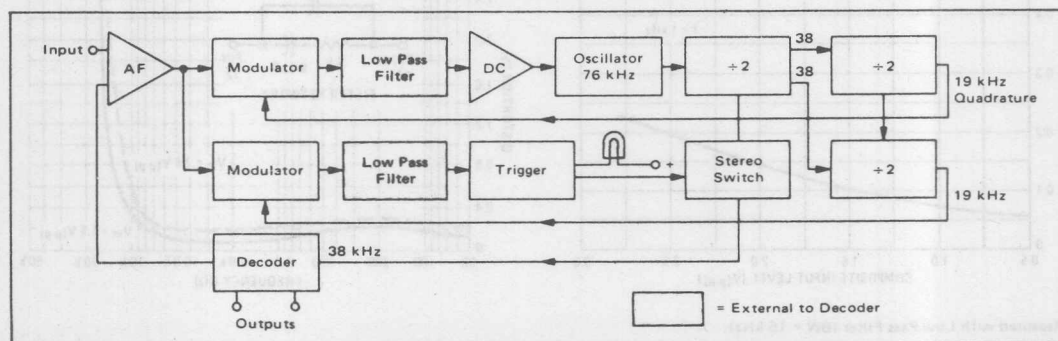


FIGURE 13 – SYSTEM BLOCK DIAGRAM



CIRCUIT OPERATION

Figure 13, on the previous page, shows the system block diagram. The upper line, comprising the 38-kHz regeneration loop operates as follows: the internal oscillator running at 76-kHz and feeding through two divider stages returns a 19-kHz signal to the input modulator. There the returned signal is multiplied with the incoming signal so that when a 19-kHz pilot tone is received a dc component is produced. The dc component is extracted by the low pass filter and used to control the frequency of the internal oscillator which consequently becomes phase-locked to the pilot tone. With the oscillator phase-locked to the pilot the 38-kHz output from the first divider is in the correct phase for decoding a stereo signal. The decoder is essentially another modulator in which the incoming signal is multiplied by

the regenerated 38-kHz signal. The regenerated 38-kHz signal is fed to the stereo decoder via an internal switch, which closes when a sufficiently large 19 kHz pilot tone is received.

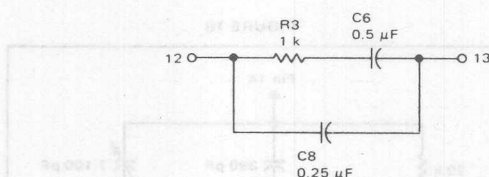
The 19-kHz signal returned to the 38-kHz regeneration loop modulator is in quadrature with the 19-kHz pilot tone when the loop is locked. With the third divider state appropriately connected, a 19-kHz signal in phase with the pilot tone is generated. This is multiplied with the incoming signal in the stereo switch modulator yielding a dc component proportional to the pilot tone amplitude. This component after filtering is applied to the trigger circuit which activates both the stereo switch and an indicator lamp.

APPLICATIONS INFORMATION

(Component numbers refer to Figure 1)

External Component Functions and Values

- C1 Input coupling capacitor; 2.0 μ F is recommended but a lower value is permissible if reduced separation at low frequencies is acceptable.
- R1, R2, C2, C3 See Maximum Load Resistance section.
- C4 Filter capacitor for stereo switch level detector; time constant is $C4 \times 53$ kilohms $\pm 30\%$, maximum dc voltage appearing across C4 is 0.25 V (pin 8 positive) at 100 mV(RMS) pilot level. The signal voltage across C4 is negligible.
- C5 See Phase Compensation section.
- R3, C6, C8 Phase-locked loop filter components; the following network is recommended:



When less performance is required a simpler network consisting of $R3 = 100$ ohms and $C6 = 0.25 \mu F$ may be used (omit C8). See Figure 9.

- R4, R5, C7 Oscillator timing network; recommended values:
- | | |
|--------------------|--------|
| C7 = 470 pF | 1% |
| R4 = 16 k Ω | 1% |
| R5 = 5 k Ω | Preset |

These values give $\pm 3.5\%$ typical capture range. Capture range may be increased by reducing C7 and increasing R4, R5 proportionally but at the cost of increasing beat-note distortion (due to oscillator-phase jitter) at high-signal levels. See Figure 12.

Stereo Lamp Nominal rating up to 75 mA at 12 V; the circuit includes surge limiting which restricts cold-lamp current to approximately 250 mA.

19-kHz Output A buffer output providing a 3.0-V_{pk} square wave at 19 kHz is available at pin 10. A frequency counter may be connected to this point to measure the oscillator free-running frequency for alignment. See Alignment section.

External Monaural/Stereo Switching

If it is desired to maintain the circuit in monaural mode, the following procedure must be followed. First, the stereo switch must be disabled to prevent false lamp triggering. This can be accomplished by connecting pin 8 negative or pin 9 positive by 0.3 volt. Pin 8 may be grounded directly if desired. Note that the voltage across C4 increases to approximately 2 volts with pin 9 positive when pin 8 is grounded.

Second, the 76-kHz oscillator must be killed to prevent interference when on AM. This can be accomplished by connecting pin 14 to ground via a current limiting resistor (3.3 kilohms is recommended).

Phase Compensation/IF Roll-off Compensation

Phase-shifts in the circuit cause the regenerated 38-kHz sub-carrier to lead the original 38 kHz by approximately 2° . The coupling capacitor C5 generates an

APPLICATIONS INFORMATION (continued)

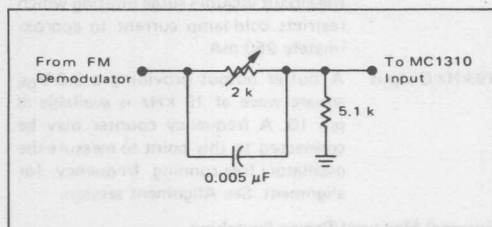
additional lead of 3.5° (for $C_5 = 0.05 \mu\text{F}$) giving a total lead of 5.5° .

The circuit is so designed that phase lag may be generated by adding a capacitor from pin 3 to ground. The source resistance at this point is 500 ohms. A capacitance of 820 pF compensates the 5.5° phase lead: increase above this value causes the regenerated sub-carrier to lag the original. However, a 5.5° phase error if left uncompensated will not degrade separation appreciably.

Note that these phase shifts occur within the phase-locked loop and affect only the regenerated 38-kHz sub-carrier: the circuit causes no significant phase or amplitude variation in the actual stereo signal prior to decoding.

Most IF amplifiers have a frequency response that limits separation to a value significantly lower than the capability of the MC1310. For example, if the response produces a 1-dB roll-off at 38 kHz, the separation will be limited to about 32 dB. This error can be compensated by using an RC lead network as shown in Figure 14. The exact values will be determined by the IF amplifier design. However, the values shown in Figure 14 are suitable for use with the MC1357 and MC1375 IF amplifiers.

FIGURE 14 — IF COMPENSATION NETWORK



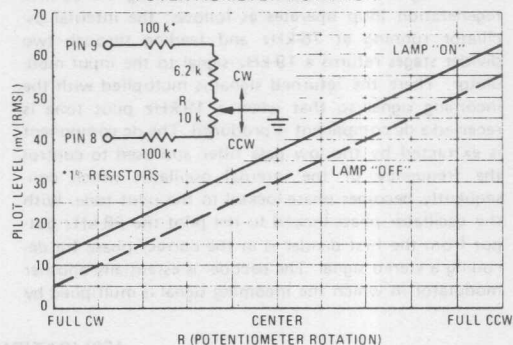
Voltage Control Oscillator Compensation

Figure 10 illustrates noncompensated Oscillator Drift versus temperature. The recommended T_C of the R4, R5, C7 combination is -300 PPM . This will hold the oscillator drift to approximately $\pm 1\%$ over a temperature range of -40 to $+85^\circ\text{C}$. Allowing $\pm 2\%$ for aging of the timing components acceptable performance is still obtained.

Lamp Sensitivity

It may be desirable in some cases, to change the lamp sensitivity due to differing signal levels produced by various FM detectors. The lamp sensitivity can be changed by making use of the external circuit shown. Typical sensitivities versus potentiometer rotation are also shown in Figure 15.

FIGURE 15 — PILOT SENSITIVITY versus POTENTIOMETER ROTATION



Alignment Procedure

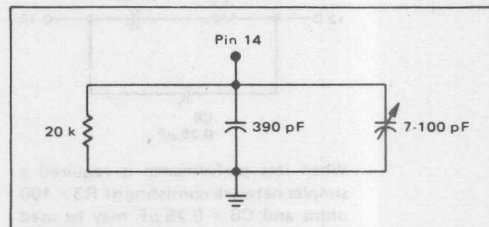
The optimum alignment procedure, with no input signal applied, is to adjust R5 until 19.00 kHz is read at pin 10 on the frequency counter.

Another procedure requiring no equipment, other than the receiver itself, will result in separation of within a few dB of optimum. This latter method is merely to tune the receiver to a stereo broadcast and adjust R5 until the pilot lamp turns "on". To find the center of the lock-in range, rotate the potentiometer back and forth until the center of the lamp "on" range is found. This completes the alignment.

Alternate Timing Network

The alternate timing network shown, incorporating a trimmer capacitor rather than a potentiometer, may be used if desired. Again, to provide correct temperature compensation, the temperature coefficient of the timing network must be approximately -300 PPM .

FIGURE 16

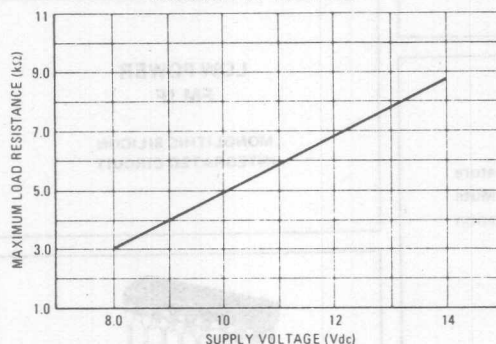


Maximum Load Resistance

The curve shown gives absolute maximum load resistance values versus supply voltage used for full-signal handling capability. With desired load resistance choose C2, C3 capacitors to provide standard $75 \mu\text{s}$ de-emphasis.

APPLICATIONS INFORMATION (continued)

FIGURE 17 — MAXIMUM LOAD RESISTANCE
versus SUPPLY VOLTAGE



Audio Output

The ratio $G = \frac{\text{p-p audio output (one-channel)}}{\text{p-p input signal}}$ for

different types of input is as follows:

INPUT	
Single-Channel Composite Signal	Monaural Signal
0.45	0.5

These figures are for 3.9-kilohm load resistors and for low-audio frequencies where de-emphasis roll-off is insignificant.

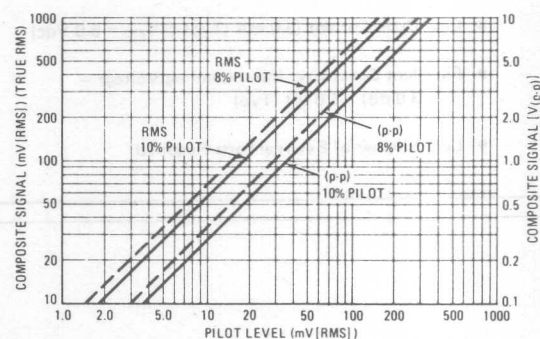
Capture Range versus Timing Components

The capture range can be changed to some extent by use of different timing components. Typical values are shown in Figure 12.

Composite Signal

Due to confusion concerning the measurement of the stereo composite signal, a curve showing both RMS and p-p composite levels versus pilot level follows, see Figure 18.

FIGURE 18 — COMPOSITE LEVEL versus PILOT
(L or R Modulation Only)



MC3357

Advance Information

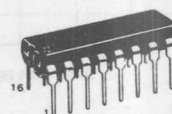
LOW POWER NARROW BAND FM IF

...includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ $V_{CC} = 6.0$ Vdc)
- Excellent Sensitivity: Input Limiting Voltage – (-3.0 dB) = $5.0 \mu\text{V}$ (Typ)
- Low Number of External Parts Required

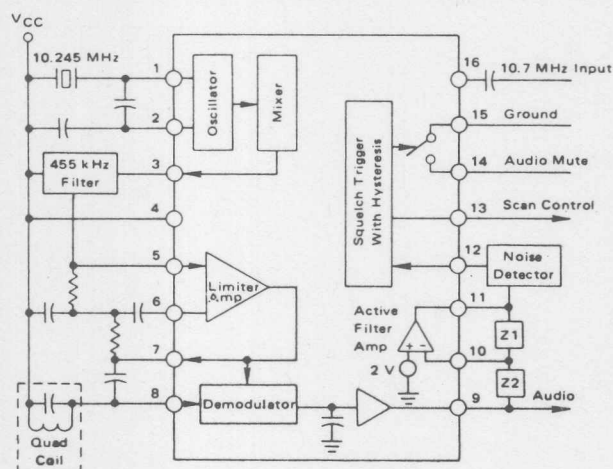
LOW POWER FM IF

MONOLITHIC SILICON
INTEGRATED CIRCUIT

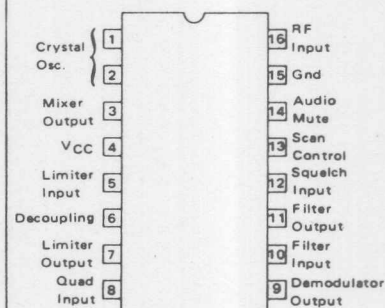


P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS

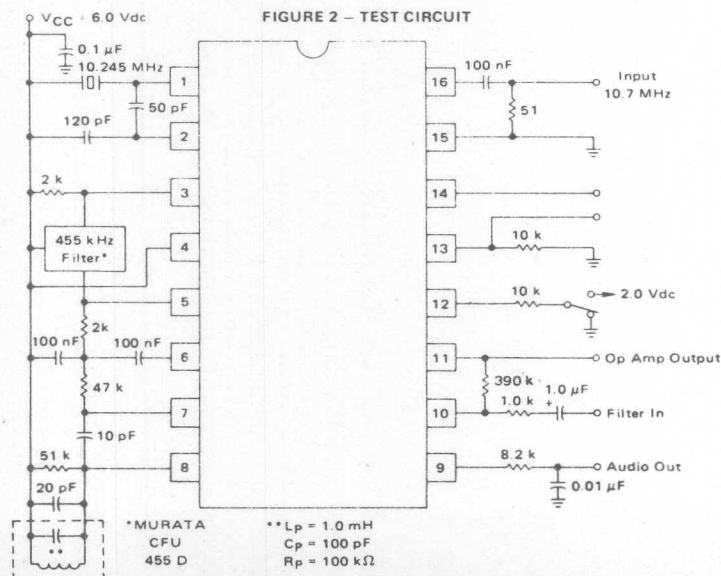


MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	$V_{CC}(\text{max})$	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	—	1.0	Vp-p
Input Voltage ($V_{CC} \geq 6.0$ Volts)	16	V_{16}	1.0	V _{RMS}
Mute Function	14	V_{14}	-0.5 to 5.0	V _{pk}
Junction Temperature	—	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	—	T_A	-30 to +70	$^\circ\text{C}$
Storage Temperature Range	—	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 6.0$ Vdc, $f_o = 10.7$ MHz, $\Delta f = \pm 3.0$ kHz, $f_{\text{mod}} = 1.0$ kHz, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current Squelch Off	4	—	2.0	—	mA
Squelch On	—	—	3.0	5.0	—
Input Limiting Voltage (-3 dB Limiting)	16	—	5.0	10	μV
Detector Output Voltage	9	—	3.0	—	Vdc
Detector Output Impedance	—	—	400	—	Ω
Recovered Audio Output Voltage ($V_{\text{in}} = 10$ mV)	9	200	350	—	mV _{rms}
Filter Gain (10 kHz) ($V_{\text{in}} = 5$ mV)	—	40	46	—	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	—	—	100	—	mV
Mute Function Low	14	—	15	50	Ω
Mute Function High	14	1.0	10	—	M Ω
Scan Function Low (Mute Off) ($V_{12} = 2$ Vdc)	13	—	0	0.5	Vdc
Scan Function High (Mute On) ($V_{12} = \text{Gnd}$)	13	5.0	—	—	Vdc
Mixer Conversion Gain	3	—	20	—	dB
Mixer Input Resistance	16	—	3.3	—	k Ω
Mixer Input Capacitance	16	—	2.2	—	pF



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly-balanced to reduce spurious responses. The input impedance at pin 16 is set by a 3 k Ω internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at pin 3 must be dc connected to B+, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC) the signal goes to the input of a five-stage limiter at pin 5.

The output of the limiter at pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at pin 7 is also used to supply dc feedback to pin 5. The other side of the first limiter stage is decoupled at pin 6.

The recovered audio is partially filtered, then buffered giving an impedance of around $400\ \Omega$ at pin 9. The signal still requires de-emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at pin 11 providing dc bias (externally) to the input at pin 10 which is referred internally to 2 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to pin 12.

An external positive bias to pin 12 sets up the squelch trigger circuit such that pin 13 is low at an impedance level of around 60 k Ω , and the audio mute (pin 14) is open circuit. If pin 12 is pulled down to 0.7 V by the noise or tone detector, pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 μ A and pin 14 is internally short-circuited to ground. There is 100 mV of hysteresis at pin 12 to prevent jitter. Audio muting is accomplished by connecting pin 14 to a high-impedance ground-reference point in the audio path between pin 9 and the audio amplifier.

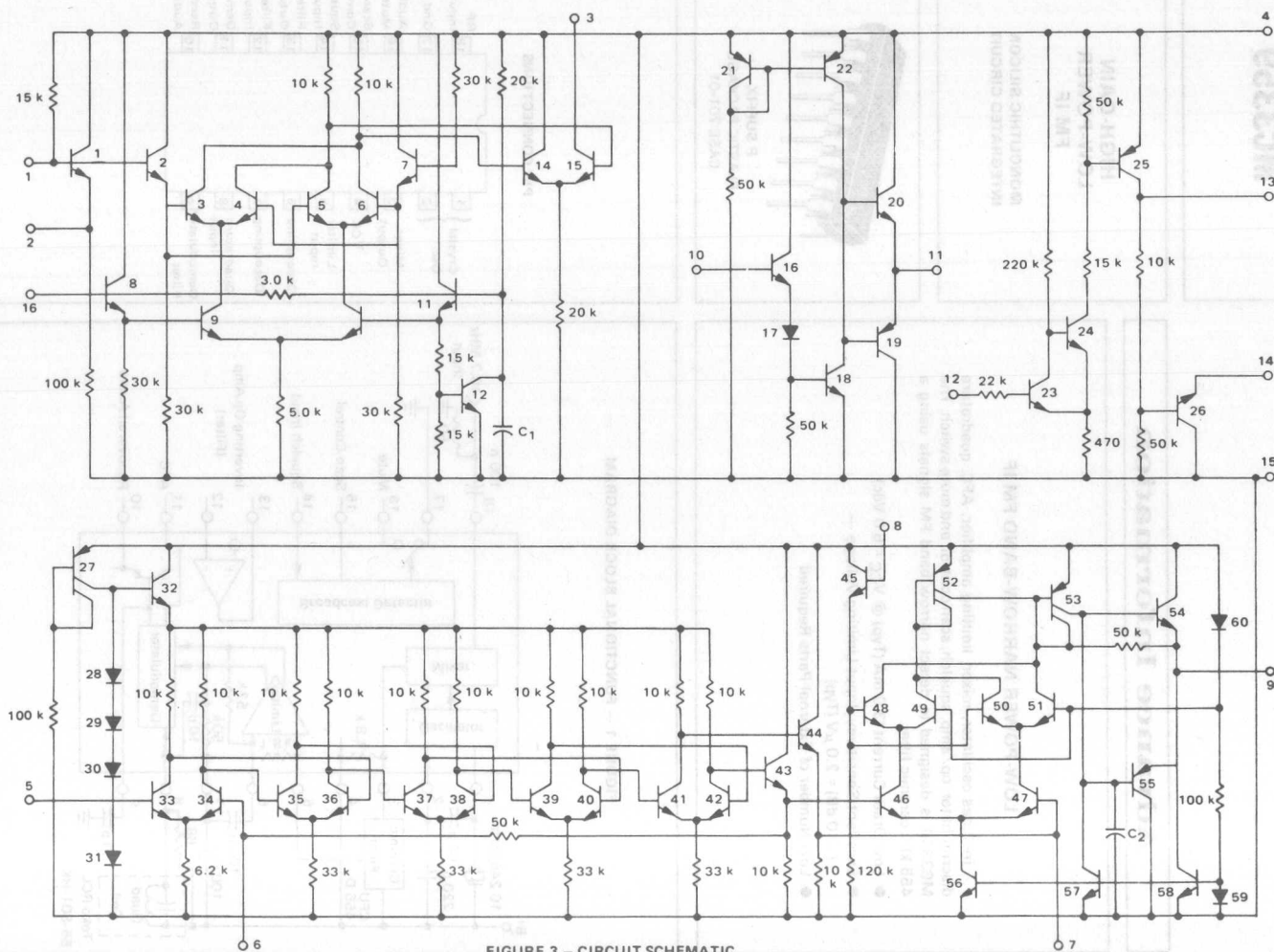


FIGURE 3 - CIRCUIT SCHEMATIC

MC3359

Advance Information

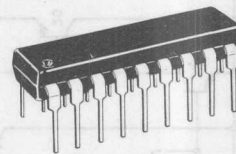
LOW-POWER NARROW-BAND FM IF

includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrow-band FM signals using a 455 kHz ceramic filter.

- Low Drain Current (3.0 mA (Typ) @ $V_{CC} = 6.0$ Vdc)
- Excellent Sensitivity: Input Limiting Voltage — (-3.0 dB) = $2.0 \mu V$ (Typ)
- Low Number of External Parts Required

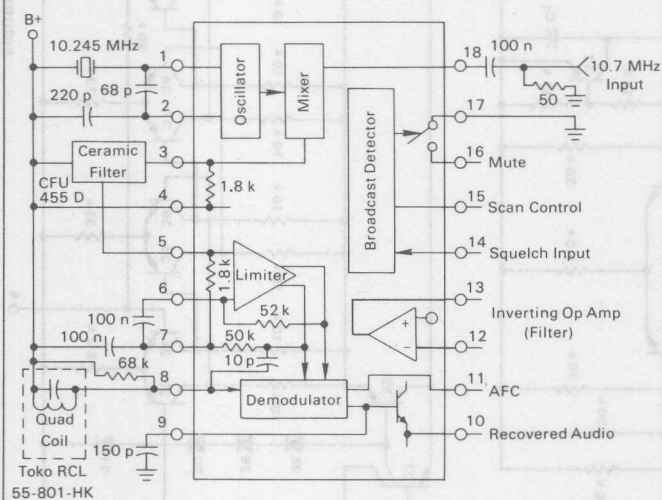
HIGH-GAIN LOW-POWER FM IF

MONOLITHIC SILICON
INTEGRATED CIRCUIT

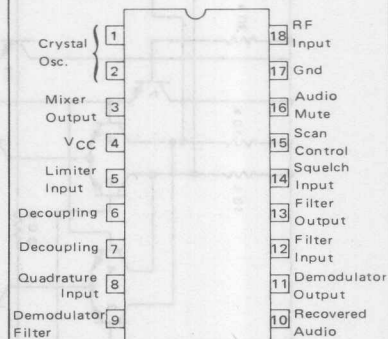


P SUFFIX
PLASTIC PACKAGE
CASE 701-01

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	$V_{CC}(\text{max})$	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 9	Vdc
Input Voltage ($V_{CC} \geq 6.0$ Volts)	18	18	1.0	V _{RMS}
Mute Function	16	V_{16}	-0.5 to 12	V _{pk}
Junction Temperature	—	T_J	150	$^\circ\text{C}$
Operating Ambient Temperature Range	—	T_A	-30 to +70	$^\circ\text{C}$
Storage Temperature Range	—	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 8.0$ Vdc, $f_o = 10.7$ MHz, $\Delta f = \pm 3.0$ kHz, $f_{\text{mod}} = 1.0$ kHz, 50 Ω source, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	4	—	—	—	mA
Squelch Off	—	—	3.0	6.0	—
Squelch On	—	—	4.0	7.0	—
Input Limiting Voltage (-3.0 dB Limiting)	18	—	2.0	6.0	μV
Output Voltage at AFC Balance	10	2.4	3.4	4.4	Vdc
Recovered Audio Output Voltage ($V_{in} = 3.0$ mV)	10	450	700	—	mVrms
Filter Gain (10 kHz) ($V_{in} = 5.0$ mV)	13	40	—	—	dB
Mute Switch Resistance ($I_{\text{test}} = 2.5$ mA)	16	—	4.0	10	Ω
Scan Source Current (Mute Off, $V_{15} = 0$)	15	2.5	—	—	mA
Mixer Conversion Gain (Figure 1)	5.0	—	28	—	dB
Mixer Input Resistance	18	—	3.6	—	k Ω
Mixer Input Capacitance	18	—	2.2	—	pF

CIRCUIT DESCRIPTION

The MC3359 is a low-power FM IF circuit designed primarily for use in voice-communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise after the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch-trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated. This can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly balanced to reduce spurious responses. The input impedance at pin 16 is set by a 3.6 k Ω internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The mixer output at pin 3 has a 1.8 k Ω impedance to match an external ceramic filter.

After suitable bandpass filtering, the signal goes to the input of a six-stage limiter at pin 5 whose impedance is again 1.8 k Ω . The output of the limiter drives a multiplier, both directly, and through a quadrature coil, to detect the FM.

An external capacitor at pin 9 can combine with the internal 50 k Ω to form a low-pass filter for the audio.

The audio is delivered through an emitter follower to pin 10, which may require an external resistor-to-ground to prevent the signal from rectifying with some capacitive loads.

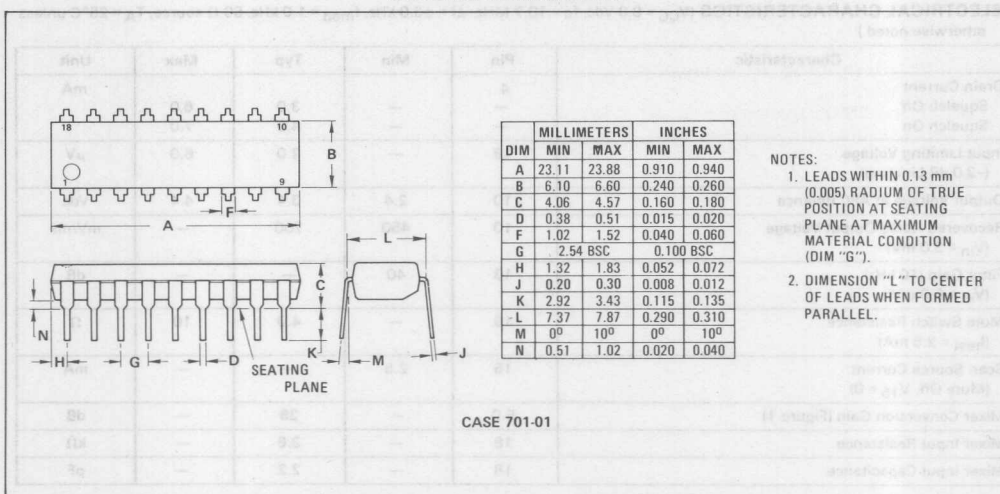
Pin 11 provides A.F.C. If A.F.C. is not required, pin 11 should be grounded, or it can be tied to pin 9 to double the recovered audio.

CIRCUIT DESCRIPTION (Continued)

A simple inverting op amp is provided with an output at pin 13 providing dc bias (externally) to the input at pin 12, which is referred internally to 2.3 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio band, or a tone signal. The result is applied to pin 14.

An external negative bias to pin 14 sets up the squelch-trigger circuit such that pin 15 is high, at an impedance level of about 2.5 k Ω , and the audio mute (pin 16) is open-circuit. If pin 14 is raised to 0.7 V by the noise or tone detector, pin 15 will go open-circuit and pin 16 is internally short-circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting pin 16 to a high-impedance ground-reference point in the audio path between pin 10 and the audio amplifier.

OUTLINE DIMENSIONS



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_D(T_A) = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)}$$

Where: $P_D(T_A)$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than

the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section
 T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

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MC3393P

Advance Information

TWO MODULUS PRESCALER

The MC3393P can divide by 15 and 16, and can be used with Motorola CMOS frequency synthesizers MC145146, 52, 56 for commercial AM-FM radio, land mobile and marine two-way radios, avionics radios, and scanner receivers.

- 140 MHz (typ) Toggle Frequency
- $\pm 15/16$
- TTL and CMOS Compatible Output
- Active Pullup and Pulldown
- +5.0 V Supply
- Buffered Clock Input
- 100-400 mV (typ) Input Sensitivity
- 200 Milliwatts (typ)

TWO MODULUS PRESCALER SILICON MONOLITHIC INTEGRATED CIRCUIT



N SUFFIX
PLASTIC PACKAGE
CASE 626

FIGURE 1 — LOGIC DIAGRAM

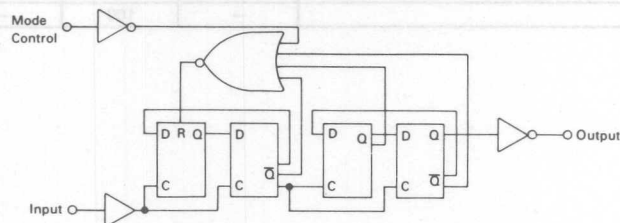
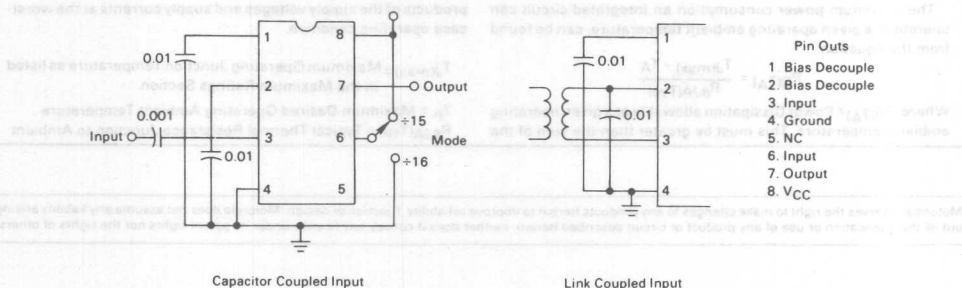


FIGURE 2 — TEST CIRCUITS



MC3393P

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	6.0	Vdc
Input Mode Control Voltage	V _{ICR}	10	Vdc
Junction Temperature	T _J	150	°C
Operating Temperature Range	T _A	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

PRELIMINARY ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = +5.0 Vdc, T_A = 25°C, f_{in} = 100 MHz)

Characteristics	Min	Typ	Max	Units
Power Supply Voltage	4.5	—	5.5	Vdc
Current Drain	—	40	—	mA
Input Voltage	100	—	400	mV(rms)
Input Impedance: Real Part	—	900	—	Ohms
Capacitance	—	6.0	—	pF
Mode Control Voltage for 15 Count	2.7	—	10	Vdc
Mode Control Voltage for 16 Count	0	—	0.8	Vdc
Output High at 30 μA Source	2.7	4.3	—	Vdc
Output Low at 1.6 mA Sink	—	0.3	0.8	Vdc
Propagation Delay Time	—	25	—	ns
Set up Time (16 to 15 Count) Measured before Rising Edge of Clock on Count 15	—	20	—	ns
Release Time (15 to 16 Count) Measured before Falling Edge of Clock Preceding Count 15	—	15	—	ns
Thermal Resistance, R _{θJC}	—	100	—	°C/W

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_D(T_A) = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)}$$

Where: P_D(T_A) = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the

products of the supply voltages and supply currents at the worst-case operating condition.

T_J(max) = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

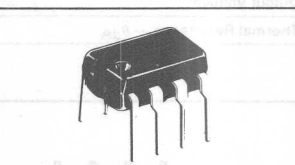
T_A = Maximum Desired Operating Ambient Temperature

R_{θJA}(Typ) = Typical Thermal Resistance Junction to Ambient

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**DIVIDE BY 20
PRESCALER**

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626

DIVIDE BY 20 PRESCALER

The MC3396P is a fixed $\div 20$ prescaler for use in frequency synthesizers and similar applications.

- 200 MHz (typ) Toggle Frequency
- Single 5.0 Volt Supply
- Buffered Clock Input
- 100 mV — 400 mV RMS Input Sensitivity
- Open Collector Saturating Output is Capable of Driving TTL and CMOS.

FIGURE 1 — LOGIC DIAGRAM

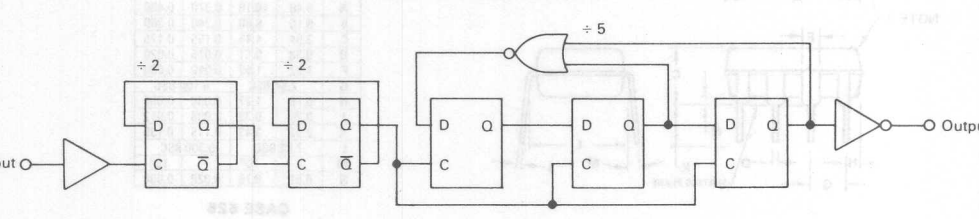
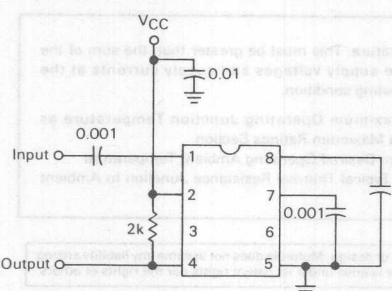


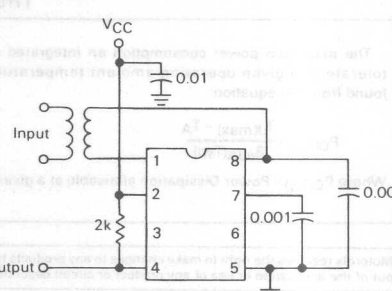
FIGURE 2 — CAPACITOR-COUPLED INPUT



PIN CONNECTIONS

1. Input
2. V_{CC}
3. NC
4. Output
5. Ground
6. NC
7. Bias Decouple
8. Bias Decouple

FIGURE 3 — LINK-COUPLED INPUT



This is advance information and specifications are subject to change without notice

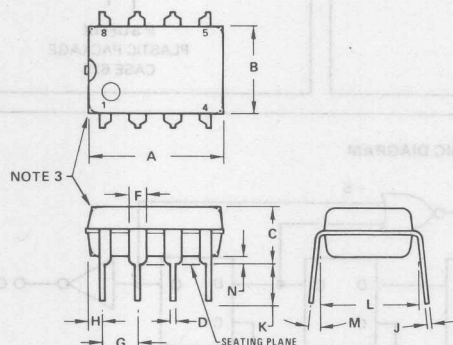
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted $V_{CC} = 5$ Vdc, $T_A = 25^\circ\text{C}$, $f_{in} = 125$ MHz measured in the circuit of Figure 2)

Characteristic	Min	Typ	Max	Unit
Operating Power Supply Voltage Range	4.5	—	5.5	Vdc
Current Drain	—	30	—	mA
Operating Input Voltage Range	100	—	400	mV(rms)
Input Impedance:				
Real Part	—	600	—	Ohms
Capacitance	—	6.0	—	pF
Output Voltage	3.0	4.5	—	V_{p-p}
Thermal Resistance — θ_{JA}	—	100	—	°C/W

OUTLINE DIMENSIONS



NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10 ⁰	—	10 ⁰
N	0.51	0.76	0.020	0.030

CASE 626

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_J(\max) - T_A}{R_{\theta JA}(\text{Typ})}$$

Where $P_{D(T_A)}$ = Power Dissipation allowable at a given operating

ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_J(\max)$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(\text{Type})$ = Typical Thermal Resistance Junction to Ambient

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MC6220

PRODUCT PREVIEW

MC6220 4-bit microcomputer unit (MCU) with PLL for frequency synthesis applications

The MC 6220 is a 4-bit single chip MCU with PLL hardware. The chip includes; a 24 hour clock, the processor, 32 x 4 bits of direct access RAM, 16 x 16 x 4 bits of indirect access RAM, 16 x 5 x 4 bits of indirect access ROM for constant, 1.2K 10-bit words of user ROM, 5 I/O lines, 5 output lines, 6 tri-state inputs, 2 special edge sensitive inputs and a serial I/O bus (clock and data I/O). In addition the PLL section contains a reference divider for 1kHz and 12.5kHz and a variable divider suitable for dual modulus applications. The device is housed in a 28 pin package.

MCU

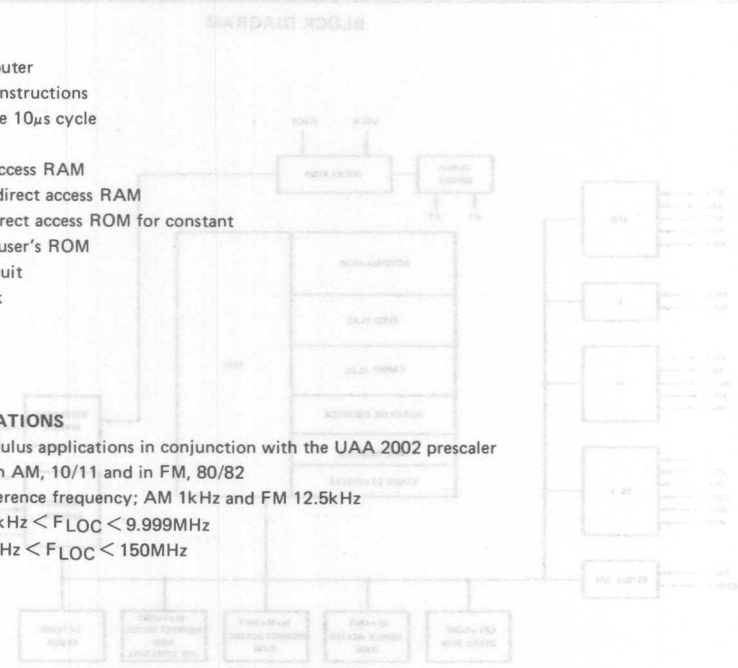
- 4-bit BCD microcomputer
- Instruction set of 16 instructions
- Each instruction is one 10 μ s cycle
- 2 level stack
- 32 x 4 bits of direct access RAM
- 16 x 16 x 4 bits of indirect access RAM
- 16 x 5 x 4 bits of indirect access ROM for constant
- 1.2K 10-bit words of user's ROM
- On-chip oscillator circuit
- Internal 24 hour clock

PLL FOR RADIO APPLICATIONS

- Suitable for dual modulus applications in conjunction with the UAA 2002 prescaler
- Dual modulus ratio; in AM, 10/11 and in FM, 80/82
- Phase comparator reference frequency; AM 1kHz and FM 12.5kHz
- AM tuning range 100kHz < F_{LOC} < 9.999MHz
- FM tuning range 40MHz < F_{LOC} < 150MHz

APPLICATIONS

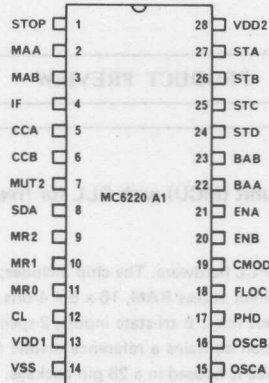
- Radio synthesizer for car and Hi-Fi
- Radio alarm
- Professional telecommunications systems
- Timer control



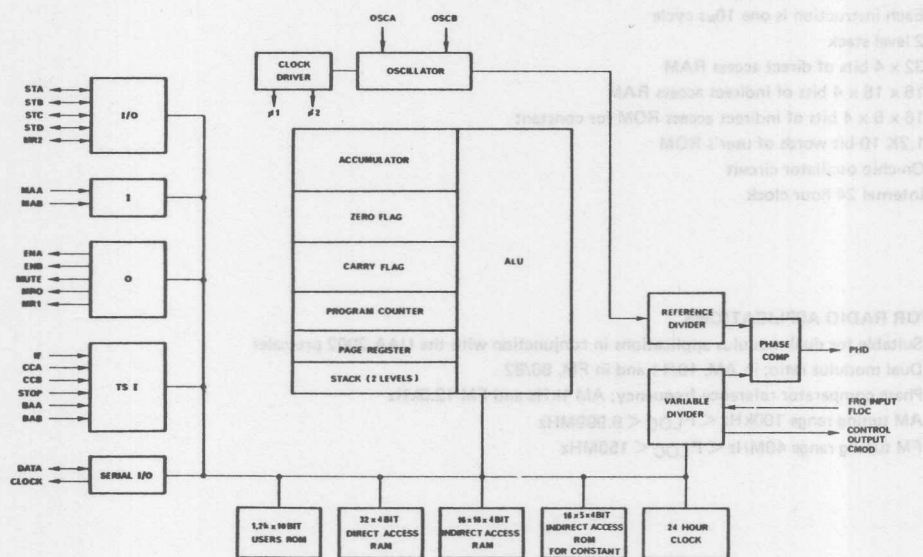
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MC6220

PIN ASSIGNMENT



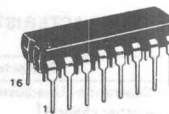
BLOCK DIAGRAM



TCA4500A

FM STEREO DEMODULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

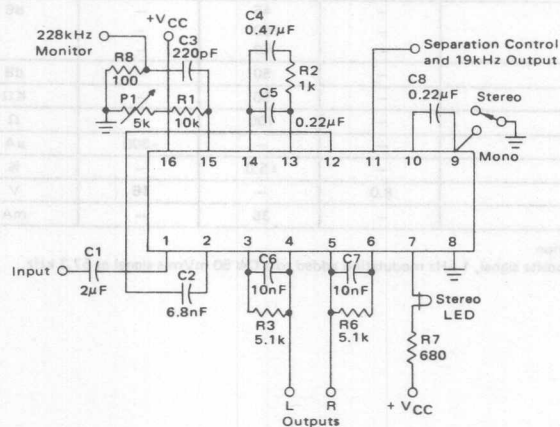


PLASTIC PACKAGE
CASE 648

FM STEREO DEMODULATOR DESIGNED FOR USE IN HI-FI STEREO RECEIVERS AND CAR RADIOS

- Wide Supply Range: 8 – 16 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range (Fixed or Adjustable)
- Variable Blend Control
- Low Distortion: 0.3% THD at 2.5 Vp-p Composite Input Signal
- Excellent Rejection of ARI Subcarrier (57 kHz)
- Excellent Rejection of Pilot Tone Harmonics including 114 kHz
- Wide Dynamic Range: 0.5 – 2.5 Vp-p Composite Input Signal
- Up to 6 dB Gain (Monaural)
- Low Output Impedance
- Transient-free Mono/Stereo Switching
- 50 dB Supply Ripple Rejection
- Integrated Stereo/Monaural Switch – 100 mA Lamp Driving Capability
- Requires No Inductors

FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT



PIN FUNCTIONS

- 1 – Input
- 2 – Pre-amplifier output
- 3 – Left amplifier input
- 4 – Left channel output
- 5 – Right channel output
- 6 – Right amplifier input
- 7 – Stereo indicator Lamp
- 8 – Ground
- 9 – Stereo switch filter
- 10 – Stereo switch filter
- 11 – 19 kHz output/blend
- 12 – Modulator input
- 13 – Loop filter
- 14 – Loop filter
- 15 – Oscillator RC network
- 16 – V_{CC}

TCA4500A

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Volts
Power Dissipation (Package limitation)	1800	mW
Derate above T _A = +25°C	15	mW/°C
Operating Temperature Range (Ambient)	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Lamp Drive Voltage (Max. voltage at pin 7 with lamp "off")	30	Volts
Lamp Current	100	mA
Blend Control Input Voltage (pin 11)	10	Volts

ELECTRICAL CHARACTERISTICS Unless otherwise noted: V_{CC} = +12 Vdc, T_A = 25°C, 2.5 Vp-p standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level, using circuit of Figure 1.

Characteristic	Min.	Typ.	Max.	Unit
Stereo Channel Separation: Unadjusted	30	—	—	dB
Optimised on other channel ¹	40	—	—	dB
Monaural Voltage Gain ¹	0.8	1.0	1.2	—
THD at 2.5 Vp-p Composite Input Signal	—	—	0.3	%
at 1.5 Vp-p Composite Input Signal	—	0.2	—	%
Signal/Noise Ratio	—	90	—	dB
RMS 20 Hz - 15 kHz	—	—	—	dB
Ultrasonic Frequency Rejection 19 kHz	—	31	—	dB
38 kHz	—	50	—	dB
Stereo Switch Level (19 kHz input level for lamp "on")	12	16	20	mVrms
Hysteresis	—	6.0	—	dB
Quiescent Output Voltage Change with Mono/Stereo Switching	—	5.0	20	mVdc
Stereo Blend Control Voltage (pin 11) 3 dB Separation	—	0.7	—	V
(see Fig. 2) 30 dB Separation	—	1.7	—	V
Minimum Separation (pin 11 at 0 V)	—	—	1.0	dB
Monaural Channel Imbalance (pilot tone off)	—	—	0.3	dB
ARI 57 kHz Pilot Tone Influence on THD ²	—	—	0.5	%
Sub-carrier Harmonic Rejection 76 kHz	—	45	—	dB
114 kHz	—	50	—	dB
152 kHz	—	50	—	dB
Supply Ripple Rejection	—	50	—	dB
Input Impedance	—	50	—	KΩ
Output Impedance	—	100	—	Ω
Blend Control Current ¹	—	—	-300	μA
Capture Range	—	±5.0	—	%
Operating Supply Voltage	8.0	—	16	V
Current Drain (lamp off)	—	35	—	mA

Notes: ¹ See Applications Information and Circuit Description

² ARI Test — Input signal: 1.5 Vp-p standard composite signal, 1 kHz modulation added to a CW 50 mVrms signal at 57.3 kHz.

TYPICAL CHARACTERISTICS

Unless otherwise noted $V_{CC} = +12\text{ V}$, $T_A = +25^\circ\text{C}$, Input Signal is Modulated L or R with 10% Pilot Level. (See Fig. 16.)

— : High Loop Gain Circuit
 - - - : Normal Circuit

FIGURE 2 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

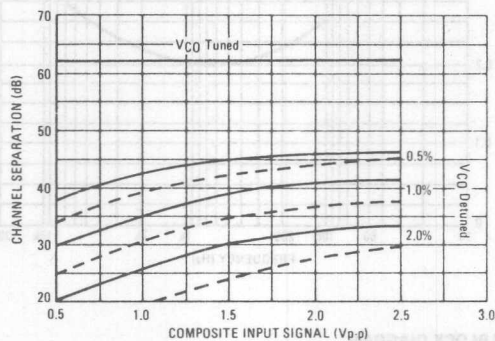


FIGURE 3 – V_{CO} FREE-RUNNING FREQUENCY versus TEMPERATURE

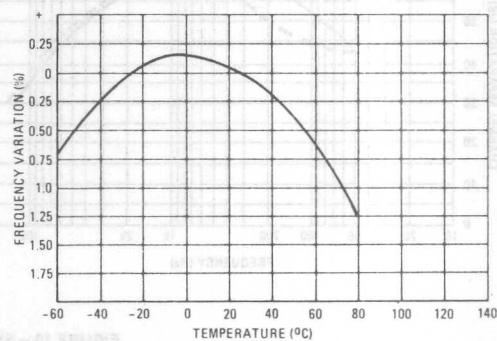


FIGURE 4 – STEREO SWITCH LEVEL versus V_{CO} FREE-RUNNING FREQUENCY

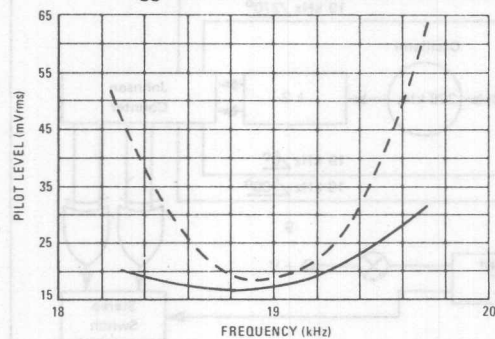


FIGURE 5 – SUPPLY RIPPLE REJECTION versus SUPPLY VOLTAGE

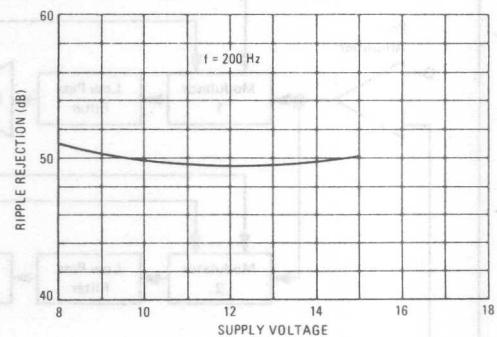


FIGURE 6 – THD versus COMPOSITE INPUT LEVEL

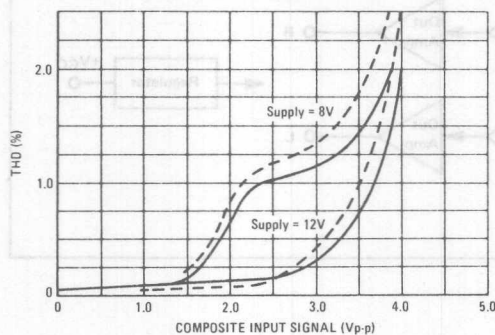


FIGURE 7 – CAPTURE and HOLDING RANGE WITH 20 mV PILOT LEVEL

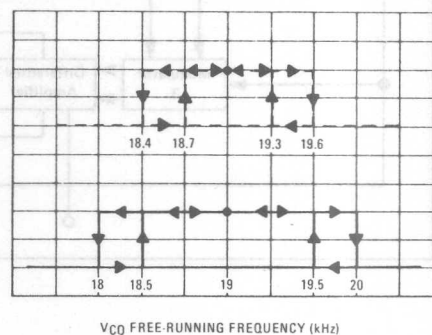


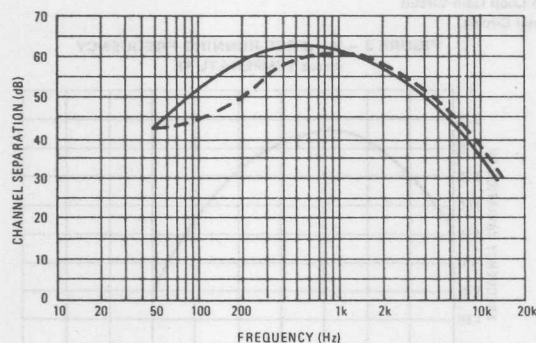
FIGURE 8 — CHANNEL SEPARATION
versus FREQUENCY

FIGURE 9 — THD versus FREQUENCY

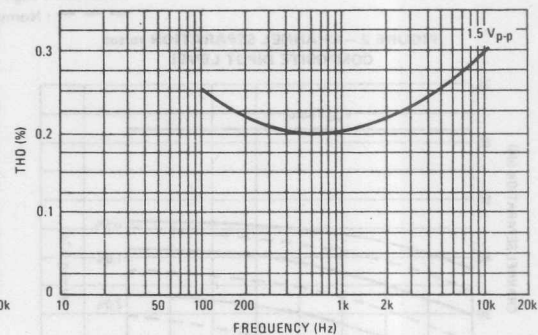
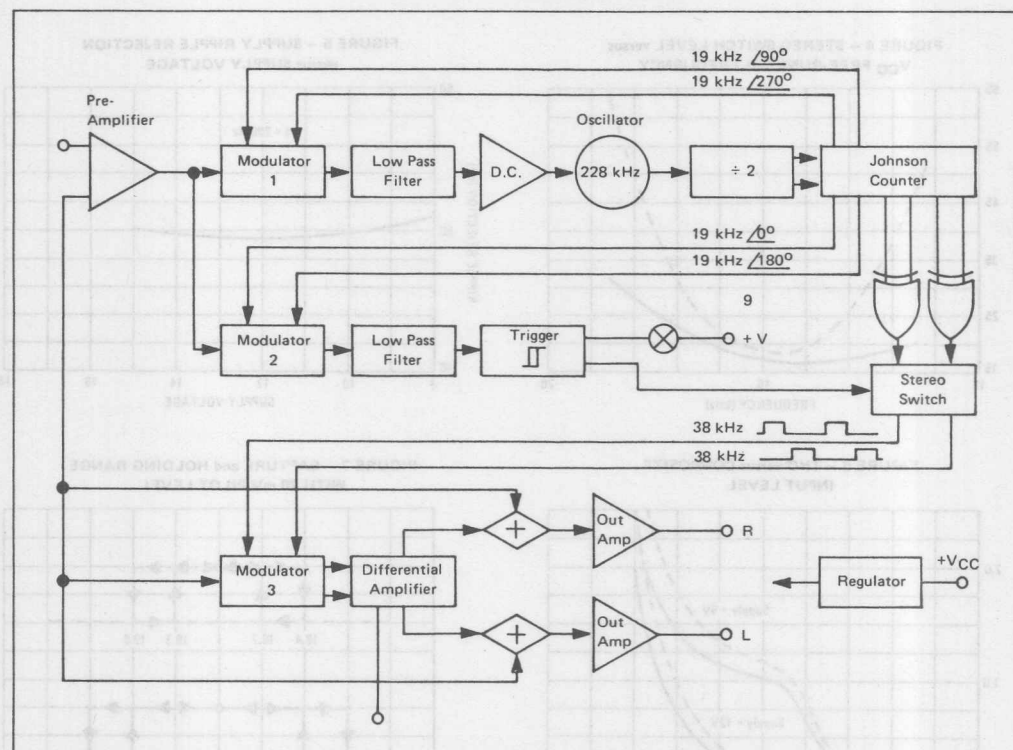


FIGURE 10 — SYSTEM BLOCK DIAGRAM



CIRCUIT DESCRIPTION

INTRODUCTION

The TCA4500A is a phase-lock-loop stereo decoder which incorporates a variable separation control, and in which sensitivity to the third harmonics of both the pilot and sub-carrier frequencies has been eliminated by the use of appropriate, digitally generated, waveforms in the phase-lock-loop and decoder sections.

The variable separation control may be operated manually, or by a receiver's AGC or S meter signals, to provide smooth transitions between monaural and stereo reception. It operates only during stereo reception: the circuit switches automatically to monaural if the 19 kHz pilot tone is absent.

The elimination of sensitivity to the third harmonic (114 kHz) of the sub-carrier (38 kHz) excludes interference from the 100 kHz (European Spacing) spaced side bands of adjacent transmitters, while elimination of sensitivity to the third harmonic (57 kHz) of the pilot tone (19 kHz) excludes interference from the ARI* system employed in Europe.

*Auto Radio Information.

CIRCUIT OPERATION

The block diagram of the circuit, shown in Fig. 10, consists of three sections: the phase-lock-loop, including the digital waveform generator; the stereo switch; and the decoder, in which the composite stereo signal is demodulated and matrixed to separate L and R channels.

In the phase-lock-loop the internal RC oscillator, operating at 228 kHz, feeds a 3 stage Johnson counter, via a binary divider, to generate a series of 19 kHz square waves. By the use of suitably connected NAND and EXCLUSIVE OR gates, the waveforms shown in Fig. 11, which are used to drive the various modulators in the circuit, are developed.

The use of such drive waveforms produces the modulating functions also shown in Fig. 11. The usual square-waveforms have been replaced in the PLL and decoder sections by 3-level forms which contain no third harmonic (actually no harmonics which are multiples of 2 or 3 are present). This eliminates the frequency translation of interference from these bands into the low frequency region. Such translation may produce audible components in the decoder section from the sidebands of adjacent channel FM signals, and may produce phase jitter, and consequent intermodulation distortion, in the PLL, from the modulated 57 kHz tones of the ARI system. The TCA 4500A is inherently free from these effects.

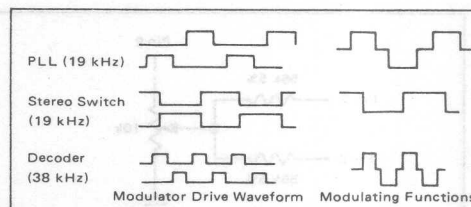
The stereo switch section is of conventional form (e.g. MC1310).

The decoder section consists of a modulator (driven by the waveforms shown in Fig. 11) whose outputs are the inverted and non-inverted channel difference signals. These signals pass to the output amplifiers via the variable

blend circuit in which they are partially combined, and hence mutually attenuated, according to the control voltage applied.

Matrixing occurs at the inputs of the output amplifiers, where the unmodified composite signal is added to the blended channel difference signals. The stereo separation may be progressively reduced from maximum to zero, dependent on the blending. The control law has been made non-linear, as the major redistribution of sound energy occurs at very low separation levels. For monaural, or very weak stereo signals, the modulator in the decoder section is deactivated by the stereo switch circuit. The variable separation control is thus, also, automatically disabled.

FIGURE 11 — DIGITAL WAVEFORM



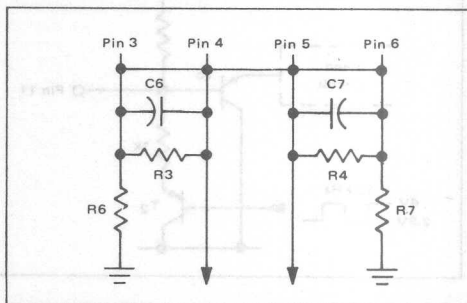
APPLICATION INFORMATION

GAIN AND DE-EMPHASIS

The gain and de-emphasis characteristics of the circuit are defined by shunt feedback via the external RC networks (R3, C6, R4, C7 of Fig. 1) around the output amplifiers. The gain is unity when resistors of 5.1 kΩ are used. Higher gains may be obtained by using networks of the form shown in Fig. 12.

The resistors R6, R7 are added to correct the output quiescent voltage levels which are optimized for R3, R4 = 5.1 kΩ and which would, if uncorrected, become too low with higher value resistors. Suitable network values are as follows:

FIGURE 12 — OUTPUT AMPLIFIER FEEDBACK NETWORKS



APPLICATION INFORMATION (continued)

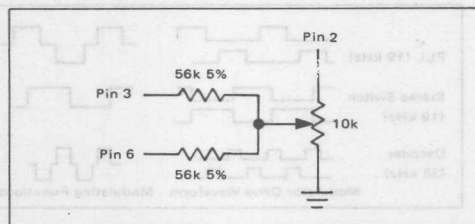
Gain (dB)	R3, R4	C6, C7		R6, R7
		50 μ s	75 μ s	
0	5.1k Ω	10 nF	15 nF	
3	6.8k Ω	6.8 nF	10 nF	47k \pm 10%
6	10k	4.7 nF	6.8 nF	27k \pm 10%

The maximum output level is 1 Vrms; consequently the max. input is limited to 1.4 Vp-p if the gain is set to 6 dB.

SEPARATION ADJUSTMENT

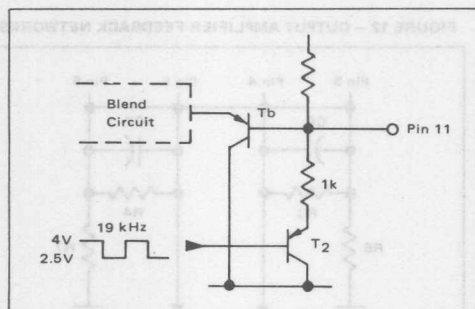
A separation adjustment may be added, as shown below, (Fig. 13), to compensate for the receiver's IF characteristics.

FIGURE 13 — NETWORK PROVIDING ADJUSTABLE SEPARATION



This network reduces the amplification of the channel sum signal in the decoder, to compensate the attenuation of the channel difference signal in the receiver's IF section. The network shown will compensate for up to 2 dB attenuation at 38 kHz. The decoder gain is, obviously, reduced by an amount equal to the compensation required. When used as described, the adjustment also corrects the inherent separation of the decoder, which may be optimized on one channel. Optimization of both channels is possible if separate potentiometers are used to feed each output amplifier.

FIGURE 14 — BLEND CONTROL INPUT CIRCUIT



VARIABLE SEPARATION (BLEND) CONTROL AND 19 kHz OUTPUT

To retain the 16-pin package, the blend control has been combined with the 19 kHz output on pin 11. The internal circuit providing this combination is shown in Fig. 14.

If pin 11 is left open-circuit, the 19 kHz signal appears at a mean dc level of 4 V. The blend circuit is inoperative at this level and the decoder provides full separation. The 19 kHz signal can be used to tune the internal oscillator.

To reduce the separation, the voltage on pin 11 is lowered. At 3.2 V, T2 ceases conduction and the 19 kHz signal disappears.

At 2.3 V, the blend circuit comes into operation and the separation decreases according to the curve shown in Fig. 15.

FIGURE 15 — SEPARATION CONTROL VOLTAGE

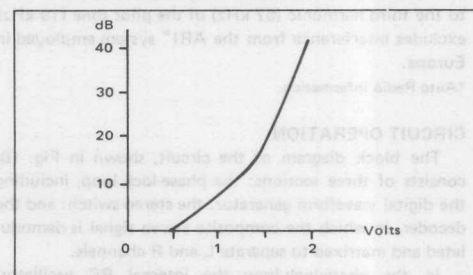
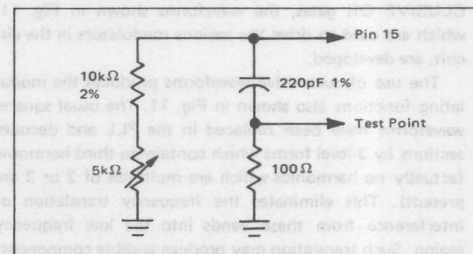


FIGURE 16 — OSCILLATOR NETWORK FOR DIRECT FREQUENCY MEASUREMENT



OSCILLATOR TUNING

If the variable separation facility is not required, pin 11 is left open-circuit and the 19 kHz signal which then appears may be used to indicate the oscillator frequency. If the variable separation is used, and the drive circuit prevents access to the 19 kHz signal, then the oscillator frequency must be measured directly. A test point should be obtained by modifying the oscillator RC network as shown in Fig. 16.

TCA4500A

The output is a pulse train of approximately 1.5 Volts amplitude. Connecting frequency counters of up to 300 pF input capacitance produces less than 0.3% change of the oscillator frequency, which should be set to 228 kHz.

HIGH LOOP GAIN COMPONENTS

For applications demanding operation under low pilot level (e.g., car radio) the following component changes to Fig. 1 are recommended.

R1 = 12k	C3 = 150 pF
R2 = 1.5k	C4 = 330 nF
R8 = 330	C5 = 150 nF
P1 = 10k	

EXTERNAL MONO-STEREO SWITCHING AND OSCILLATOR KILLING

If required, the TCA 4500A can be forced into mono mode simply by grounding pin 9 (see Fig. 1). The 228 kHz oscillator will be automatically killed.

The conditions governing Mono/Stereo switching on

pin 9 are the following:

- Quiescent voltage: +2.3 Vdc
- Current required to ensure mono operation (with 100 mVrms pilot level): 10 μ A (from pin 9 to ground)
- Hysteresis: 0.7 μ A
- Stereo/mono switching and oscillator killing: less than +500 mV
- Maximum stray capacitance between pin 9 and ground: 100 pF

EXTERNAL COMPONENT FUNCTIONS

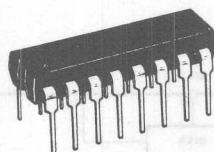
- P1 — 19 kHz frequency adjustment
- P2 — channel separation adjustment and compensation for IF roll-off.
- R3, R6 — gain fixing resistors. The values shown in the schematic are for unity gain.
- C6, C7 — de-emphasis capacitors. Value to give: RC = 50 μ s.

Values shown in Fig. 1 are recommended for applications with input level higher than 1.0 Vrms.

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

OUTLINE DIMENSIONS

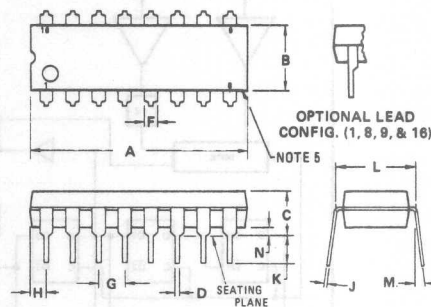


PLASTIC PACKAGE
CASE 648

DIM	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
- ROUNDED CORNERS OPTIONAL.



UAA2002

ADVANCE INFORMATION

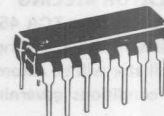
FREQUENCY SYNTHESIZER PRESCALER

The UAA2002 is a frequency synthesizer prescaler designed to be used in conjunction with the MC6220 (Microprocessor Phase Locked Loop system) and the UAA2003 (Interface circuit) in radio applications. The circuit contains AM and FM preamplifiers and a switchable dual-modulus divider. The circuit, realised in EFL technology, interfaces between the receiver's local oscillators and the MC6220 NMOS controller.

- Divide by 80/82 operation to 120MHz (FM band)
- Divide by 10/11 operation to 20MHz (AM bands)
- High input sensitivity (50mV)
- Wide temperature range; -25 to $+70^{\circ}\text{C}$

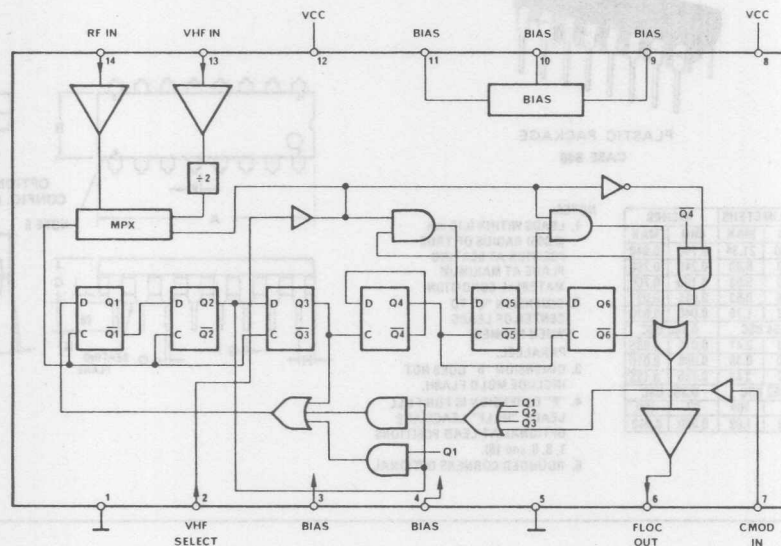
FREQUENCY SYNTHESIZER PRESCALER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646 (TO 116)

FIGURE 1 - UAA2002 BLOCK DIAGRAM AND PINOUT



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$) All voltages are referenced to ground
(pins 1 & 5)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	8, 12	V_{CC}	7.0	V
Signal Input Voltage	13, 14	V_{in}	2000	mV RMS
Digital Input Voltage	2, 7	V_{CMOD} V_{SVHF}	V_{CC}	V
Output Pin Loading	6	R_{FLOC}	>500	Ω
Bias Pin Loading	3, 4, 9, 10, 11	R_{BIAS}	>500	Ω
Storage Temperature Range		T_{STG}	-55 to $+150$	$^\circ\text{C}$
Operating Temperature Range		T_A	-25 to $+70$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

Characteristic	Pin	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	8, 12	V_{CC}		5.6	6.0	6.4	V
Power Supply Current	8, 12	I_{CC}			69	90	mA
Input Signals	13, 14	V_{RF}	$f_{max} < 20\text{MHz}$	50		500	mV
		I_{RF}		100			μA
		V_{VHF}	$f_{max} < 120\text{MHz}$	50		500	mV
		I_{VHF}		100			μA
Logic Input Levels	7, 2	V_{IL}		0		1.5	V
Input Voltage Low		V_{IH}		4.0		V_{CC}	V
Input Current Low		I_{IL}	$V_{IL} = 0$			300	μA
Input Current High (pin 2)		I_{IH2}	$V_{IH} = V_{CC}$			1.5	mA
Input Current High (pin 7)		I_{IH7}	$V_{IH} = V_{CC}$			300	μA
Output Logic Levels	6	V_{OL}		0		0.4	V
Low		V_{OH}		4.0		V_{CC}	V
High		I_{out}	$V_{OH} = V_{CC}$			6	mA

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Lead and Lag Times (relative to Falling Edge of FLOC)	7	t_{lead}	100			ns
		t_{lag}	0			ns

INPUT/OUTPUT FUNCTIONS

VCC SUPPLY — (pins 8 & 12) These pins should be connected in parallel and provide power for the entire circuit.

BIAS PINS — (pins 3, 4, 9, 10 & 11) These pins permit external decoupling of the internally generated reference bias voltages. Capacitors (low-inductance ceramic disc for high frequency operation) should be 1nF. They remove noise from the critical bias points. Although the circuit will operate without these capacitors the maximum frequency range will be reduced.

FLOC OUTPUT — (pin 6) The output appearing on this pin is suitable for direct connection to the NMOS MC6220 controller. For optimum waveform this pin should be loaded with less than 30pF capacitance to earth. Resistive loading should be greater than 1k Ω .

CMOD INPUT — (pin 7) A logical '1' from the MC6220 controller applied to this pin switches the division ratio from 82 to 80 or 11 to 10 depending on the mode selected (at pin SVHF). The switching threshold is approx.

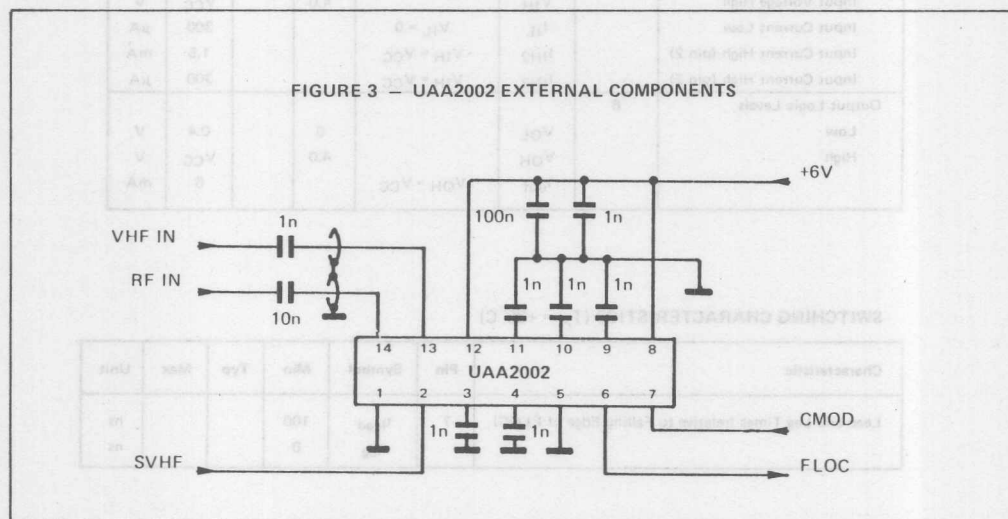
3.2V. It can be switched by NMOS, CMOS or TTL logic levels. Input current is less than 30 μ A in the high state and 2 μ A when low. The high voltage must not exceed VCC.

SVHF INPUT — (pin 2) A logical '1' from the UAA2003 interface circuit applied to this pin selects the VHF mode operation, i.e. the circuit divides by 80/82 (dependant on the condition of CMOD) and enables the VHF input amplifier and divide-by 2 prescaler. The switching voltage is as for the CMOD input. However, the input current requirement is higher, when high ($V_{in} = V_{CC}$) the pin draws less than 900 μ A.

VHF INPUT — (pin 13) A low level input from the receiver local oscillator (VHF FM band) is applied to this pin. The level window for correct operation is between 50mV and 500mV RMS.

RF INPUT — (pin 14) This pin is identical to the VHF input except the low frequency oscillator signal (AM bands) is applied — $f_{max} < 20$ MHz.

FIGURE 3 — UAA2002 EXTERNAL COMPONENTS



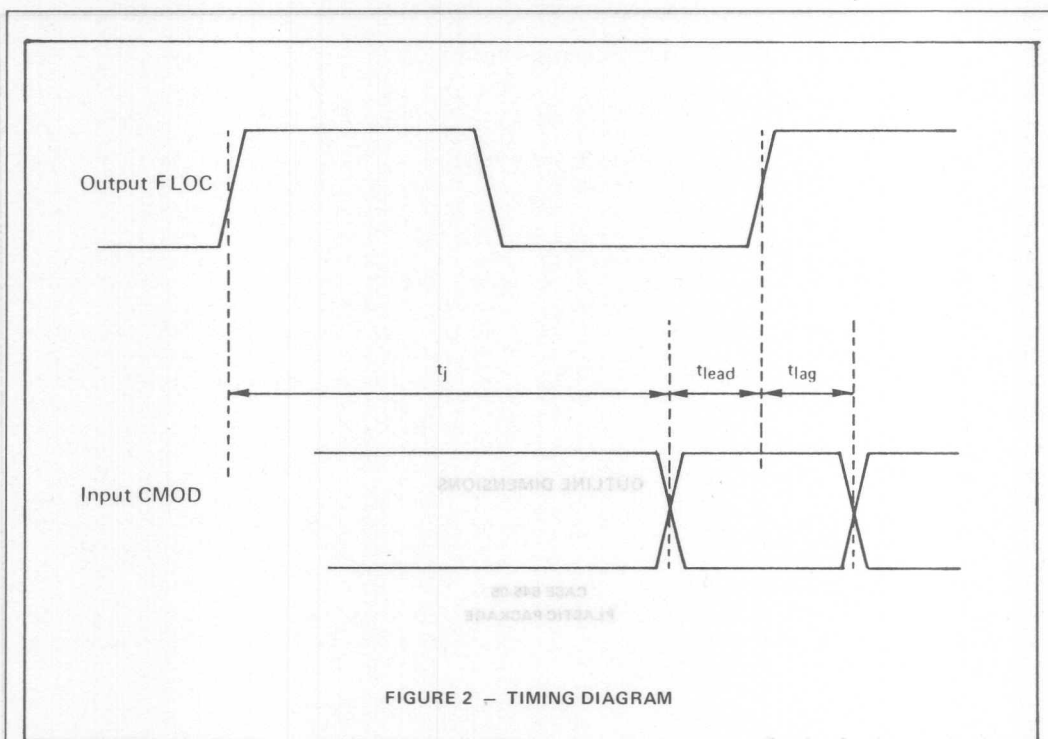


FIGURE 2 — TIMING DIAGRAM

CIRCUIT OPERATION

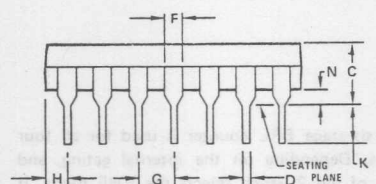
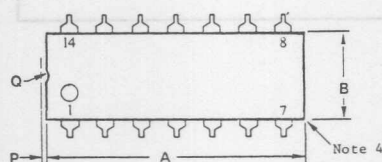
The circuit operation can be followed by reference to the block diagram (Figure 1). A low level RF sine wave input, from the receiver's 'AM' local oscillator, fed to pin 14 is amplified, limited and converted to an EFL logic level by the internal RF amplifier. Similarly, signals arriving at pin 13, from the receiver's 'VHF' or 'FM' local oscillator, are amplified, limited and divided-by-two. Both amplified signals are fed to a multiplexer, which is controlled by a logic voltage on pin 2 (SVHF). When pin 2 is at a logical '1' the VHF input to the multiplexer is enabled; conversely, when pin 2 is at logical '0' the multiplexer's RF input is enabled. The selected output is then fed to the main counter for division.

The main six-stage EFL counter is used for all four division ratios. Depending on the internal gating, and the condition of pin 2 which selects the VHF mode, it will divide by 10/11 (RF mode) or 40/41 (VHF mode). In the 40/41 mode overall division ratios of 80/82 result since the fixed divide-by-two prescaler is in circuit.

The application of a logical '1' or 'high' voltage on pin 7 (CMOD) locks the counter to divide-by 40 (VHF mode) or divide-by 10 (RF mode). Similarly, a logical '0' on pin 7 will result in divide-by 41 (VHF) or divide-by 11 (RF).

In order to ensure the desired division ratio the modulus change voltage must be applied at least ' t_{lead} ' (see the switching characteristics) before the next falling edge.

OUTLINE DIMENSIONS

CASE 646-05
PLASTIC PACKAGE

NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.
5. 646-04 OBSOLETE, NEW STD 646-05.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	8.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
E	1.02	1.78	0.040	0.070
F	2.54	BSC	0.100	BSC
G	1.32	2.41	0.052	0.095
H	0.20	0.38	0.008	0.015
J	2.92	3.43	0.115	0.135
K	7.62	BSC	0.300	BSC
L	0°	10°	0°	10°
M	0.51	1.02	0.020	0.040
N				

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

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UAA 2003

Advance Information

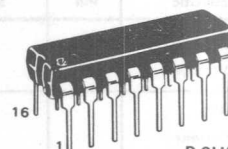
PLL INTERFACE IC

The UAA2003 is designed to be used in conjunction with the MC 6220 (Microprocessor - PLL System) and the UAA2002 (Twin Dual Modulous Counter) in Radio Frequency Synthesizers. It is realised in I^2L /Linear technology and interfaces the Microprocessor to the Radio Receiver. The circuit contains a Serial Data to Parallel Band Driver shift register. A stop signal detector and a low input current Operational Amplifier.

- 5 Bit Parallel Output Data (10mA current source capability)
- Sensitive 2 Threshold ($\pm 90mV$) Detector
- Very Low OP AMP Input Current (0.5nA typical)
- Wide Temperature Range ($-25^\circ C$ to $+75^\circ C$)

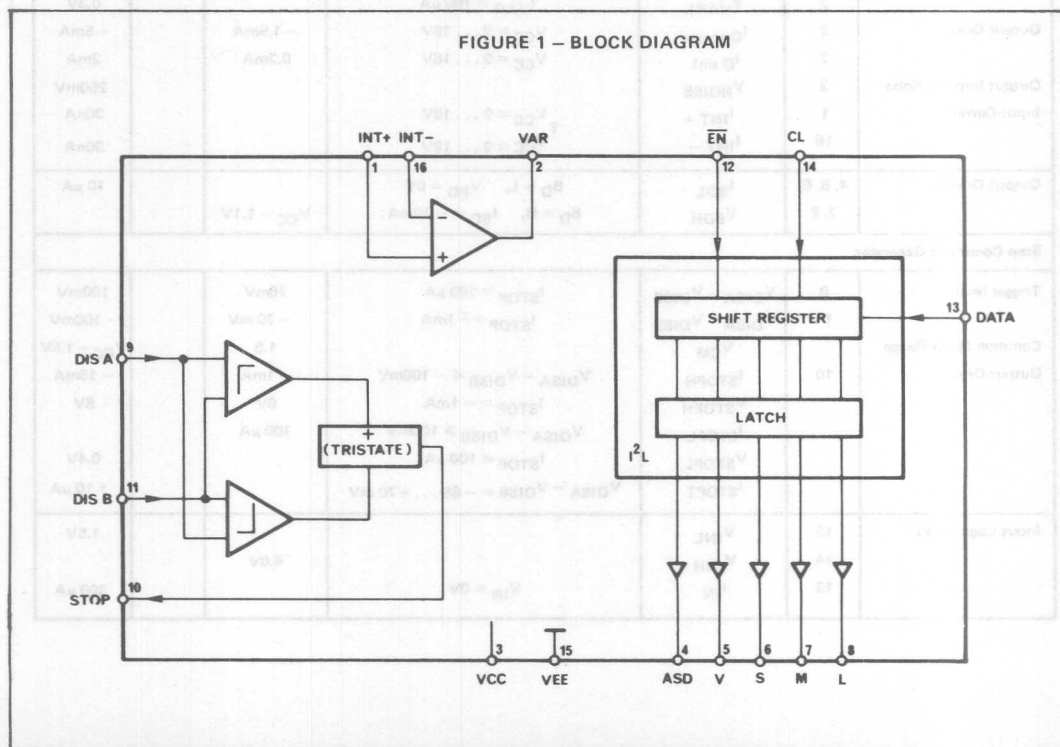
PLL INTERFACE IC

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 - BLOCK DIAGRAM



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	20	Vdc
Maximum band driver output current	I_{CC}	20	mAdc
Operating temperature range	T_A	-25 to +70	$^\circ\text{C}$
Storage temperature range	T_{STC}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 12\text{V}$, $T_A = 25^\circ\text{C}$)

Characteristic	Pin	Symbol	Condition	Min	Typ	Max
Power Supply Operating Voltage	3	V_{CC}	—	9V		18V
Power Supply Operating Current		I_{CC}	$V_{CC} = 9\text{V}$ $I_{BD} = 0$ $V_{CC} = 18\text{V}$ $I_{BD} = 0$		6.5mA 13mA	10mA 20mA
OP-AMP						
Output Swing	2	V_{VARH}	$I_{VAR} = -100\mu\text{A}$	$V_{CC} - 1.1\text{V}$		
	2	V_{VARL}	$I_{VAR} = 100\mu\text{A}$			0.3V
Output Drive	2	$I_{O\text{ source}}$	$V_{CC} = 9 \dots 18\text{V}$	-1.5mA		-5mA
	2	$I_{O\text{ sink}}$	$V_{CC} = 9 \dots 18\text{V}$	0.2mA		2mA
Output Impulse Noise	2	V_{NOISE}				250mV
Input Current	1	I_{INT+}	$V_{CC} = 9 \dots 18\text{V}$			30nA
	16	I_{INT-}	$V_{CC} = 9 \dots 18\text{V}$			30nA
Output Drivers	4, 5, 6, 7, 8	I_{BDL} V_{BDH}	$B_D = L$, $V_{BD} = 0\text{V}$ $B_D = H$, $I_{BD} = -10\text{mA}$	$V_{CC} - 1.1\text{V}$		10 μA
Stop Command Generator						
Trigger level	9	$V_{DISA} - V_{DISB}$	$I_{STOP} = 100\mu\text{A}$	75mV		100mV
	11	$V_{DISA} - V_{DISB}$	$I_{STOP} = \pm 1\text{mA}$	-70mV		-100mV
Common Mode Range		V_{CM}		1.5		$V_{CC} - 1.5\text{V}$
Output Drive	10	I_{STOPH}	$V_{DISA} - V_{DISB} \leq -100\text{mV}$	-1mA		-15mA
		V_{STOPH}	$I_{STOP} = -1\text{mA}$	6V		8V
		I_{STOPL}	$V_{DISA} - V_{DISB} \geq 100\text{mV}$	100 μA		
		V_{STOPL}	$I_{STOP} = 100\mu\text{A}$			0.4V
		I_{STOPT}	$V_{DISA} - V_{DISB} = -65 \dots +70\text{mV}$			$\pm 10\mu\text{A}$
Input Logic levels	13	V_{INL}		4.0V		1.5V
	14	V_{INH}				
	12	I_{IN}	$V_{IN} = 0\text{V}$			300 μA

CIRCUIT OPERATION

With reference to the block diagram (figure 1), the circuit contains a low input current, wide output swing operational amplifier. This is specifically designed for low input bias current (typically 500pA) and is intended for use as the active integrator in the PLL.

A 5-output Serial/Parallel data converter is included. This takes serial data from the MC6220 and outputs the desired band of operation and also, if automatic search is in progress, up to 10mA per output may be drawn from these pins.

Also included is a Dual threshold detector. This has high input impedance differential inputs. The conditions :

$$DISA > DISB + 90mV;$$

$$DISB + 90mV > DISA > DISB - 90mV;$$

$$DISA < DISB - 90mV;$$

are detected and made available on pin STOP in tristate form (low, hi-z, high).

INPUT/OUTPUT FUNCTIONS

V_{CC} SUPPLY - (pin 3) This pin supplies power for the entire circuit (I_L included).

INT - (pins 1 & 16) These are the differential inputs of the Operational Amplifier. Pin 1 is the positive input, pin 16 the negative. More than 7V is not allowed differentially between these pins.

VAR - (pin 2) This is the output of the Operational Amplifier. It is short circuit protected to V_{CC} and earth.

DISA - (pin 9), **DISB** - (pin 11) These pins are the differential inputs of the threshold detector (STOP command generator). As with the OP-AMP more than 7V differential will damage the circuit.

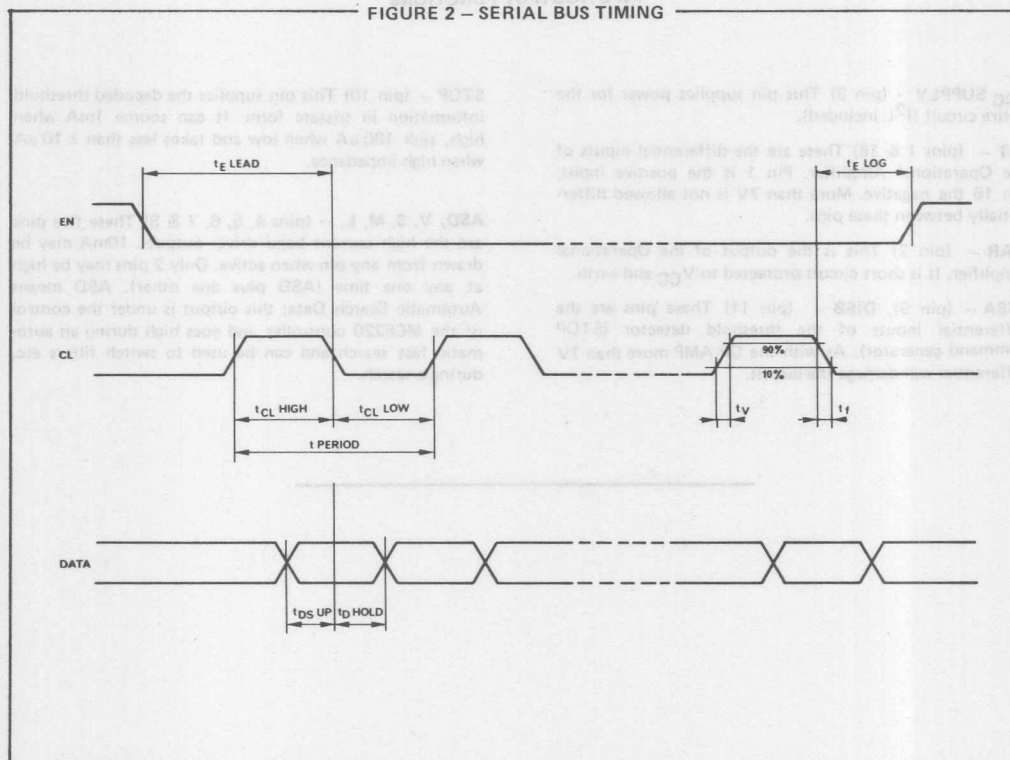
STOP - (pin 10) This pin supplies the decoded threshold information in tristate form. It can source 1mA when high, sink 100 μ A when low and takes less than $\pm 10 \mu$ A when high impedance.

ASD, V, S, M, L - (pins 4, 5, 6, 7 & 8) These five pins are the high current band driver outputs. 10mA may be drawn from any pin when active. Only 2 pins may be high at any one time (ASD plus one other). ASD means Automatic Search Data; this output is under the control of the MC6220 controller and goes high during an automatic fast search and can be used to switch filters etc. during a search.

SWITCHING CHARACTERISTICS ($V_{CC} = 12 \pm 10\%$, $T_A = 0$ to 70°C)

Rating	Symbol	Min	Typ	Max
Clock High Time	$t_{CL\text{high}}$	1 μs		
Clock Low Time	$t_{CL\text{low}}$	4 μs		
Clock Period	t_{CLp}	7 μs		
Clock Rise Time	t_{CLr}			2 μs
Clock Fall Time	t_{CLf}			2 μs
Data Set-Up Time	t_{DSup}	500 ns		
Data Hold Time	t_{Dhold}	4 μs		
Enable Lead Time	t_{Elead}	4 μs		
Enable Lag Time	t_{Elag}	4 μs		

FIGURE 2 - SERIAL BUS TIMING



μA758A

Advance Information

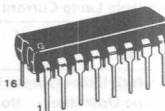
PHASE LOCK LOOP FM STEREO DEMODULATOR

The μA758A is an improved FM stereo multiplex decoder with an extended operating supply voltage range.
It is a direct replacement for the μA758 and LM1800.

- Requires No Inductors
- Low External Part Count
- Excellent Channel Separation Without Adjustment
- Only Single Potentiometer Oscillator Frequency Adjustment Necessary
- 100 mA Lamp or LED Driving Capability With Current Limiting
- Automatic, Transient-Free Stereo/Mono Switching
- Wide Supply Range: 8–16 Vdc
- Excellent SCA Rejection
- 50 dB Power Supply Rejection
- Low Impedance, Buffered Output

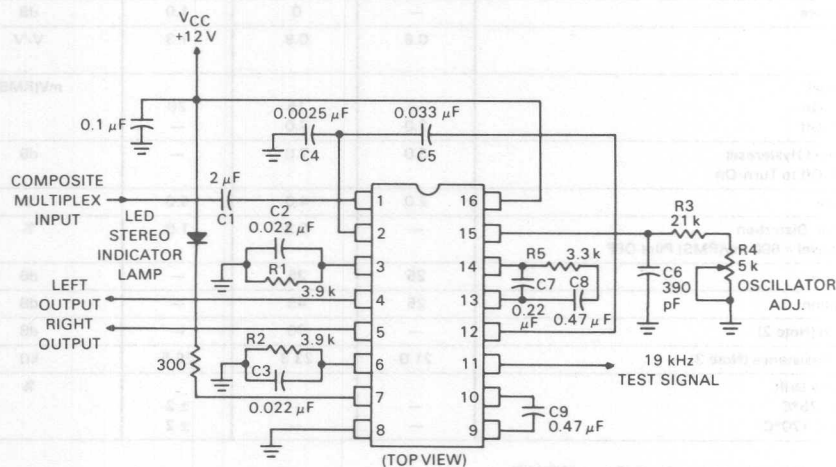
PHASE LOCK LOOP FM STEREO DEMODULATOR

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



**P SUFFIX
PLASTIC PACKAGE
CASE 648C**

FIGURE 1 — TYPICAL APPLICATION AND TEST CIRCUIT



NOTES:

- C4 may be removed for most applications
- C6 Tolerance = $\pm 1\%$ in test circuit and $\pm 5\%$ in typical applications
- R3 Tolerance = $\pm 1\%$
- R4 Tolerance = $\pm 10\%$
- R1 and R2 Tolerances = $\pm 1\%$ in test circuit and $\pm 5\%$ in typical application

This is advance information and specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage	18	Vdc
Supply Voltage (≤ 15 Seconds)	22	Vdc
Voltage at Lamp Driver Terminal (Lamp OFF)	22	Vdc
Junction Temperature	150	°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Operating Voltage Range	8-16	Vdc

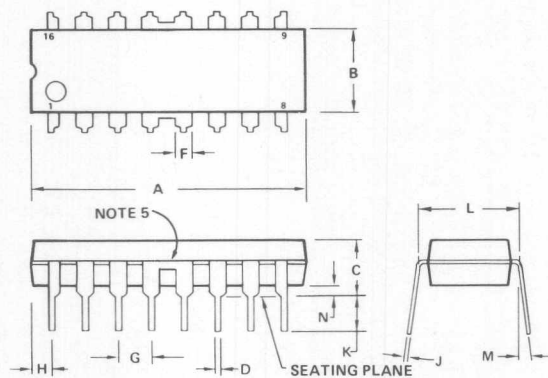
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = +12\text{ Vdc}$, 19 kHz pilot level = 30 mV(RMS), Multiplex Signal (L = R, pilot OFF) = 300 mV(RMS), Modulation Frequency = 400 Hz or 1 kHz, Test Circuit 1, unless otherwise specified)

Characteristic	Min	Typ	Max	Unit
Current Drain Lamp OFF	—	21	35	mAdc
Maximum Available Lamp Current	100	150	—	mAdc
Voltage @ Lamp Driver Terminal $I_{\text{Lamp}} = 50\text{ mA}$	—	1.0	1.8	Vdc
DC Voltage Shift @ Either Output Terminal Stereo to Mono Operation — No Lamp	—	2.0	100	mVdc
Power Supply Ripple Rejection 200 Hz, 200 mV(RMS)	35	50	—	dB
Input Resistance	20	35	—	k Ω
Output Resistance	0.9	1.3	1.7	k Ω
Channel Separation 100 Hz 400 Hz 10 kHz	— 30 —	40 45 45	— — —	dB
Channel Balance	—	0	1.0	dB
Voltage Gain 1 kHz	0.6	0.9	1.3	V/V
Pilot Input Level Lamp Turn-On Lamp Turn-Off	— 2.0	15 7.0	20 —	mV(RMS)
Pilot Input Level Hysteresis Lamp Turn-Off to Turn-On	3.0	7.0	—	dB
Capture Range	2.0	4.0	6.0	%
Total Harmonic Distortion Multiplex Level = 600 mV(RMS) Pilot OFF	—	0.2	1.0	%
9 kHz Rejection	25	35	—	dB
38 kHz Rejection	25	45	—	dB
SCA Rejection (Note 2)	—	70	—	dB
VCO Tuning Resistance (Note 3)	21.0	23.3	25.5	k Ω
VCO Frequency Drift $0^\circ\text{C} \leq T_A \leq 25^\circ\text{C}$ $25^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	— —	— —	± 2 ± 2	%

NOTES:

1. Rating applied for ambient temperatures. $R_{\theta JA} = 100^\circ\text{C/W}$
2. Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
3. Total resistance from pin 15 to ground, in test circuit 1, required to set reference frequency at pin 11 to 19 kHz $\pm 10\text{ Hz}$.

OUTLINE DIMENSIONS



NOTES:

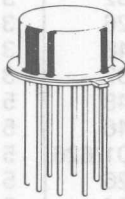
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. EXTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13 AS SHOWN.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

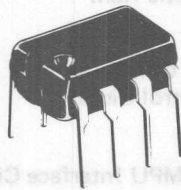
CASE 648C

SECTION 5 APPLIANCE INTEGRATED CIRCUITS

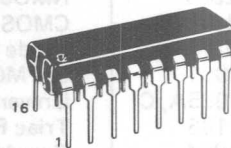
Section 5—Packages



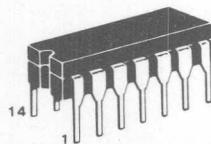
CASE 601 (TO99)



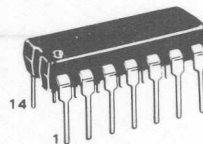
CASE 626



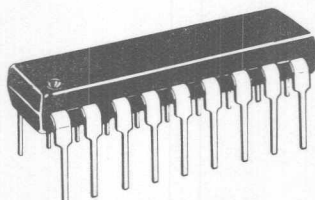
CASE 648



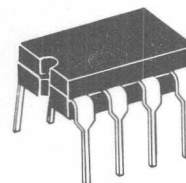
CASE 632 (TO116)



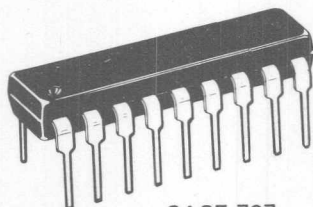
CASE 646 (TO116)



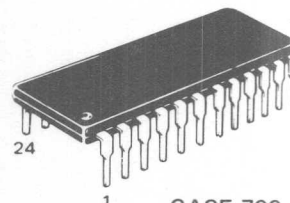
CASE 701



CASE 693



CASE 707



CASE 709

APPLIANCE INTEGRATED CIRCUITS

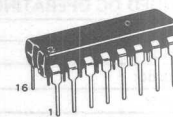
Device	Designation	Package	Page
MC3490	7-Digit Gas Discharge Display Driver	648	2 - 83
MC3491	8-Segment Visual Display Driver	701	2 - 89
MC3492	8-Segment Visual Display Driver	701	2 - 89
MC3494	7-Digit Gas Discharge Display Driver	648	2 - 83
MC14466	Low Cost Smoke Detector	648	5 - 3
MC144100	CMOS Duplex Mode 32-Segment LED Driver	709	3 - 67
MC144115	CMOS 2-Digit/16-Segment LCD Driver	709	3 - 80
MCM2801	NMOS 16x16 Electrically Erasable PROM	632	3 - 86
MCM144102	CMOS 16x16-Word Static Ram	626	3 - 98
SAA1006	Diode Matrix Encoder	648	3 - 103
SMA2001	See MCM2801	632	3 - 86
TDA1085A, C	Universal Motor Speed Controller	648	5 - 8
TDA1185	Triac Firing Angle Control Circuit	646	5 - 15
UAA1004	Zero Voltage Switch	601/626	5 - 19
UAA1016A, B	Zero Voltage Switch	626	5 - 23
UAA2022	16-Bit LED Driver/ or MPU Interface Circuit	724	3 - 182

MC14466

CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

LOW-COST SMOKE DETECTOR



P SUFFIX
PLASTIC PACKAGE
CASE 648B

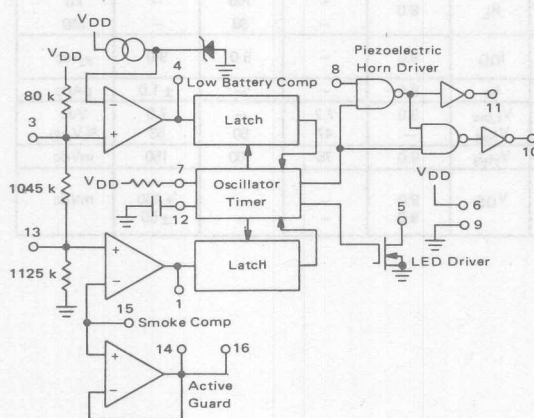
NOTE: Pins 15 and 16 are connected via a metal shorting bar. See package details in data sheet.

LOW-COST SMOKE DETECTOR

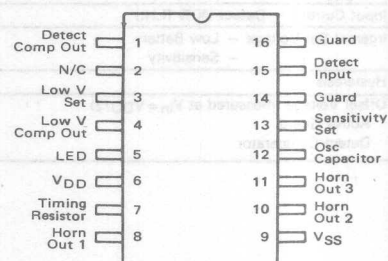
The MC14466 together with an ionization chamber will detect smoke using a minimum of external components. When smoke is sensed, an alarm is sounded via an external piezoelectric transducer and internal drivers. This circuit is designed to comply with the U.L. 217 specification.

- Ionization Type with On-Chip FET
- Piezoelectric Horn Driver
- Guard Outputs on Both Sides of Detect Input
- Low Battery Trip Point Internally Set Can Be Altered Via External Resistor
- Detect Threshold Internally Set Can Be Altered Via External Resistor
- Pulse Testing for Low Battery Uses LED for Battery Loading
- Comparator Outputs for Detect and Low Battery
- Internal Reverse Battery Protection

FIGURE 1 — BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +15	Vdc
Input Voltage, All Inputs	V_{in}	-0.25 to $V_{DD} + 0.25$	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	30	mAdc
Operating Temperature Range	T_A	0 to +50	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Reverse Battery Time	t_{RB}	5.0	s

RECOMMENDED DC OPERATING CONDITIONS (Voltage referenced to V_{SS})

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	9.0	Vdc
Timing Capacitor	—	0.1	μF
Timing Resistor	—	8.2	M Ω
Battery Load (Resistor or LED)	—	10	mAdc

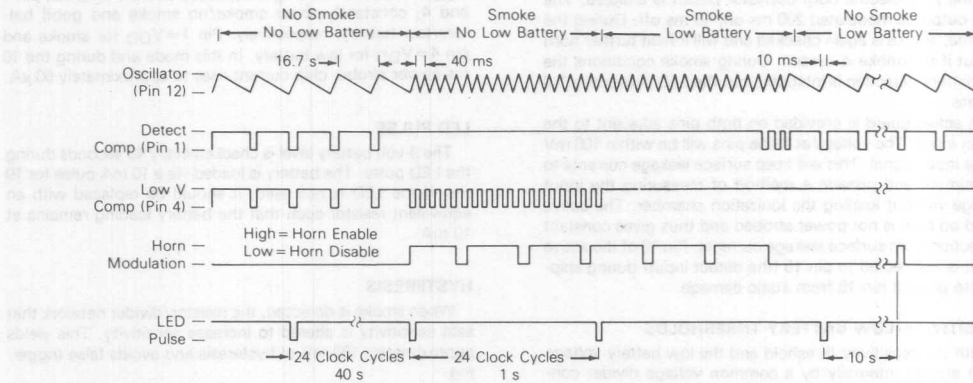
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	—	6.0	—	10	Vdc
Output Voltage						
Piezoelectric Horn Drivers ($I_{OH} = 16 \text{ mA}$)	V_{OH}	7.4	6.5	—	—	
Comparators ($I_{OH} = 30 \mu A$)		9.0	8.5	8.8	—	
Piezoelectric Horn Drivers ($I_{OL} = -16 \text{ mA}$)	V_{OL}	7.4	—	—	0.9	
Comparators ($I_{OL} = -30 \mu A$)		9.0	—	0.1	0.5	
Output Current — LED Driver ($V_{OL} = 3.0 \text{ Vdc}$)	I_{OL}	7.4	10	—	—	mAdc
Active Guard Drive	R_L	9.0	—	100	—	k Ω
Capability						
	R_L to V_{SS}		—	30	—	M Ω
Operating Current ($R_{Bias} = 8.2 \text{ M}\Omega$)	I_{DD}	9.0	—	5.0	9.0	μA_{dc}
Input Current — Detect (40% R.H.)	I_{in}	9.0	—	—	± 1.0	pAdc
Internal Set Voltage — Low Battery	V_{Low}	9.0	7.2	—	7.8	Vdc
— Sensitivity	V_{Set}	—	47	50	53	% V_{DD}
Hysteresis	V_{Hys}	9.0	75	100	150	mVdc
Offset Voltage (measured at $V_{in} = V_{DD}/2$)						
Active Guard	V_{OS}	9.0	—	—	± 100	mVdc
Detect Comparator		9.0	—	—	± 50	

TIMING PARAMETERS (C = 0.1 μ F, R_{Bias} = 8.2 M Ω , V_{DD} = 9.0 Vdc, T_A = 25°C)

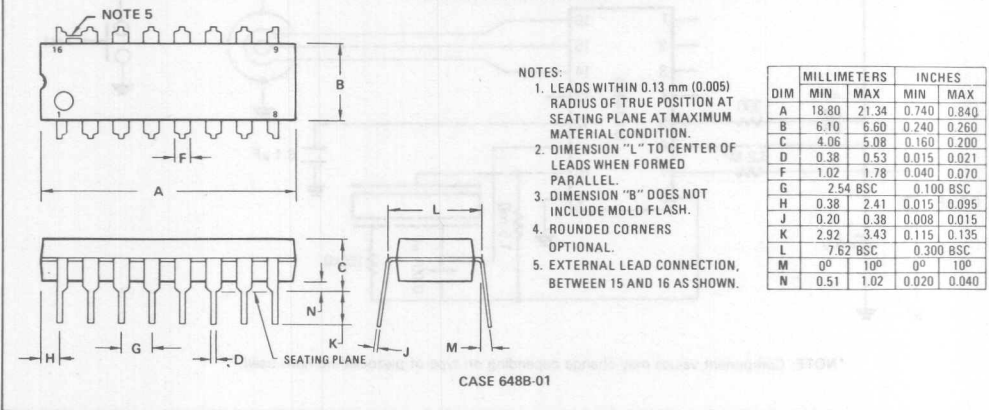
Characteristics		Symbol	Min	Typ	Max	Units
Oscillator Period	No Smoke	t _{Cl}	1.34	1.67	2.0	s
	Smoke		32	40	48	ms
Oscillator Pulse Width		PW _{Cl}	8	10	12	ms
Horn Output (During Smoke)	On Time	PW _{on}	—	200	—	ms
	Off Time	PW _{off}	—	40	—	ms
LED Output	Between Pulses	t _{LED}	32	40	48	s
	On Time	PW _{on}	8	10	12	ms
Horn Output (During Low Battery)	On Time	t _{on}	8	10	12	ms
	Between Pulses	t _{off}	32	40	48	s

TIMING DIAGRAM



- NOTES: 1. Horn modulation is self-completing. When going from smoke to no smoke, the alarm condition will terminate only when horn is off.
2. Comparators are strobed on once per clock cycle (1.67 s for no smoke, 40 ms for smoke).
3. Low battery comparator information is latched only during LED pulse.

PACKAGE DIMENSIONS



DEVICE OPERATION

TIMING

The internal oscillator of the MC14466 operates with a period of 1.67 seconds during no-smoke conditions. Each 1.67 seconds, internal power is applied to the entire IC and a check is made for smoke. Every 24 clock cycles a check is made for low battery by comparing V_{DD} to an internal zener voltage. Since very small currents are used in the oscillator, the oscillator capacitor should be of a low leakage type.

DETECT CIRCUITRY

If smoke is detected, the oscillator period becomes 40 ms and the piezoelectric horn oscillator circuit is enabled. The horn output is modulated 200 ms on, 40 ms off. During the off time, smoke is again checked and will inhibit further horn output if no smoke is sensed. During smoke conditions the low battery detection is inhibited, but the LED pulses at a 1.0 Hz rate.

An active guard is provided on both pins adjacent to the detect input. The voltage at these pins will be within 100 mV of the input signal. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard op amp is not power strobed and thus gives constant protection from surface leakage currents. Pin 16 of the active guard is connected to pin 15 (the detect input) during shipping to protect pin 15 from static damage.

SENSITIVITY/LOW BATTERY THRESHOLDS

Both the sensitivity threshold and the low battery voltage levels are set internally by a common voltage divider con-

nected between V_{DD} and V_{SS} . These voltages can be altered by external resistors connected from pins 3 or 13 to either V_{DD} or V_{SS} . There will be a slight interaction here due to the common voltage divider network.

TEST MODE

Since the internal op amps and comparators are power strobed, adjustments for sensitivity or low battery level could be difficult and/or time-consuming. By forcing pin 12 to V_{SS} , the power strobing is bypassed and the outputs, pin 1 and 4, constantly show smoke/no smoke and good battery/low battery, respectively. Pin 1 = V_{DD} for smoke and pin 4 = V_{DD} for low battery. In this mode and during the 10 ms power strobe, chip current rises to approximately 50 μ A.

LED PULSE

The 9-volt battery level is checked every 40 seconds during the LED pulse. The battery is loaded via a 10 mA pulse for 10 ms. If the LED is not used, it should be replaced with an equivalent resistor such that the battery loading remains at 10 mA.

HYSTERESIS

When smoke is detected, the resistor/divider network that sets sensitivity is altered to increase sensitivity. This yields approximately 100 mV of hysteresis and avoids false triggering.

FIGURE 2 — TYPICAL APPLICATION AS IONIZATION SMOKE DETECTOR

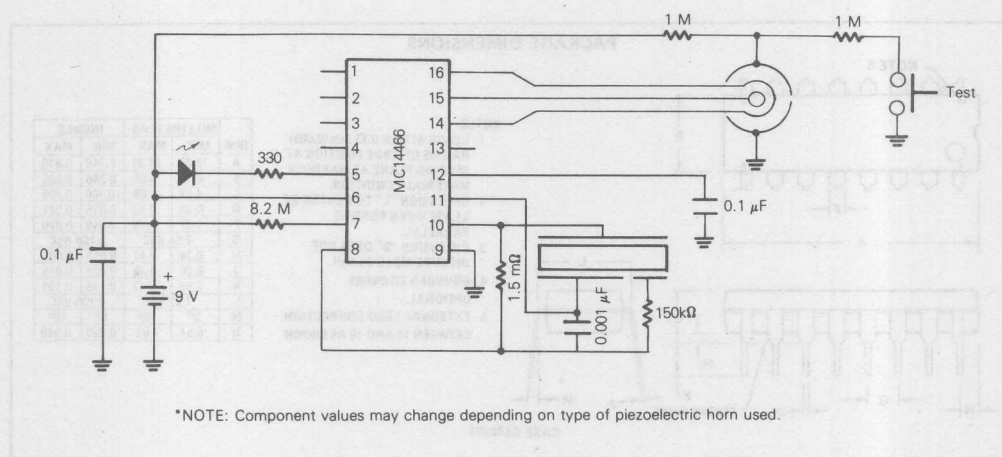
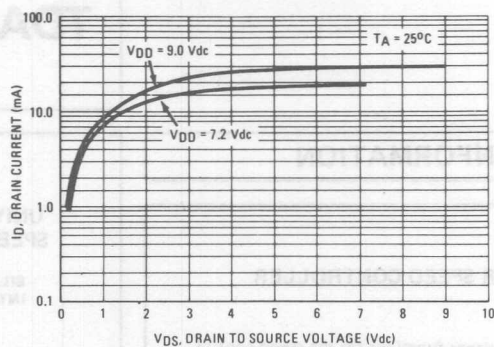
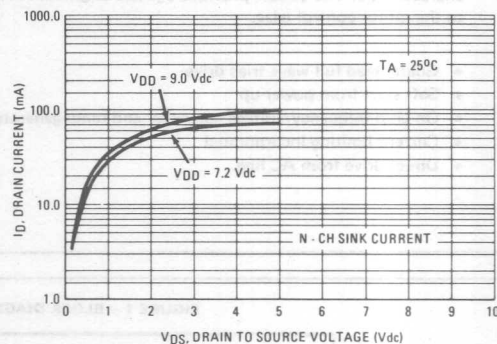
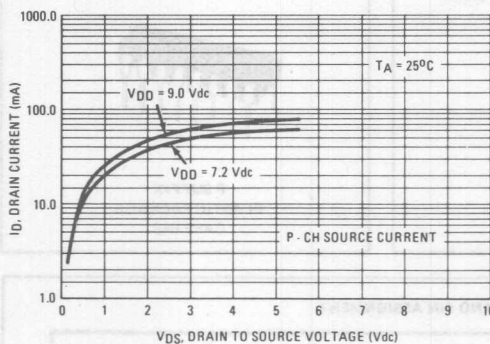
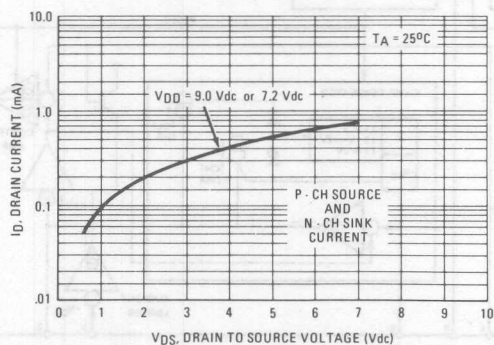


FIGURE 3 — TYPICAL LED OUTPUT
I-V CHARACTERISTICFIGURE 4 — TYPICAL P HORN DRIVER OUTPUT
I-V CHARACTERISTICFIGURE 5 — TYPICAL COMPARATOR OUTPUT
I-V CHARACTERISTIC

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TDA 1085 A, C

ADVANCE INFORMATION

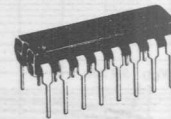
UNIVERSAL MOTOR SPEED CONTROLLER

The TDA1085A has all the necessary functions for the speed control of universal (AC/DC) motors in a closed loop configuration. Additionally it has the facility for defining the initial speed/time characteristic. The circuit provides a phase angle varied trigger pulse to the motor control triac.

- Guaranteed full wave triac drive
- Soft start from power-up
- On-chip frequency/voltage convertor and ramp generator
- Current limiting incorporated
- Direct drive from AC line.

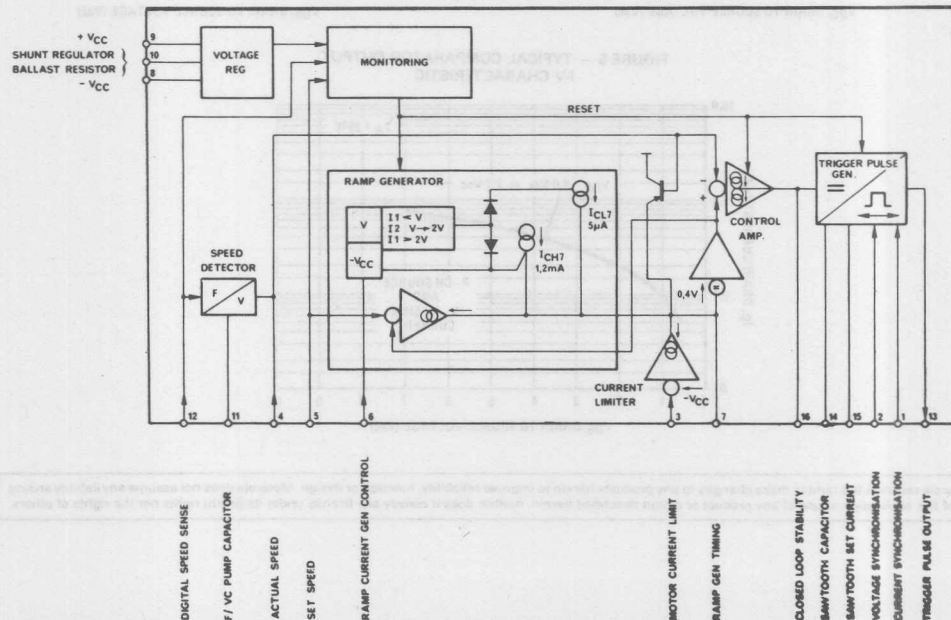
UNIVERSAL MOTOR SPEED CONTROLLER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 - BLOCK DIAGRAM AND PIN ASSIGNMENT



MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V _{pin 9-8}	17	V
Power Supply Current (pin 10 open)	I _{pin 9}	15	mA
Peak Power Supply Regulation Current	I _{pin 9} + I _{pin 10}	35	mA
Peak AC Synchronisation Input Current	I _{pin 1} I _{pin 2}	±1	mA
Peak Output Triggering Current (pulse width 300 µs; duty cycle ≤3%)	I _{pin 13}	200	mA
Current Drain per listed pin	I ₁₅ I ₃ I ₁₂	1 -5 -3, +0.1	mA
Power Dissipation (T _A = 25 °C) Derate above 25 °C	P _D 1/θ _{JA}	625 6.8	mW mW/°C
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = +25 °C Unless Otherwise Stated)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Voltage Regulator	Regulated Voltage* (I _g + I ₁₀ = 10 mA)	V _{CC}	14	15.5	17	V
	Monitoring Enable Level*	V _{ME}	V _{CC} - 1	15.1	V _{CC} - 0.3	V
	Monitoring Disable Level*	V _{MD}		14.5		V
	Internal Current Consumption ¹	I _{pin 9}		4.2		mA
Ramp Generator	Reference Input voltage Range ²	V _{pin 5-8}	0.08		13.5	V
	Reference Input Bias Current	I _{pin 5}			-20	µA
	Distribute Low Level Voltage Range	V _{pin 6}	0		2	V
	Distribute—Low Level (fig. 2)	V _{DL}	V _{pin 6} - 20mV	V _{pin 6}	V _{pin 6} + 20mV	V
	Distribute—Upper Level* (fig. 2) (V _{pin 6} = 950 mV)	V _{DU}	1.9 V ₆	2 V ₆	2.1 V ₆	V
	Low—High Acceleration Range (fig. 2)	ΔV _{DA}		400		mV
	High Acceleration Charging Current	I _{CH7}		1.2		mA
	Low Charging Current ³	I _{CL7}	3	5	7	µA

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Current Limiter	Stage Current Gain	$\frac{\Delta I_{DL7}}{\Delta I_3}$	65	170	235	—
	Output Discharge Current Swing	I_{DL7}		3.5	7	mA
Control Amplifier	Actual Speed Voltage Range	$V_{pin\ 4-8}$	0		13	V
	Actual Speed Input Bias Current	$I_{pin\ 4}$			-350	nA
	Total Input Offset Voltage ⁴	V_{off}	-60		-1	mV
	Transconductance $\left(\frac{\Delta I_{pin\ 16}}{(\Delta V_{pin\ 4} - \Delta V_{pin\ 7})} \right)$	gm	200	300	400	$\mu A/V$
	Output Current Swing	$I_{pin\ 16}$		± 100		μA
Frequency/Voltage Converter	Input Signal Low Voltage ⁵	V_{L12}	-0.1			V
	Input Signal High Voltage	V_{H12}	0.1		5	V
	Polarisation Current	$I_{pin\ 12}$		-25		μA
	Conversion Rate ⁶ *	K_C		15		mV/Hz
	Pin 12 clamped voltage in reset condition			5.6		V _i
Trigger Pulse Generator	Voltage Synchronisation Levels	$I_{pin\ 2}$		± 50	± 100	μA
	Current Synchronisation Levels	$I_{pin\ 1}$		± 50	± 100	μA
	Input Voltage Swing (for full angle swing)	V		11.7		V
	Trigger Pulse Width ⁷	t		55	85	μs
	Trigger Pulse Repetition Period	T		215	400	μs
	Trigger Pulse High Level ($I_{pin\ 13} = 150\ mA$)	$V_{pin\ 13}$	$V_{CC}-4$			V
	Output Leakage Current ($V_{pin\ 13} = 0\ V$)	$I_{opin\ 13}$			30	μA

NOTES:

¹ Pins 1, 2, 11, 12, 14 and 15 not connected; pins 4, 5, 6 and 7 grounded to pin 8: $V_{CC} = 15.5\ V$

² When $V_{pin\ 5}$ is $\leq 80\ mV$, the internal monitoring circuit interprets it as a true zero, thus minimising the effects of control amplifier offsets.

³ This value should be accounted for when externally setting the distribute acceleration charging current.

⁴ V_{off} is defined as being the voltage difference between pin 5 and 4 with no current flow on pin 16.

⁵ The negative swing is clamped to $-0.3\ V$.

⁶ $V_{pin\ 4} = K \cdot C_{pin\ 11} \cdot (V_{CC} - V_a) \cdot R_{pin\ 4} \cdot \left(1 + \frac{140 \times 10^3}{R_{pin\ 11}} \right) \cdot freq_{in}$

Where: $9 < K < 13$ & $V_a = 1.3\ V$.

⁷ The timing given is when $C_{pin\ 14} = 47\ nF$

* These figures apply for the application shown in figure 4.

INPUT/OUTPUT FUNCTIONS

VOLTAGE REGULATOR — (pins 8, 9, 10). This is a parallel type voltage regulator able to sink a large amount of current while offering good regulation characteristics.

A resistor between pins 9 and 10 reduces the internal power dissipation. Under minimal current sink conditions (min. current from the unregulated supply, max. consumption by the circuitry) at least 1 mA should flow through this resistor. Under max. sink conditions (max. current from the unregulated supply, min. consumption by the circuitry) the maximum resistor value is chosen so that the voltage at pin 10 falls towards 3 V, but not lower. The above, fixed dynamic range of the regulator must not be exceeded within one line cycle.

A power supply failure causes shut-down.

For operation from an externally regulated voltage, pin 10 is not connected.

SPEED SENSING — (pin 4, 11, 12). Speed sensing can be achieved either digitally (tachogenerator frequency) or analogically (tachogenerator amplitude).

For digital sensing a bipolar signal, with respect to ground, is applied to pin 12. During positive excursions C_{pin 11} is charged. An internal mirror delivers ten times

the charge on C_{pin 11} via pin 4. However, due to internal circuitry the charge on pin 4 can vary in the region of 9 to 13 times the charge on C_{pin 11}. For that reason it is necessary to calibrate the Frequency/Voltage Converter (F/V/C) with a variable resistor on pin 4. Thus as can be seen the relationship between speed and V_{pin 4} is defined by R_{pin 4} and C_{pin 11}.

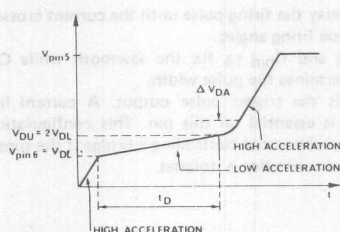
To maintain linearity in the high speed ranges it is important that C_{pin 11} is fully charged across an equivalent resistor of about 140 k Ω . It should be borne in mind that the impedance on pin 11 should be kept as low as possible as C_{pin 11} has a large influence on the temperature coefficient of the FV/C. The time constant on pin 4 should also be kept as low as possible.

Pin 12 is also an impedance monitoring input; at high impedances V_{pin 12} increases. Should V_{pin 12} exceed 5 V the triac trigger pulses are inhibited and the circuit resets.

A 470 k Ω resistor from pin 11 to +V_{CC} significantly reduces the leakage current and reduces the device temperature coefficient to almost zero.

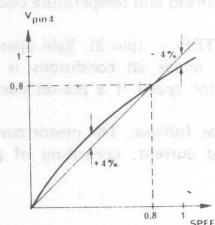
For analogue sensing input 12 should be grounded and a positive signal, with respect to ground, pin 8, applied to pin 4.

FIGURE 2 — RAMP GENERATOR
TRANSFER CHARACTERISTIC



The shape of the curve is determined by C_{Rpin 7}; where C_{pin 7} defines the high acceleration slope and R_{pin 7} defines that of the low acceleration.

FIGURE 3 — FREQUENCY/VOLTAGE CONVERTER
OUTPUT CHARACTERISTIC



INPUT/OUTPUT FUNCTIONS (continued)

RAMP GENERATOR — (pin 5, 6, 7) (refer to figure 2). A pre-set voltage applied to pin 5 will initiate the generation of a ramp whose final value is determined by the voltage applied to pin 5. The voltage applied to pin 6 will determine how much of the full ramp, shown in figure 2, is used. The charging current passing through pin 7 to the ramp generator timing capacitor determines the ramp slope.

When pin 6 is held at $-V_{CC}$ a charging current of 1.2 mA is delivered to pin 7, regardless of the voltage of pin 5. This represents the high acceleration period shown in figure 2.

If the pre-set voltage applied to pin 5 is equal to or less than the voltage on pin 6 the charging current will be 1.2 mA, high acceleration.

If the pre-set voltage applied to pin 5 is between $V_{pin 6}$ and $2 V_{pin 6}$ the charging current is 1.2 mA, high acceleration, until the voltage at the reference input of the control amplifier equals $V_{pin 6}$. At this point the charging current will switch to 5 μA ; i.e. low acceleration.

If the pre-set voltage applied to pin 5 is greater than $2 V_{pin 6}$ the charging current will be 1.2 mA, high acceleration, until the control amplifier's reference input reaches $V_{pin 6}$ when it will switch to 5 μA , low acceleration, until $2 V_{pin 6}$ is reached. At this point the charging current will revert to 1.2 mA, high acceleration, until the final value, $V_{pin 5}$, is reached.

Should the pre-set voltage at pin 5 fall below 80 mV the triac trigger pulses are inhibited and the circuit resets. This fact should be borne in mind when switching from one pre-set value to another.

As long as the voltages applied at pins 5 and 6 are derived from the internal voltage regulator they and the voltage on pin 4 are ratioed and thus independent of the voltage regulator spread and temperature coefficient.

CURRENT LIMITER — (pin 3). Safe operation of the motor and triac under all conditions is ensured by reducing the motor speed if a pre-set current limit is exceeded.

This is achieved as follows: The motor current will set up an alternating current, consisting of positive and

negative peaks, through the shunt resistor (0.05 Ω in figure 4).

The negative peaks of this current are fed through a resistor to pin 3 where they are compared with a pre-set current, defined by a further resistor between pin 3 and $+V_{CC}$. An excessive shunt current will try to pull pin 3 below $-V_{CC}$, but the current limiter becomes active at this point and reduces the charge on $C_{pin 7}$ consequently reducing the motor speed.

Thus the value of the shunt and the ratio of the two resistors to pin 3 fix the level at which the limiter becomes active while the parallel equivalent of the two resistors determines the magnitude of the discharge current and thus how rapidly the circuit responds to an over current condition.

CONTROL AMPLIFIER — (pin 16). Connected to this pin is a network which compensates electrically for the mechanical characteristics of the motor and its load to give the circuit optimum closed loop stability and transient response.

The component values are best determined empirically by connecting R and C substitution boxes and looking for the best results.

TRIGGER PULSE GENERATOR — (pins 1, 2, 13, 14, 15). This circuit performs four functions:

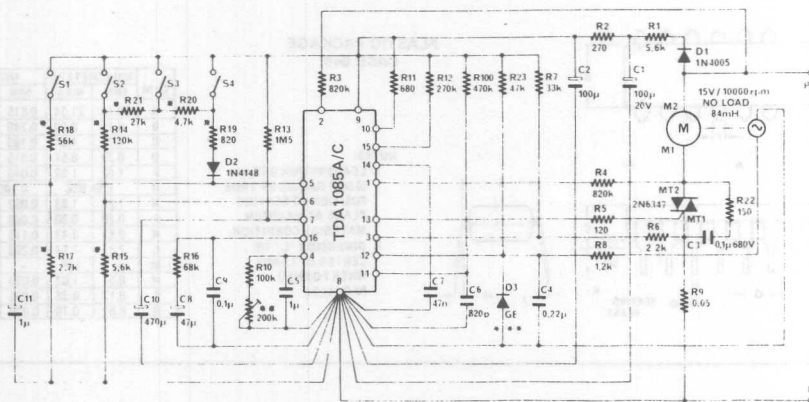
1. The conversion of the control amplifier's DC output level to a proportional firing angle positioned to within half a line cycle.
2. The calibration of the pulse width.
3. The repetition of the firing pulse if the triac fails to latch, or if the current is interrupted by brush bounce.
4. To delay the firing pulse until the current crosses zero at wide firing angles.

$R_{pin 15}$ and $C_{pin 14}$ fix the sawtooth while $C_{pin 14}$ also determines the pulse width.

Pin 13 is the trigger pulse output. A current limiting resistor is essential on this pin. This configuration will drive two thyristors controlling a bridge if the supply for the speed controller is isolated.

TYPICAL APPLICATIONS

FIGURE 4 – CLOSED LOOP, FULLY PROGRAMMED, MULTI-SPEED SYSTEM WITH CURRENT LIMITING



- * Chosen to suit the speeds required
- ** Adjust for the highest speed
- *** Required only with 'A' suffix device

Speed Control Resistor Network Equations

R17	=	given
R18	=	$R17 \left(\frac{15.5 \text{ V}}{V_W} - 1 \right)$
R19	=	$R17 \left(\frac{14.8 \text{ V}}{V_{\text{spin } 2}} - 1 \right)$
R20	=	$R17 \left(\frac{14.8 \text{ V}}{V_{\text{spin } 1}} - 1 \right) - R19$
R21	=	$R17 \left(\frac{14.8 \text{ V}}{K \cdot V_W} - 1 \right) - R19 - R20$
R15	=	$R21 \left(\frac{K \cdot V_W}{15.5 \text{ V} (2 \cdot K)} \right)$
R14	=	$R15 \left(\frac{15.5 \text{ V}}{V_W} - 1 \right)$

The ratio distribute speed to wash speed can be chosen as:

$$\frac{V_{\text{DIST}}}{V_{\text{WASH}}} \cdot 2 = K$$

Note:

When changing from one speed to another $V_{\text{pin } 5}$ must not be allowed to fall below 80 mV—otherwise the circuit will reset and restart from zero.

	S1	S2	S3	S4	$V_{\text{pin } 5}$	$V_{\text{pin } 6}$
Wash	sc	oc	oc	oc	V_W	0
Distribute	oc	sc	oc	oc	$K V_W$	V_W
Spin 1	oc	oc	sc	oc	$> K V_W$	$\frac{K}{2} V_W$
Spin 2	oc	oc	oc	sc	$>> K V_W$	$\sim \frac{K}{2} V_W$

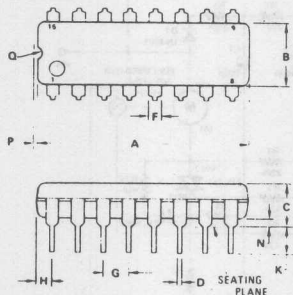
sc = switch closed, oc = open

The component values given in figure 4 correspond to

$$\begin{aligned} V_W &= 0.7 \text{ V} \\ V_D &= 1.13 \text{ V} \\ V_{\text{spin } 1} &= 5 \text{ V} \\ V_{\text{spin } 2} &= 11 \text{ V} \\ K &= 1.6 \end{aligned}$$

TYPICAL APPLICATIONS

PACKAGE DIMENSIONS



PLASTIC PACKAGE
CASE 648

- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.54 BSC		0.100 BSC	
G	1.32	1.83	0.052	0.072
H	0.20	0.30	0.008	0.012
J	2.92	3.43	0.115	0.135
K	7.37	7.87	0.290	0.310
L	10°		10°	
M	0.51	1.02	0.020	0.040
N	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

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TDA 1185

Product Preview

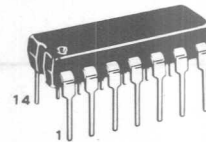
TRIAC FIRING ANGLE CONTROL CIRCUIT

The TDA 1185 generates gate trigger pulses for a triac with a controllable phase delay. Feedback loop control is possible, for applications such as motor speed control. Another typical application is for the soft start-up of power circuitry.

- Low external component count
- AC supply 50/60 Hz
- Full wave triac drive
- Circuit reset in case of power down
- Repetition of firing pulse if triac fails to latch or current interrupted by brush bounce
- Typically 1mA current consumption
- Soft-start
- Low cost applications.

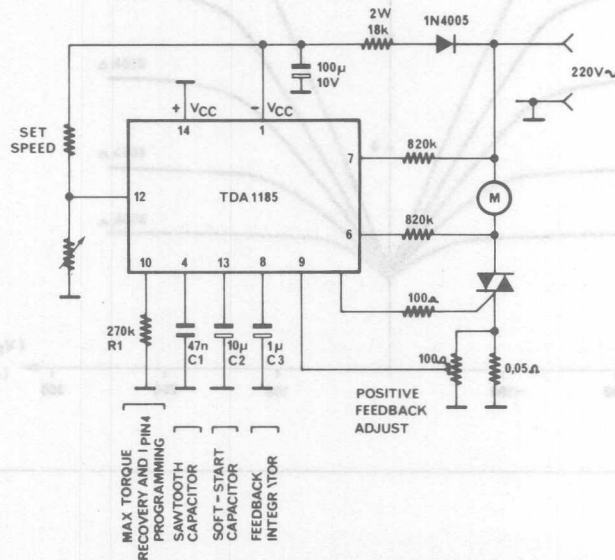
TRIAC FIRING ANGLE CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – TYPICAL SYSTEM CONFIGURATION

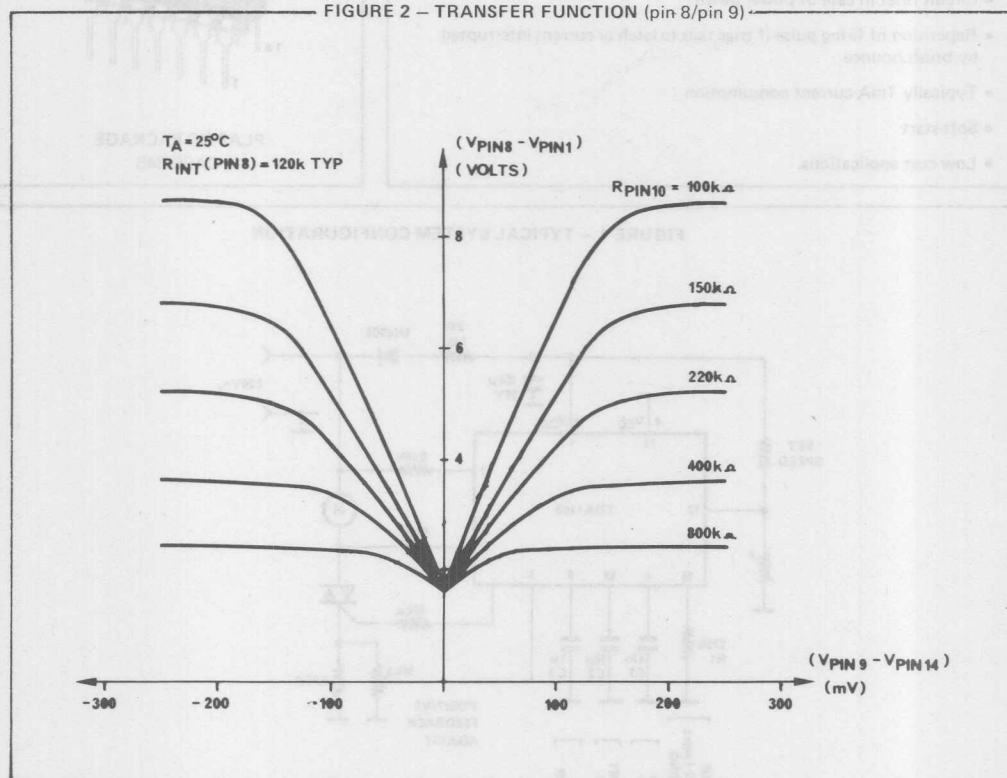


TDA1185

ELECTRICAL CHARACTERISTICS

Characteristic	Min	Typ	Max	Units
Operating Voltage		8.6		V
Current Consumption Pin 2 not connected		1		mA
Output Pulse Current	60			mA
Output Pulse Width $C_1 = 47\text{nF}$		55		μS
Saw-tooth Sink Current Pin 4		$\frac{7.3}{R_1}$		A
Saw-tooth Peak (referred to Pin 14)		-1.58		V
Saw-tooth Low Threshold Referred to Pin 14)		$-(V_{CC} - 1.48)$		V
Comparator Offset ($V_{\text{pin 4}} - V_{\text{pin 12}}$)		280		mV

FIGURE 2 - TRANSFER FUNCTION (pin 8/pin 9)



CIRCUIT DESCRIPTION

The TDA 1185 generates trigger pulses for a triac for phase control of the power in a load, such as an AC motor. The firing angle of the triac is determined by comparison of a ramp voltage synchronised to the AC supply line half period and an adjustable set voltage. A single capacitor on pin 4 determines the slope of the ramp and the trigger pulse width. The set voltage is the sum of the voltages on pin 12 and pin 8. Pin 12 is the connection for the normal control potentiometer, e.g. motor speed control. Pin 8 is connected to an integrating capacitor C_3 and in the typical system configuration (see figure 1) the voltage at pin 8 is the smoothed, full wave rectified and amplified voltage given by the signal on pin 9. Pin 9 is thus a positive feedback input with transfer function as shown in figure 2.

The circuit in figure 1 provides torque regulation of an AC motor due to the increasing current vs. load characteristic of the motor. Regulation characteristics of this circuit with a commercial AC motor are shown in figure 3.

The current consumed by the circuit is the sum of the internal I.C. consumption plus the average of the trigger current pulses, which totals typically 2mA. Together

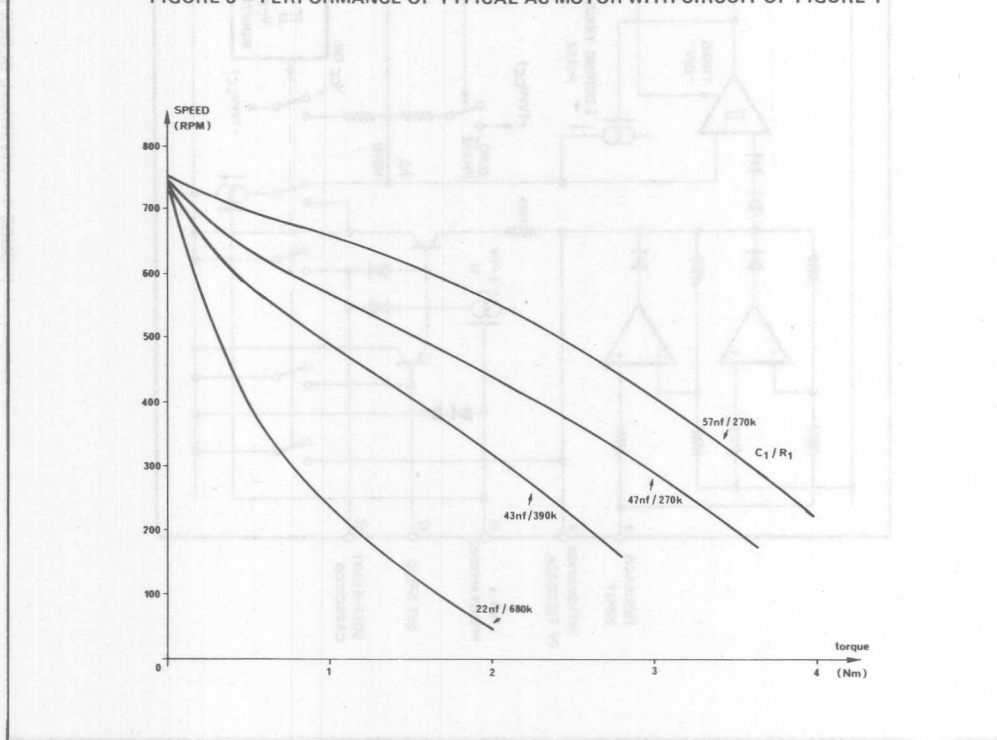
with a low stabilised supply voltage of 8.6V this allows a low-cost dropping resistor and low-cost electrolytic capacitor to be used as the power supply.

Capacitor C_2 in figure 1 provides a soft-start characteristic: the firing angle increases gradually from zero when power is first applied, at a rate determined by the value of C_2 . If power to the circuit is interrupted, a reset occurs in which C_2 is discharged. Thus a soft-start occurs after a power line interruption.

Synchronisation with the line zero crossing voltage is derived through pin 7. In controlling inductive loads, the current lags the voltage in the load so current synchronisation is also included via pin 6.

AC motor brush noise can cause the triac current to collapse and load to half-wave or asymmetric use of the AC line. Therefore the TDA 1185 incorporates circuitry to repeat the triac trigger pulse if the triac has failed to latch. The value of C_1 in figure 1 sets the pulse repetition delay as well as the synchronisation ramp slope and trigger pulse width as described above.

FIGURE 3 — PERFORMANCE OF TYPICAL AC MOTOR WITH CIRCUIT OF FIGURE 1



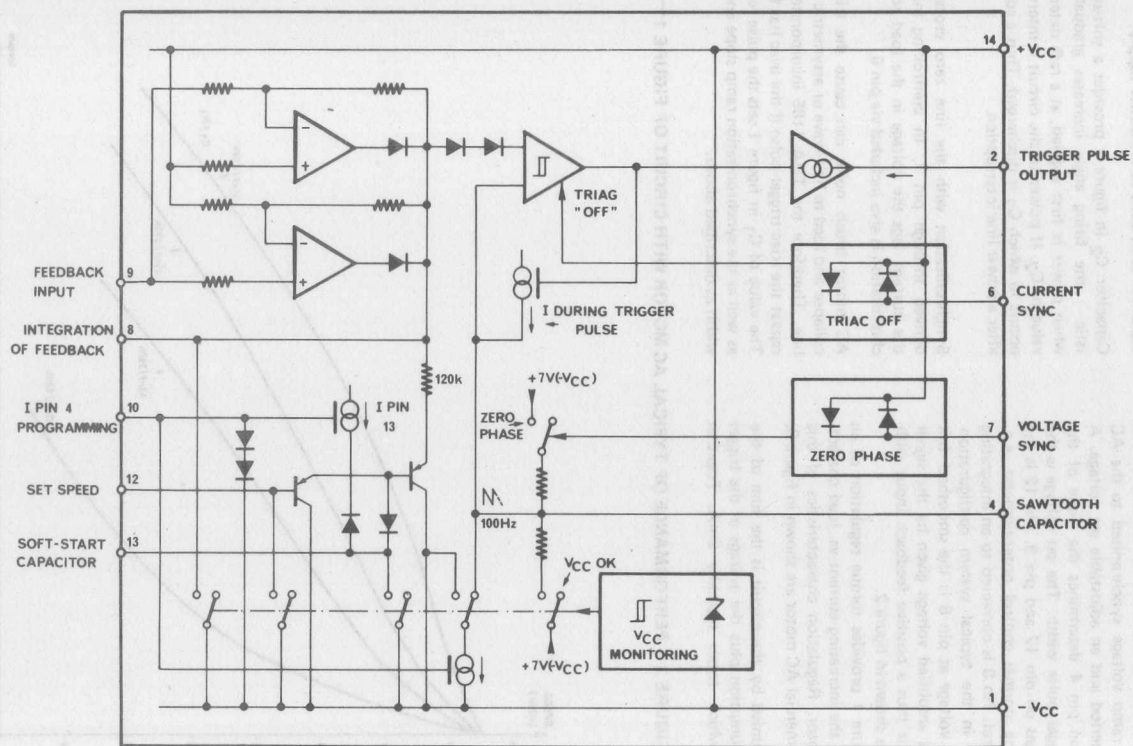


FIGURE 4 — INTERNAL BLOCK DIAGRAM

UAA 1004-DP **UAA 1004-CM**

ZERO VOLTAGE SWITCH

Designed for use in high volume AC power switching applications with output drive capable of triggering SCR's or triacs. Other operational features include:

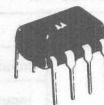
- Direct AC line or DC operation.
- A zero voltage crossing detector that synchronises the SCR or the triac at the zero crossing of the AC line voltage.
- High impedance input differential amplifier.
- Built-in hysteresis which avoids a DC current component through the load.
- Fail safe: a high impedance differential amplifier which supervises the sensor and insures that the triac will never turn "on" due to sensor failure.
- High power, asymmetric gate trigger pulses for power saving with internal current limitation. (Negative pulses)
- Voltage regulator for the supply of the sensor or other external circuits.

Typical Applications:

- | | |
|----------------------|------------------------|
| • heater control | • valve control |
| • hot plate control | • on-off power control |
| • photo control | • relay driver |
| • threshold detector | • lamp driver |

ZERO VOLTAGE SWITCH

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



DP SUFFIX
PLASTIC PACKAGE
CASE 626



CM SUFFIX
METAL PACKAGE
CASE 601
TO-99

PIN CONNECTIONS

1. INVERTING INPUT (INPUT AMP.)
2. NON INVERTING INPUT (FAIL SAFE)
3. AUXILIARY VOLTAGE ($-$)
4. $+ V_{cc}$ (GROUND)
5. AC LINE
6. OUTPUT
7. $- V_{cc}$
8. NON INVERTING INPUT (INPUT AMP.)

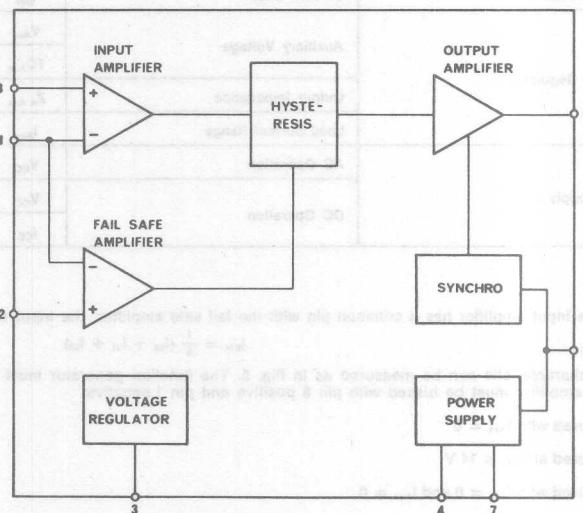


FIGURE 1 - BLOCK DIAGRAM

UAA1004-DP, UAA1004-CM

MAXIMUM RATINGS

Rating	Symbol	UAA1004-DP	UAA1004-CM	Unit
External DC Power Supply	V_{CC} (4-7)	20		Vdc
AC Peak Supply Current (sine wave, 50-60 Hz)	I_{AC} (5-4)	55		mA
Differential Input Voltage	V_{in} (1-8)	± 6		Vdc
	V_{in} (1-2)	± 6		Vdc
Power Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625	680	mW
	$1/\theta_{JA}$	5.0	4.6	mW/ $^\circ\text{C}$
Operating Temperature Range	T_A	-20 to +75	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	-65 to +150	$^\circ\text{C}$

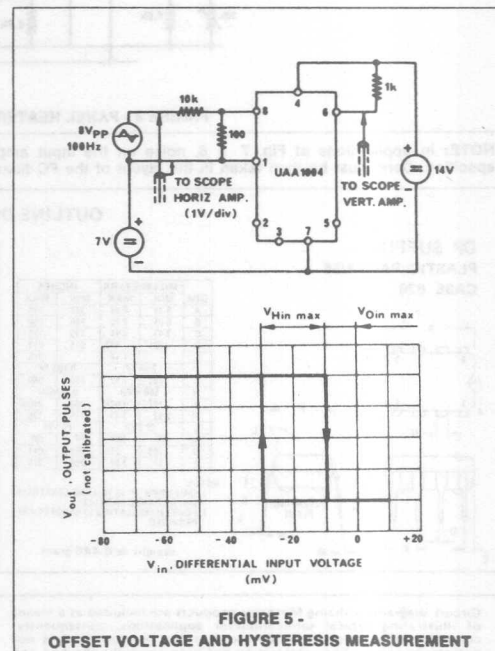
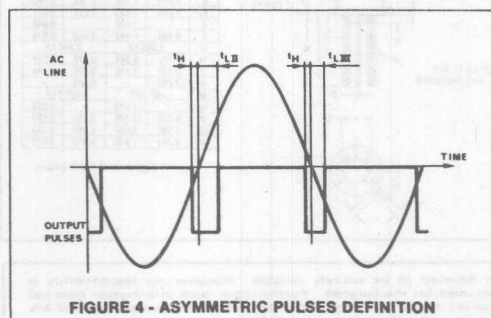
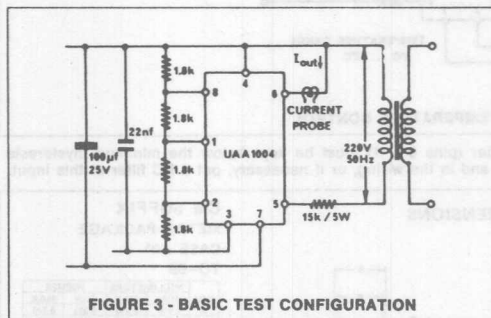
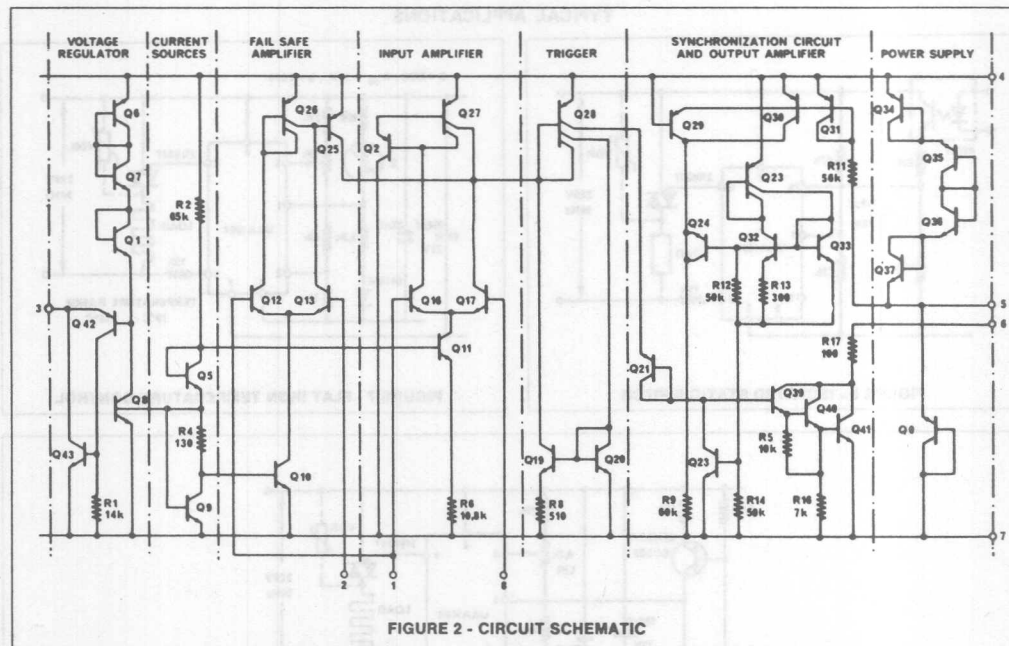
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ Unless Otherwise Stated)

Characteristics	Symbol	Fig./Note	Min	Typ	Max	Unit
Input Differential Amplifier	Input Common Mode	CMV_{in}	-1		$-V_{CC} + 2$	V
	Input Bias Current	I_{bin}	Note 1		1	μA
	Input Offset Voltage	V_{oin}	-10		+10	mV
Schmitt-Trigger	Hysteresis	V_{Hin}	+10		+20	mV
Fail Safe Amplifier	Input Common Mode	CMV_{fs}	-1		$-V_{CC} + 2$	V
	Input Bias Current	I_{bin}	Note 1		1	μA
	Input Offset Voltage	V_{ofs}	Note 2	-20	+20	mV
Synchronization	Pulse Duration	t_{LH}		100		μs
		t_{LHL}	Fig. 3 + 4	75		μs
		t_H		20		μs
Output Amplifier	Current Sink	I_{out}	Note 4	80		mA
Voltage Regulator	Auxiliary Voltage	V_{Aux}		-7.7		V
		TC_{Aux}		-0.7		mV/ $^\circ\text{C}$
	Output Impedance	$Z_{o\text{Aux}}$		10		Ω
	Load Current Range	I_{Aux}	Fig. 3	0.2	3	mA
Main Supply	AC Operation	V_{CC}	Fig. 3/Note 3	-14		V
	DC Operation	V_{CC}		-11		V
		I_{CC}	Note 5		1.9	mA

NOTES

- As the input amplifier has a common pin with the fail safe amplifier, the input bias current of each amplifier is defined as:

$$I_{bin} = \frac{1}{4} (I_{b8} + I_{b1} + I_{b2})$$
- This characteristic can be measured as in Fig. 5. The function generator must be connected between pins 1 & 2 and the input amplifier must be biased with pin 8 positive and pin 1 negative.
- Measured with $I_{Aux} = 0$
- Measured at $V_{CC} = 14\text{ V}$
- Measured with $I_{out} = 0$ and $I_{Aux} = 0$



TYPICAL APPLICATIONS

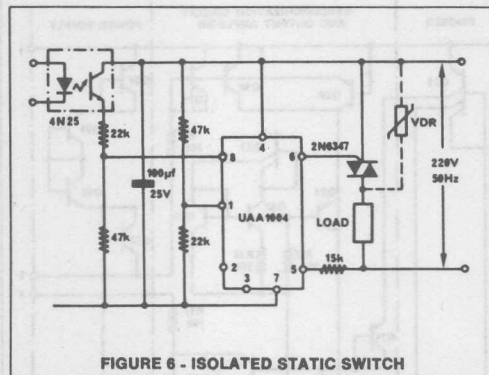


FIGURE 6 - ISOLATED STATIC SWITCH

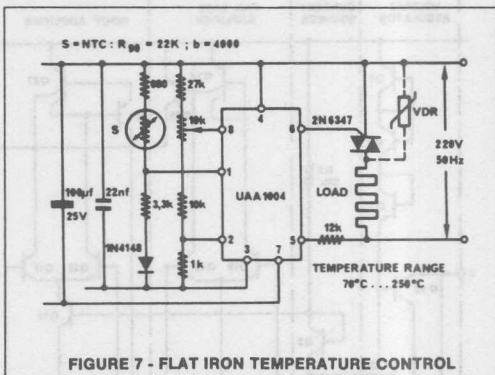


FIGURE 7 - FLAT IRON TEMPERATURE CONTROL

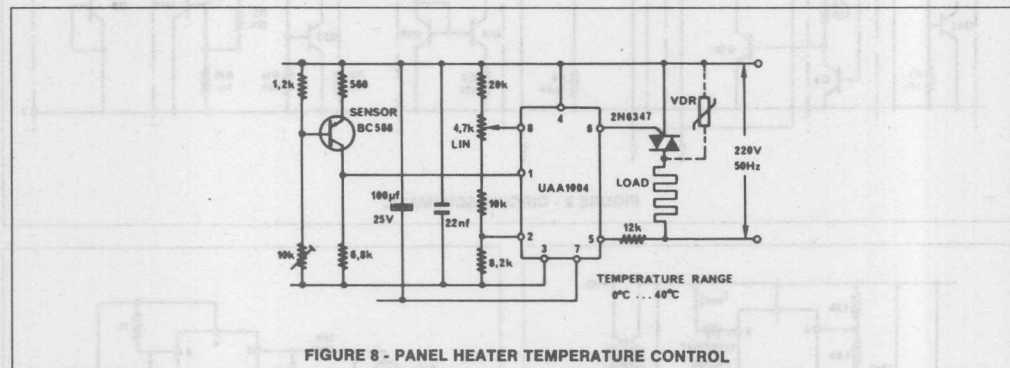
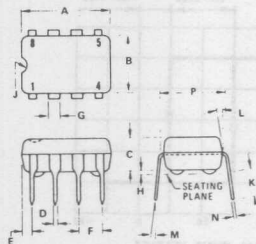


FIGURE 8 - PANEL HEATER TEMPERATURE CONTROL

NOTE: In applications of Fig. 7 & 8, noise on the input amplifier (pins 8 & 1) must be kept below the minimum hysteresis specified. Care must be then taken in the layout of the PC board and in the wiring, or if necessary, put a RC filter at this input.

OUTLINE DIMENSIONS

DP SUFFIX
PLASTIC PACKAGE
CASE 626

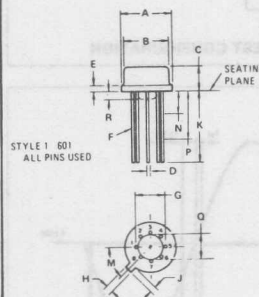


DIM	MIN	MAX	MIN	MAX
A	5.39	9.90	370	390
B	6.09	6.35	240	250
C	3.43	3.94	135	155
D	3.81	4.83	0.15	0.19
E	-	1.14	-	0.45
F	2.54	TP	0.100	TP
G	7.62	1.52	0.30	0.60
H	508	NOM	0.20	NOM
J	7.62	1.02R	0.30	0.40R
K	2.92	3.43	115	135
L	TP	TP	TP	TP
M	0.0	10.0	0.0	10.0
N	203	279	0.08	0.11
P	7.37	7.87	290	310

NOTES:
1. DIMENSION "P" IS TO LEAD CENTERLINE WHEN FORMED PARALLEL.
2. FOUR (4) INSULATING STANDOFFS ARE PROVIDED.

Weight \approx 0.446 gram

CM SUFFIX
METAL PACKAGE
CASE 601
TO-99



DIM	MIN	MAX	MIN	MAX
A	8.510	9.390	0.335	0.370
B	7.750	8.500	0.305	0.335
C	4.700	4.890	0.185	0.195
D	4.070	0.533	0.016	0.021
E	-	1.020	-	0.040
F	0.406	0.482	0.016	0.019
G	9.000	TP	0.200	TP
H	0.712	0.864	0.028	0.034
J	0.737	1.140	0.029	0.045
K	12.700	-	0.500	-
M	45°	TP	45°	TP
N	-	1.270	-	0.050
P	6.350	12.700	0.250	0.500
Q	3.580	4.060	0.140	0.160
R	0.254	1.010	0.010	0.040

Weight \approx 0.920 gram

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is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

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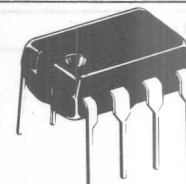
Advance Information

ZERO VOLTAGE BURST CONTROL

Designed for high volume AC power switching applications in conjunction with a triac.

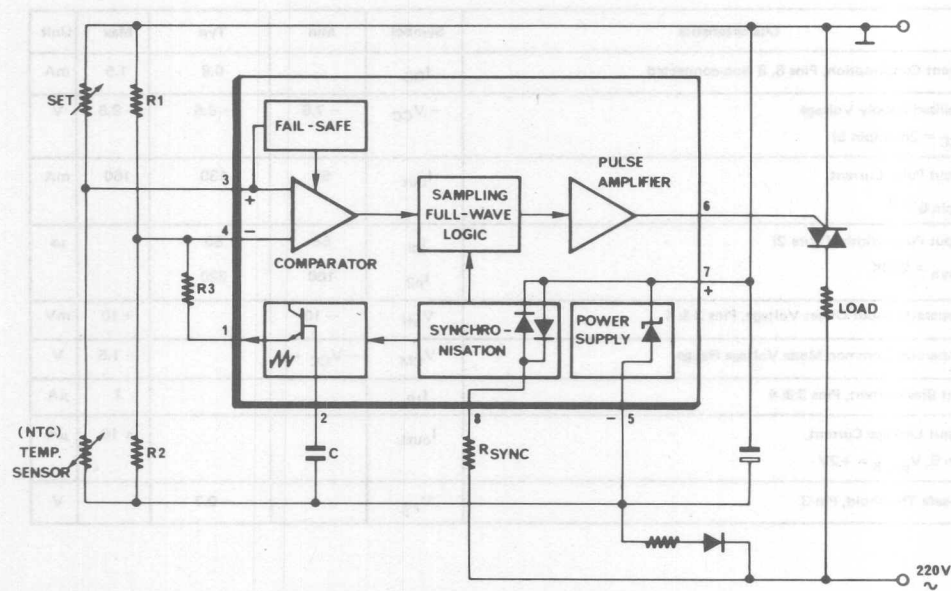
- AC line or DC operation.
- Low external component count.
- Full-wave and zero crossing logic eliminate load dc. current component and RFI.
- Negative output current pulse (Triac quadrants 2 & 3), short circuit protected.
- Linear ramp generator allows precise proportional temperature control, and setting of the burst frequency.
- Sensor fail-safe.
- Allows requirements of EN 50.006 to be satisfied.

ZERO VOLTAGE SWITCH



PLASTIC PACKAGE
CASE 626

FIGURE 1 – BLOCK DIAGRAM & PIN ASSIGNMENT



* R_3 : UAA 1016B only

UAA1016A, B

MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Supply Current (pin 7)	I_{CC}	15	mA
AC Synchronisation Current (50Hz) Pin 8	I_{syn}	3	mA RMS
Input Voltages	$V_{pin\ 3-4}$ $V_{pin\ 2-5}$ $V_{pin-1-3}$ $V_{pin-1-4}$ $V_{pin\ 6-7}$	± 6.7 ± 6.7 $\pm V_{CC}$ $-V_{CC} + 2.0V$	volts
Current Drain (pin 1)	$I_{pin\ 1}$	1	mA
Power dissipation ($T_A = 25^\circ C$)	P_D	680	mW
Thermal resistance	θ_{JA}	200	$^\circ C/W$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$) – Voltages referred to pin 7 unless otherwise indicated.

Characteristics	Symbol	Min	Typ	Max	Unit
Current Consumption, Pins 6, 8 Non-connected	I_{CC}		0.8	1.5	mA
Stabilised Supply Voltage $I_{CC} = 2mA$ (pin 5)	$-V_{CC}$	-7.6	-8.6	-9.6	V
Output Pulse Current $V_{pin\ 6} = 0$	I_{out}	60	130	160	mA
Output Pulse Width (figure 2) $R_{syn} = 220K$	t_{pl} t_{p2}	58 160	80 220		μs
Comparator Input Offset Voltage, Pins 3 & 4	V_{off}	-10		+10	mV
Comparator Common Mode Voltage Range	V_{CM}	$-V_{CC} + 1$		-1.5	V
Input Bias Current, Pins 3 & 4	I_{IB}			1	μA
Output Leakage Current, Pin 6, $V_{pin\ 6} = +2V$	I_{outL}			± 10	μA
Fail-safe Threshold, Pin 3	V_{FS}		-0.7		V

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Saw-Tooth Current Output, Pin 1 UAA 1016A	I_{TL}		2.1		μA
	I_{TH}		15		μA
Pin 1 Clamped Voltage Range For Correct Saw-tooth Operation UAA 1016A	V_{ICL}		-0.5 to $-V_{CC}$		V
Maximum Source Current, Pin 1	$I_{pin\ 1max}$		200		μA
Output Voltage, Pin 1 UAA 1016B	$V_{pin\ 1}$		$V_{pin\ 2} - 0.75$		V
Saw-tooth Threshold Levels, Pin 2	V_{TH1}		$-1V$		V
	V_{TH2}		$(-V_{CC} + 1.25)$		V
Average Capacitor Charging Current, Pin 2 (Source)	$I_{pin\ 2}$		7.5		μA
Capacitor Discharge Current Pin 2 (Sink) Average	$I'_{pin\ 2}$		6.4		mA
Typical Saw-tooth Pulse Length $C = 1\ \mu F$	t_{saw}		0.85		S

CIRCUIT DESCRIPTION

The I.C. can be directly powered from the mains via a dropping resistor, diode, and a smoothing capacitor. The current consumption of the UAA 1016 is typically less than 1 mA so that the average current drawn through the dropping resistor is largely the gate drive for the triac plus the current drawn by the sensor bridge.

Triac drive pulses are delivered at the zero crossings of the mains line sensed by pin 8 if the comparator input (pins 3-4) is positive. Equal numbers of positive and negative half cycles are delivered to the load by synchronizing two zero-crossing trigger pulses to each positive mains half-cycle with the comparator output being sampled at the beginning of the positive half-cycle. The trigger pulses are timed about the zero-crossing point as per figure 2.

The saw-tooth generator output from pin 1 enables proportional temperature control to be achieved by

modulating the comparator voltage (see figure 4). Capacitor C (see figure 1) on pin 2 determines the modulation frequency in conformance with standards such as EN 50.006 (CENELEC). A constant source current from pin 2 charges capacitor C at 7.5 μA typically, between threshold voltages V_{TH1} and V_{TH2} ; C is discharged at an average current of 6.4 mA typically. Pin 1 follows pin 2 such that for the UAA 1016A, the source current is modulated and for the UAA 1016B, the voltage is modulated.

The charging current at pin 2 occurs only with negative half-cycles of the mains and the discharge synchronises also with a negative half-cycle.

Output pulses are inhibited by the "fail-safe" circuit if the comparator input exceeds the specified threshold, which could occur due to a fault in the temperature sensor circuit.

FIGURE 2 — OUTPUT PULSE WIDTH DEFINITIONS

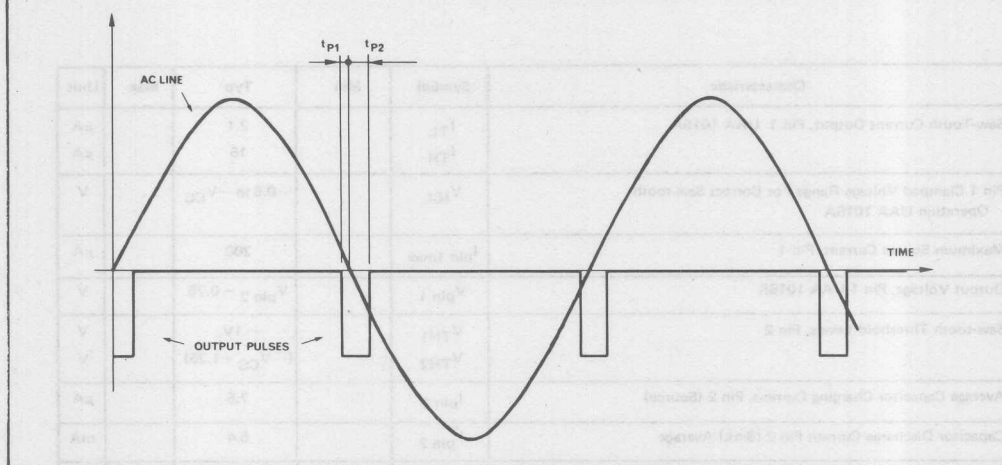


FIGURE 3 — TYPICAL OUTPUT PULSE LENGTH VS. SYNCHRONISATION RESISTOR

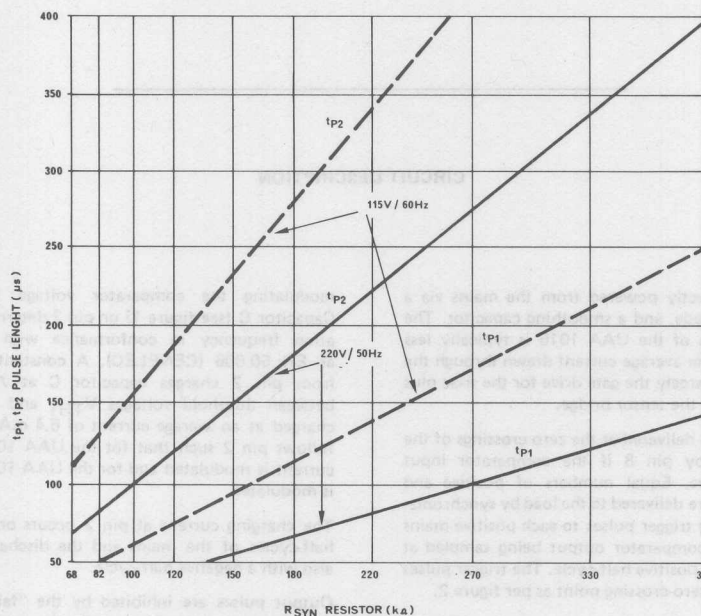


FIGURE 4 — PROPORTIONAL TEMPERATURE CONTROL

The output duty cycle is proportional to the temperature deviation from the set point within the proportional band.

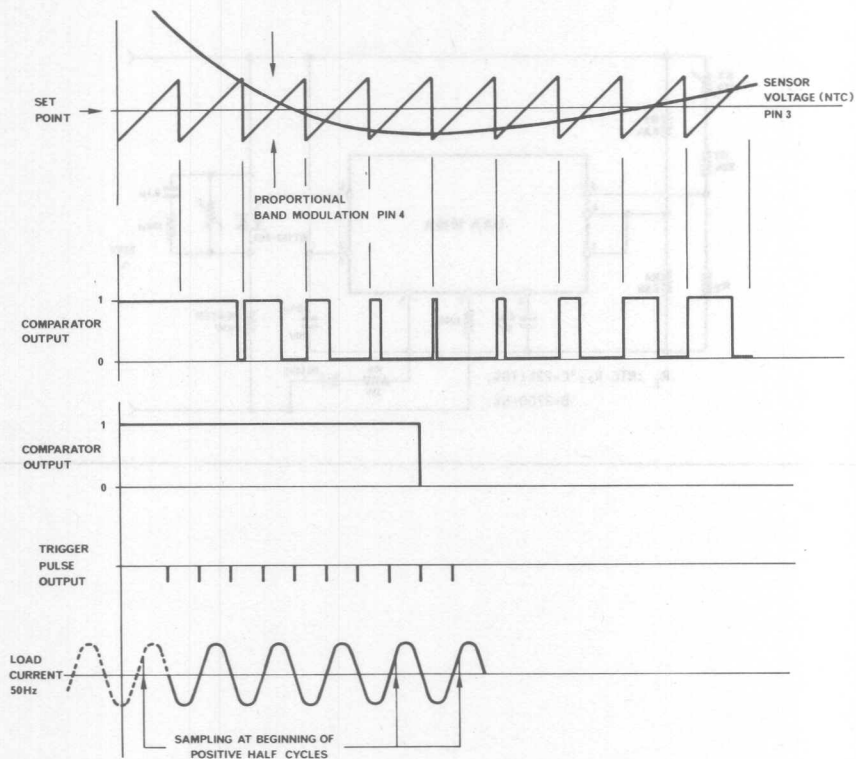


FIGURE 5 — APPLICATION CIRCUIT — ELECTRONIC RHEOSTAT OR ENERGY REGULATOR

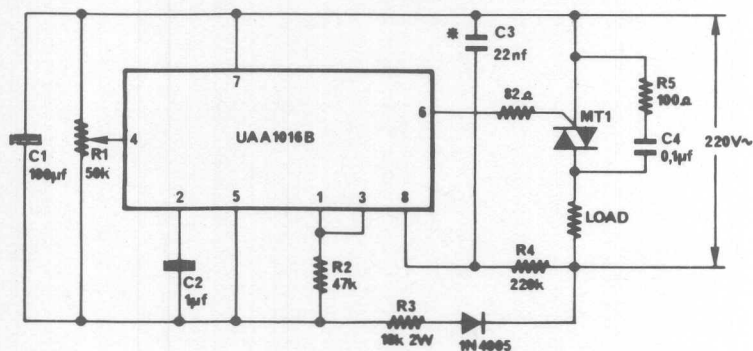
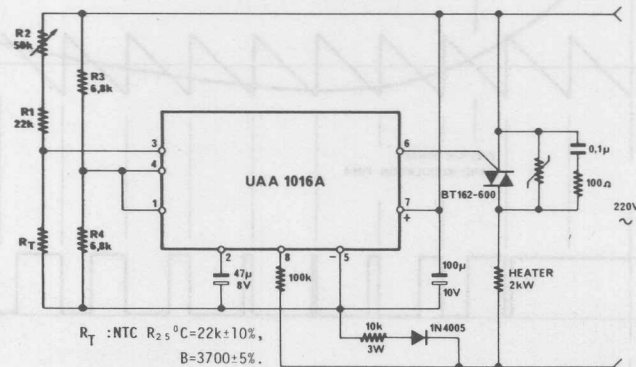


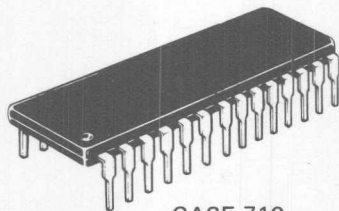
FIGURE 6 — APPLICATION CIRCUIT — ELECTRIC RADIATOR WITH PROPORTIONAL BAND
THERMOSTAT. PROPORTIONAL BAND 1 °C AT 25 °C



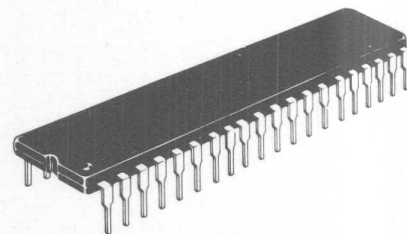
SECTION 6 MICROCOMPUTERS

Page	Package	Description	Device
6-3	711/715	Single-Chip Microcontroller	MC8B11
6-33	710/715/733	HMOS 8-Bit MCU	MC8B05
6-41	711/715/734	HMOS 8-Bit MCU with A/D	MC8B05
6-73	710	HMOS 8-Bit MCU with PLL	MC8B05
6-73	711/715/734	HMOS 8-Bit MCU	MC8B05
6-73	711/715	HMOS 8-Bit MCU	MC8B05

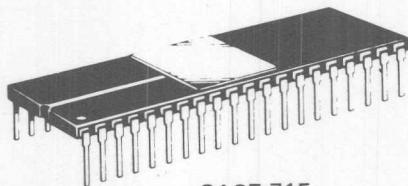
Section 6—Packages



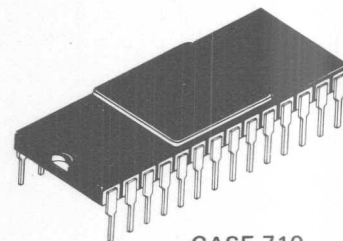
CASE 710



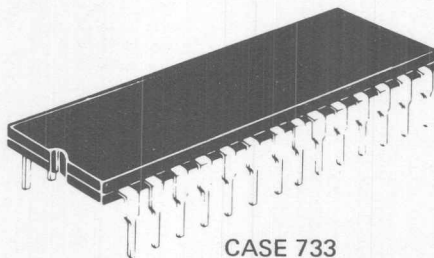
CASE 711



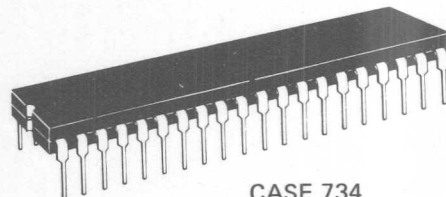
CASE 715



CASE 719



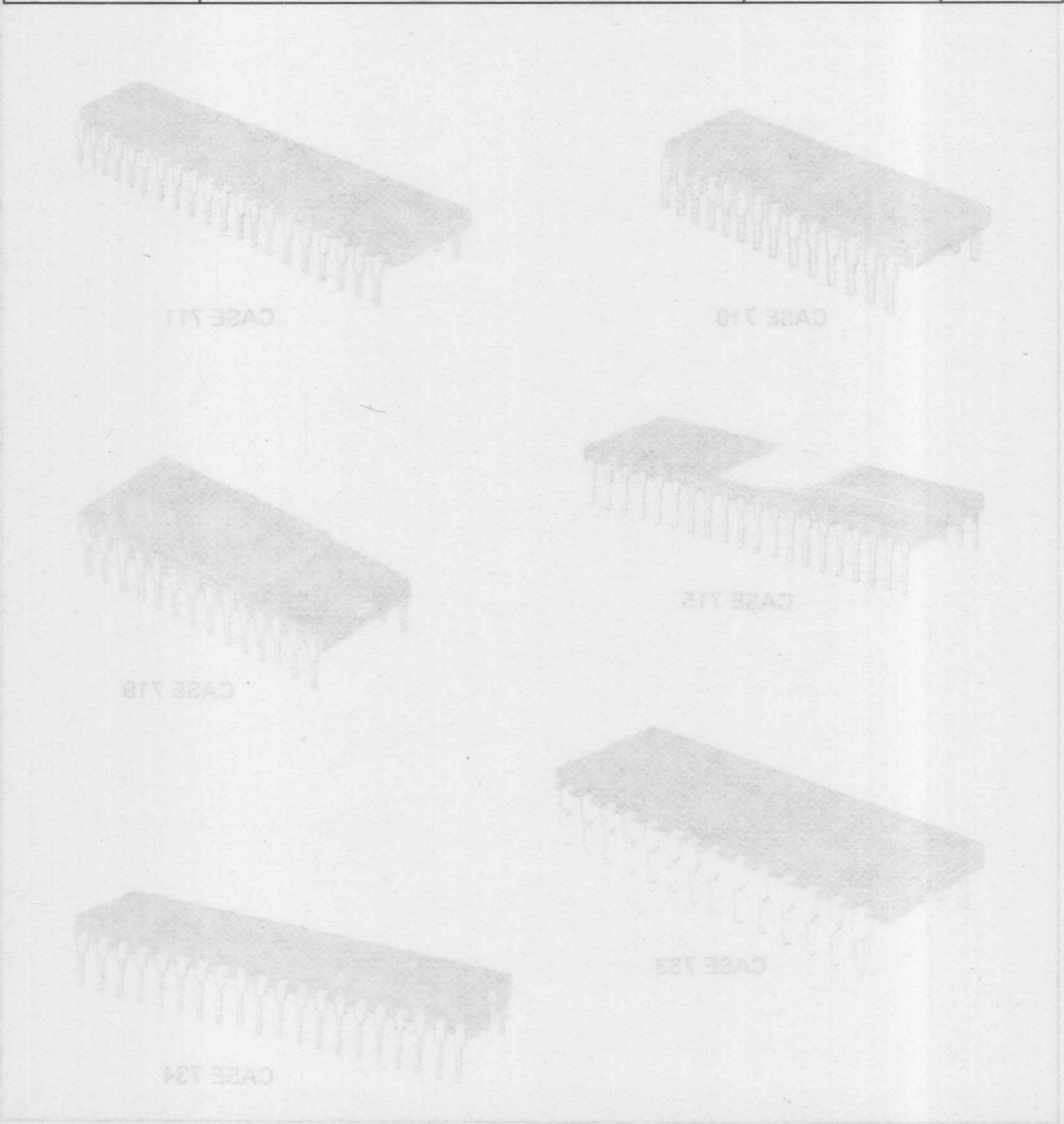
CASE 733



CASE 734

MICROCOMPUTERS

Device	Designation	Package	Page
MC3870	Single-Chip Microcontroller	711/715	6 - 3
MC6805P2	HMOS 8-Bit MCU	710/719/733	6 - 23
MC6805R2	HMOS 8-Bit MCU with A/D	711/715/734	6 - 47
MC6805T2	HMOS 8-Bit MCU with PLL	710	6 - 73
MC6805U2	HMOS 8-Bit MCU	711/715/734	6 - 12
MC141000	CMOS LSI One Chip Microcomputer	710/719	6 - 128



MC3870

Advance Information

SINGLE-CHIP MICROCONTROLLER

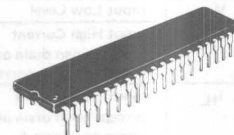
The MC3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. Utilizing ion-implanted, N-channel silicon-gate technology and advanced circuit design techniques, the single-chip 3870 offers maximum cost effectiveness in a wide range of control and logic replacement applications.

- Software Compatible with F8 Family
- 2048 Byte Mask Programmable ROM
- 64 Byte Scratchpad RAM
- 32 Bits (4 Ports) TTL Compatible I/O
- Programmable Binary Timer
 - Interval Timer Mode
 - Pulse Width Measurement Mode
 - Event Counter Mode
- External Interrupt
- Crystal, LC, RC, External, or Internal Time Base
- Low Power (275 mW Typ.)
- Single +5 Volt $\pm 10\%$ Power Supply

MOS

(N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

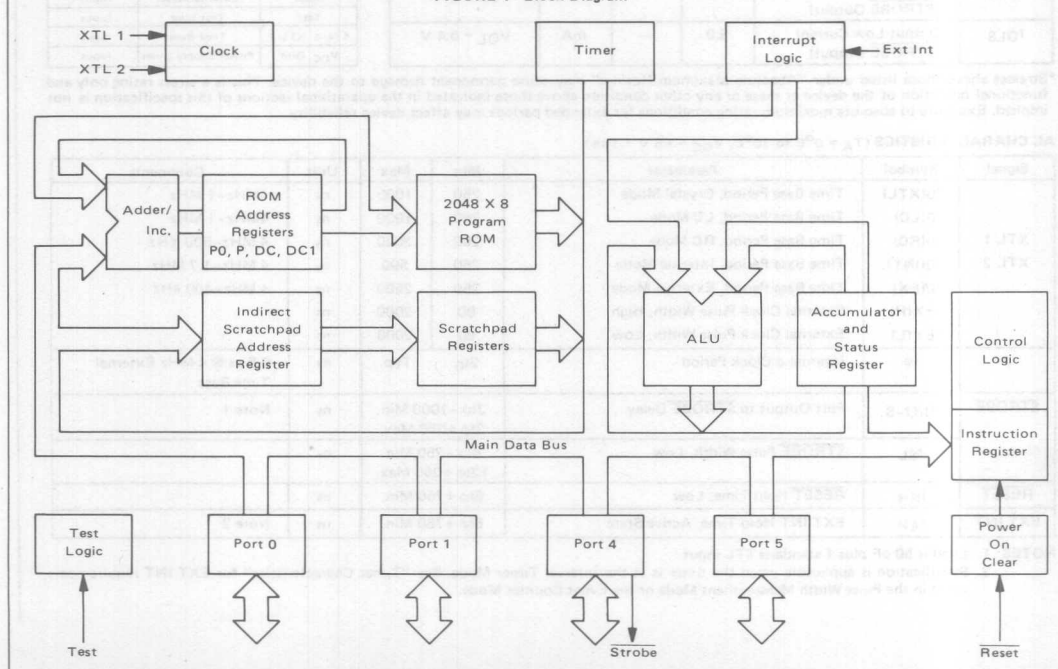
SINGLE-CHIP MICROCONTROLLER



P SUFFIX
PLASTIC PACKAGE
CASE 711

L SUFFIX
CERAMIC PACKAGE
CASE 715
(Available, not shown)

FIGURE 1 - Block Diagram



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MC3870

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias 0°C to 70°C
 Storage Temperature -65°C to +150°C
 Voltage on Any Pin with Respect to Ground -1.0 V to +7 V
 Power Dissipation 1.0 W

DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%)

Symbol	Parameter	Min	Max	Unit	Test Conditions
I _{CC}	Power Supply Current	—	TBD	mA	Outputs Open
P _D	Power Dissipation	—	TBD	mW	Outputs Open
V _{IHEX}	External Clock Input High Level	2.4	5.8	V	
V _{ILEX}	External Clock Input Low Level	-0.3	0.6	V	
I _{IHEX}	External Clock Input High Current	—	100	μA	V _{IHEX} = 2.4 V
I _{ILEX}	External Clock Input Low Current	—	-100	μA	V _{ILEX} = 0.6 V
V _{IH}	Input High Level	2.0	5.8	V	
V _{IL}	Input Low Level	-0.3	0.8	V	
I _{IH}	Input High Current (except open drain and direct drive I/O ports)	—	100	μA	V _{IH} = 2.4 V Internal Pull-up
I _{IL}	Input Low Current (except open drain and direct drive ports)	—	-1.6	mA	V _{IL} = 0.4 V
I _{LOD}	Leakage Current (open drain ports)	—	10	μA	Pulldown Device Off
I _{OH}	Output High Current (except open drain and direct drive ports)	-100	—	μA	V _{OH} = 2.4 V
I _{OHDD}	Output Drive Current (direct drive ports)	-1.5	-8	mA	V _{OH} = 0.7 V to 1.5 V
I _{OL}	Output Low Current	1.8	—	mA	V _{OL} = 0.4 V
I _{OHs}	Output High Current (STROBE Output)	-300	—	μA	V _{OH} = 2.4 V
I _{OLs}	Output Low Current (STROBE Output)	5.0	—	mA	V _{OL} = 0.4 V

PIN CONNECTIONS

XTL 1	1	40	V _{CC}
XTL 2	2	39	RESET
P0-0	3	38	Ext Int
P0-1	4	37	P1-0
P0-2	5	36	P1-1
P0-3	6	35	P1-2
Strobe	7	34	P1-3
P4-0	8	33	P5-0
P4-1	9	32	P5-1
P4-2	10	31	P5-2
P4-3	11	30	P5-3
P4-4	12	29	P5-4
P4-5	13	28	P5-5
P4-6	14	27	P5-6
P4-7	15	26	P5-7
P0-7	16	25	P1-7
P0-6	17	24	P1-6
P0-5	18	23	P1-5
P0-4	19	22	P1-4
Gnd	20	21	Test

Pin Name	Description	Type
P0-0 - P0-7	I/O Port 0	Bidirectional
P1-0 - P1-7	I/O Port 1	Bidirectional
P4-0 - P4-7	I/O Port 4	Bidirectional
P5-0 - P5-7	I/O Port 5	Bidirectional
Strobe	Ready Strobe	Output
Ext Int	External Interrupt	Input
Reset	External Reset	Input
Test	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V _{CC} , Gnd	Power Supply Lines	Input

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5 V ± 10%)

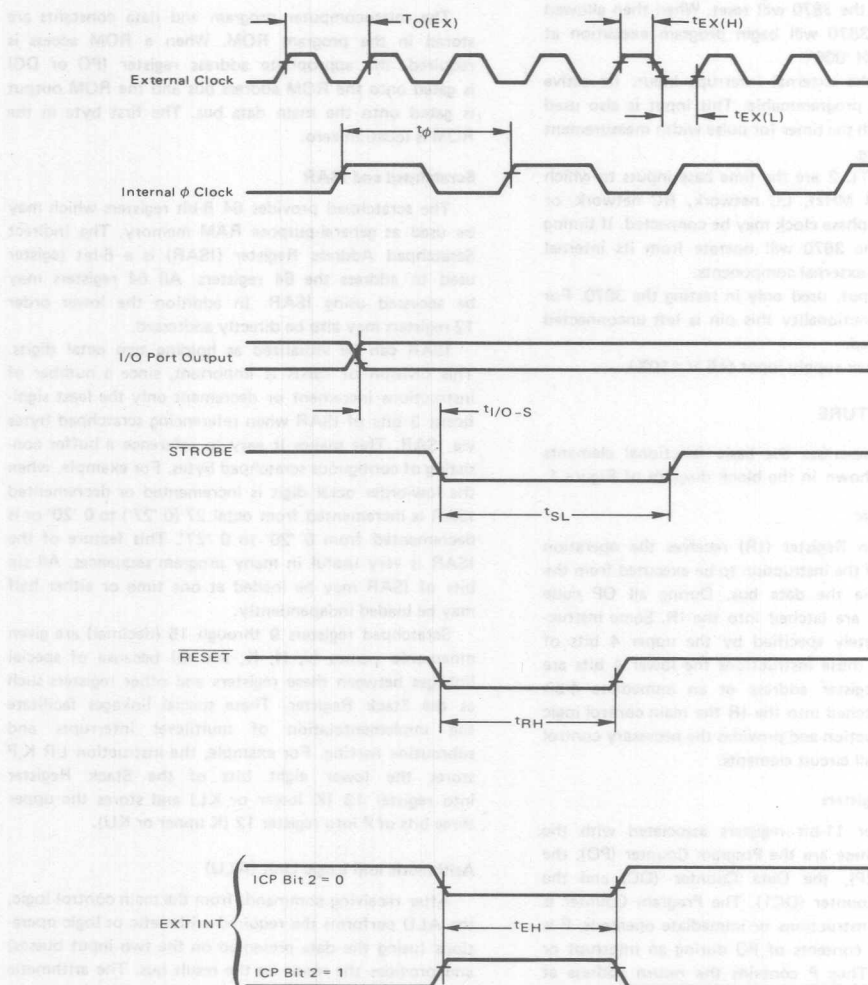
Signal	Symbol	Parameter	Min	Max	Unit	Comments
XTL 1 XTL 2	t ₀ (XTL)	Time Base Period, Crystal Mode	250	1000	ns	4MHz - 1 MHz
	t ₀ (LC)	Time Base Period, LC Mode	250	1000	ns	4MHz - 1 MHz
	t ₀ (RC)	Time Base Period, RC Mode	250	2000	ns	4 MHz - 500 KHz
	t ₀ (INT)	Time Base Period, Internal Mode	250	590	ns	4 MHz - 1.7 MHz
	t ₀ (EX)	Time Base Period, External Mode	250	2500	ns	4 MHz - 400 kHz
	t _{EX} (H)	External Clock Pulse Width, High	90	2000	ns	
	t _{EX} (L)	External Clock Pulse Width, Low	90	2000	ns	
φ	t _φ	Internal φ Clock Period	2t ₀	Typ.	ns	0.5 μs @ 4 MHz External Time Base
STROBE	t _{I/O-S}	Port Output to STROBE Delay	3t _φ - 1000 Min. 3t _φ + 250 Max.		ns	Note 1
	t _{SL}	STROBE Pulse Width, Low	8t _φ - 250 Min. 12t _φ + 250 Max.		ns	
RESET	t _{RH}	RESET Hold Time, Low	6t _φ + 750 Min.		ns	
EXT INT	t _{EH}	EXT INT Hold Time, Active State	6t _φ + 750 Min.		ns	Note 2

NOTES: 1. Load is 50 pF plus 1 standard TTL input.
 2. Specification is applicable when the timer is in the Interval Timer Mode. See "Timer Characteristics" for EXT INT requirements when in the Pulse Width Measurement Mode or the Event Counter Mode.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 2\text{ MHz}$)

Symbol	Parameter	Min	Max	Unit	Test Condition
C_{IN}	Input Capacitance: I/O Ports, RESET, EXT INT	—	7.0	pF	Unmeasured pins returned to GND
C_{XTL}	Input Capacitance: XTL 1, XTL 2	18	23	pF	

AC TIMING DIAGRAMS

NOTE: All measurements are referenced to $V_{IL\text{ max.}}$, $V_{IH\text{ min.}}$, $V_{OL\text{ max.}}$, or $V_{OH\text{ min.}}$.

FUNCTIONAL PIN DESCRIPTION

$\overline{P0-0}-\overline{P0-7}$, $\overline{P1-0}-\overline{P1-7}$, $\overline{P4-0}-\overline{P4-7}$, and $\overline{P5-0}-\overline{P5-7}$ are 32 lines which can be individually used as either TTL compatible inputs or as latched outputs.

STROBE is a ready strobe associated with I/O Port 4. This pin which is normally high provides a single low pulse after valid data is present on the $\overline{P4-0}-\overline{P4-7}$ pins during an output instruction.

RESET may be used to externally reset the 3870. When pulled low the 3870 will reset. When then allowed to go high the 3870 will begin program execution at program location H '000'.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and **XTL 2** are the time base inputs to which a crystal (1 to 4 MHz), LC network, RC network, or an external single-phase clock may be connected. If timing is not critical, the 3870 will operate from its internal oscillator with no external components.

TEST is an input, used only in testing the 3870. For normal circuit functionality this pin is left unconnected or may be grounded.

VCC is the power supply input (+5 V $\pm 10\%$).

3870 ARCHITECTURE

This section describes the basic functional elements of the 3870 as shown in the block diagram of Figure 1.

Main Control Logic

The instruction Register (IR) receives the operation code (OP code) of the instruction to be executed from the program ROM via the data bus. During all OP code fetches eight bits are latched into the IR. Some instructions are completely specified by the upper 4 bits of the OP code. In those instructions the lower 4 bits are an immediate register address or an immediate 4-bit operand. Once latched into the IR the main control logic decodes the instruction and provides the necessary control gating signals to all circuit elements.

ROM Address Registers

There are four 11-bit registers associated with the 2K x 8 ROM. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC) and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. P is used to save the contents of PO during an interrupt or subroutine call. Thus P contains the return address at which processing is to resume upon completion of the subroutine or the interrupt routine.

The Data Counter (DC) is used to address data tables. This register is auto-incrementing. Of the two data

counters only DC can access the ROM. However, the XDC instruction allows DC and DC1 to be exchanged.

Associated with the address registers is an 11-bit Adder/Incrementer. This logic element is used to increment PO or DC when required and is also used to add displacements to PO on relative branches or to add the data bus contents to DC in the ADC (add data counter) instruction.

2048 X 8 ROM

The microcomputer program and data constants are stored in the program ROM. When a ROM access is required, the appropriate address register (PO or DC) is gated onto the ROM address bus and the ROM output is gated onto the main data bus. The first byte in the ROM is location zero.

Scratchpad and ISAR

The scratchpad provides 64 8-bit registers which may be used as general-purpose RAM memory. The Indirect Scratchpad Address Register (ISAR) is a 6-bit register used to address the 64 registers. All 64 registers may be accessed using ISAR. In addition the lower order 12 registers may also be directly addressed.

ISAR can be visualized as holding two octal digits. This division of ISAR is important, since a number of instructions increment or decrement only the least significant 3 bits of ISAR when referencing scratchpad bytes via ISAR. This makes it easy to reference a buffer consisting of contiguous scratchpad bytes. For example, when the low-order octal digit is incremented or decremented ISAR is incremented from octal 27 (0 '27') to 0 '20' or is decremented from 0 '20' to 0 '27'. This feature of the ISAR is very useful in many program sequences. All six bits of ISAR may be loaded at one time or either half may be loaded independently.

Scratchpad registers 9 through 15 (decimal) are given mnemonic names (J, H, K, and Q) because of special linkages between these registers and other registers such as the Stack Register. These special linkages facilitate the implementation of multilevel interrupts and subroutine nesting. For example, the instruction LR K,P' stores the lower eight bits of the Stack Register into register 13 (K lower or KL) and stores the upper three bits of P into register 12 (K upper or KU).

Arithmetic and Logic Unit (ALU)

After receiving commands from the main control logic, the ALU performs the required arithmetic or logic operations (using the data presented on the two input busses) and provides the result on the result bus. The arithmetic operations that can be performed in the ALU are binary add, decimal adjust, add with carry, decrement, and increment. The logic operations that can be performed are AND, OR, EXCLUSIVE OR, 1's complement, shift

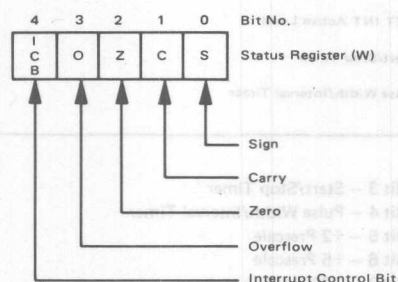
right, and shift left. Besides providing the result on the result bus, the ALU also provides four signals representing the status of the result. These signals, stored in the Status Register (W), represent CARRY, OVERFLOW, SIGN, and ZERO condition of the result of the operation.

Accumulator

The Accumulator (ACC) is the principal register for data manipulation with the 3870. The ACC serves as one input to the ALU for arithmetic or logical operations. The result of ALU operations are stored in the ACC.

The Status Register

The Status Register (also called the W register) holds five status flags as follows.



SUMMARY OF STATUS BITS

$$\text{Overflow} = \text{Carry}_7 \oplus \text{Carry}_6$$

$$\text{Zero} = \overline{\text{ALU}_7 \wedge \text{ALU}_6 \wedge \text{ALU}_5 \wedge \text{ALU}_4 \wedge \text{ALU}_3 \wedge \text{ALU}_2 \wedge \text{ALU}_1 \wedge \text{ALU}_0}$$

$$\text{Carry} = \text{Carry}_7$$

$$\text{Sign} = \text{ALU}_7$$

Interrupt Control Bit

The ICB may be used to allow or disallow interrupts in the 3870. This bit is not the same as the two interrupt enable bits in the Interrupt Control Port (ICP). If the ICB is set and the 3870 interrupt logic communicates an interrupt request to the CPU section, the interrupt will be acknowledged and processed upon completion of the first nonprivileged instruction. If the ICB is cleared, an interrupt request will not be acknowledged or processed until the ICB is set.

I/O Ports

The 3870 provides four complete bidirectional Input/Output ports.

These are ports 0, 1, 4, and 5. In addition, the Interrupt Control Port is addressed as port 6 and the binary timer is addressed as port 7. An output instruction (OUT or OUTS) causes the contents of the ACC to be latched

into the addressed port. An input instruction (IN or INS) transfers the contents of the port to the ACC (port 6 is an exception which is described later). The I/O pins on the 3870 are logically inverted. The schematic of an I/O pin and available output drive options are shown in Figure 2.

FIGURE 2 — I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

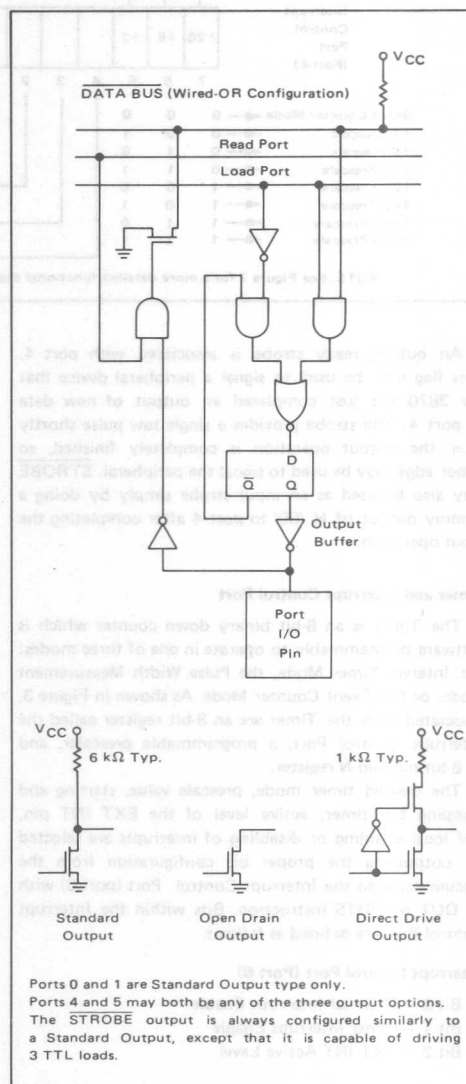
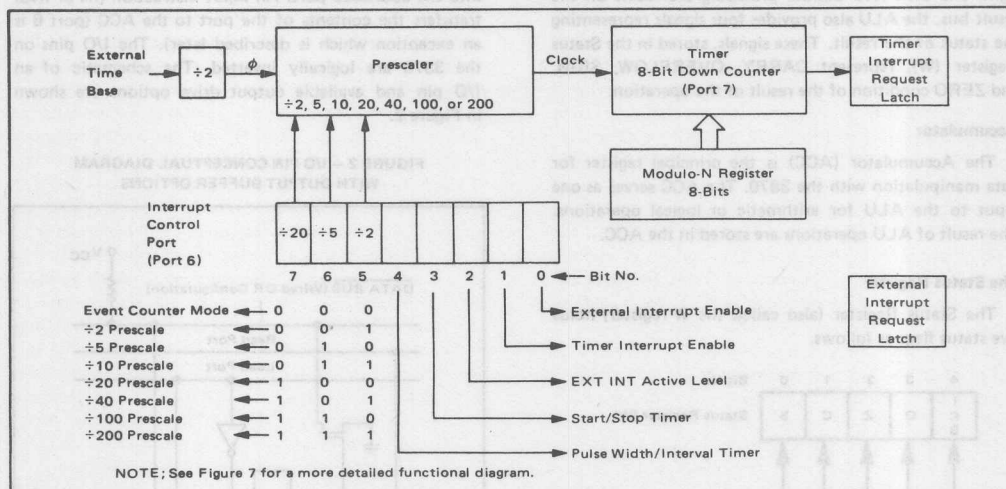


FIGURE 3 – TIMER AND INTERRUPT CONTROL PORT BLOCK DIAGRAM



An output ready strobe is associated with port 4. This flag may be used to signal a peripheral device that the 3870 has just completed an output of new data to port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. STROBE may also be used as an input strobe simply by doing a dummy output of H '00' to port 4 after completing the input operation.

Timer and Interrupt Control Port

The Timer is an 8-bit binary down counter which is software programmable to operate in one of three modes: the Interval Timer Mode, the Pulse Width Measurement Mode, or the Event Counter Mode. As shown in Figure 3, associated with the Timer are an 8-bit register called the Interrupt Control Port, a programmable prescaler, and an 8-bit modulo-N register.

The desired timer mode, prescale value, starting and stopping the timer, active level of the EXT INT pin, and local enabling or disabling of interrupts are selected by outputting the proper bit configuration from the Accumulator to the Interrupt Control Port (port 6) with an OUT or OUTS instruction. Bits within the Interrupt Control Port are defined as follows.

Interrupt Control Port (Port 6)

- Bit 0 – External Interrupt Enable
- Bit 1 – Timer Interrupt Enable
- Bit 2 – EXT INT Active Level

- Bit 3 – Start/Stop Timer
- Bit 4 – Pulse Width/Interval Timer
- Bit 5 – ÷2 Prescale
- Bit 6 – ÷5 Prescale
- Bit 7 – ÷20 Prescale

A special situation exists when reading the Interrupt Control Port (with an IN or INS instruction). The Accumulator is *not* loaded with the content of the ICP. Instead, Accumulator bits 0 through 6 are loaded with 0s, while bit 7 is loaded with the logic level being applied to the EXT INT pin, thus allowing the status of EXT INT to be determined without the necessity of servicing an external interrupt request. This capability is useful in establishing a high-speed polled handshake procedure or for using EXT INT as an extra input pin, if external interrupts are not required and the Timer is used only in the Interval Timer Mode. However, if it is desirable to read the content of the ICP, then one of the 64 scratch-pad registers may be used to save a copy of whatever is written to the ICP.

The rate at which the timer is clocked in the Interval Timer Mode is determined by the frequency of an internal ϕ clock and by the division value selected for the prescaler. (The internal ϕ clock operates at one-half the external time base frequency.) If ICP bit 5 is set and bits 6 and 7 are cleared, the prescaler divides ϕ by 2. Likewise, if bit 6 or 7 is individually set, the prescaler divides ϕ by 5 or 20, respectively. Combinations of bits 5, 6, and 7 may also be selected. For example, if bits 5 and 7 are set while

6 is cleared, the prescaler will divide by 40. Thus, possible prescaler values are: $\div 2$, $\div 5$, $\div 10$, $\div 20$, $\div 40$, $\div 100$, and $\div 200$.

Any of three conditions will cause the prescaler to be reset: Whenever the timer is stopped by clearing ICP bit 3, execution of an output instruction to port 7 (the timer is assigned port address 7), or on the trailing edge transition of the EXT INT pin when in the Pulse Width Measurement Mode. These last two conditions are explained in more detail below.

An OUT or OUTS instruction to port 7 will load the content of the Accumulator to both the Timer and the 8-bit modulo-N register, reset the prescaler, and clear any previously stored time interrupt request. As previously noted, the Timer is an 8-bit down counter which is clocked by the prescaler in the Interval Timer Mode and in the Pulse Width Measurement Mode. The prescaler is not used in the Event Counter Mode. The modulo-N register is a buffer whose function is to save the value which was most recently outputted to port 7. The modulo-N register is used in all three timer modes.

Interval Timer Mode

When ICP bit 4 is cleared (logic 0) and at least one prescale bit is set, the Timer operates in the Interval

Timer Mode. When bit 3 of the ICP is set, the Timer will start counting down from the modulo-N value. After counting down to H '01', the Timer returns to the modulo-N value at the next count. On the transition from H '01' to H 'N' the Timer sets a timer interrupt request latch. Note that the interrupt request latch is set by the transition to H 'N' and not by the presence of H 'N' in the Timer, thus allowing a full 256 counts, if the modulo-N register is preset to H '00'. If bit 1 of the ICP is set, the interrupt request is passed on to the CPU section of the 3870. However, if bit 1 of the ICP is a logic 0, the interrupt request is not passed on to the CPU section, but the interrupt request latch remains set. If ICP bit 1 is subsequently set, the interrupt request will then be passed on to the CPU section. (Recall from the discussion of the Status Register's Interrupt Control Bit that the interrupt request will be acknowledged by the CPU section only if ICB is set.) Only two events can reset the timer interrupt request latch: When the timer interrupt request is acknowledged by the CPU section, or when a new load of the modulo-N register is performed.

Consider an example in which the modulo-N register is loaded with H '64' (decimal 100). The timer interrupt request latch will be set at the 100th count following the timer start and the timer interrupt request latch will

TIMER CHARACTERISTICS

Definitions:

Error = Indicated Time Value — Actual Time Value
 $tpsc = \phi \times \text{Prescale Value}$

Interval Timer Mode:

Single interval error, free running (Note 3) $\pm 6tp\phi$
 Cumulative interval error, free running (Note 3) 0
 Error between two Timer reads (Note 2) $\pm (tpsc + t\phi)$
 Start Timer to stop Timer error (Notes 1, 4) $+t\phi$ to $-(tpsc + t\phi)$
 Start Timer to read Timer error (Notes 1, 2) $-5t\phi$ to $-(tpsc + 7t\phi)$
 Start Timer to interrupt request error (Notes 1, 3) $-2t\phi$ to $-8t\phi$
 Load Timer to stop Timer error (Note 1) $+t\phi$ to $-(tpsc + 2t\phi)$
 Load Timer to read Timer error (Notes 1, 2) $-5t\phi$ to $-(tpsc + 8t\phi)$
 Load Timer to interrupt request error (Notes 1, 3) $-2t\phi$ to $-9t\phi$

Pulse Width Measurement Mode:

Measurement accuracy (Note 4) $+t\phi$ to $-(tpsc + 2t\phi)$
 Minimum pulse width of EXT INT pin $.2t\phi$

Event Counter Mode:

Minimum active time of EXT INT pin $.2t\phi$
 Minimum inactive time of EXT INT pin $.2t\phi$

Notes:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse, if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative, if operation is repetitively performed.

repeatedly be set on precise 100-count intervals. If the prescaler is set at $\div 40$, the timer interrupt request latch will be set every 4000 ϕ clock periods. For a 2 MHz ϕ clock (4 MHz time base frequency) this will produce 2 ms intervals.

The range of possible intervals is from 2 to 51,200 ϕ clock periods (1 μ s to 25.6 ms for a 2 MHz ϕ clock). However, approximately 50 ϕ periods is a practical minimum because the time between setting the interrupt request latch and the execution of the first instruction of the interrupt service routine is at least 29 ϕ periods. (The response time is dependent upon how many privileged instructions are encountered when the request occurs.) To establish time intervals greater than 51,200 ϕ clock periods is a simple matter of using the timer interrupt service routine to count the number of interrupts, saving the result in one or more of the scratchpad registers until the desired interval is achieved. With this technique virtually any time interval, or several time intervals may be generated.

The Timer may be read at any time and in any mode using an input instruction (IN 7 or INS 7) and may take place "on the fly" without interfering with normal timer operation. Also, the Timer may be stopped at any time by clearing bit 3 of the ICP. The Timer will hold its current contents indefinitely and will resume counting when bit 3 is again set. Recall, however, that the prescaler is reset whenever the Timer is stopped; thus, a series of starting and stoppings will result in a cumulative truncation error.

A summary of other timer errors is given in the timing section of this specification. For a free-running timer in the Interval Timer Mode the time interval between any two interrupt requests may be in error by $\pm 6 \phi$ clock periods, although the cumulative error over many intervals is zero. The prescaler and Timer generate precise intervals for setting the timer interrupt request latch, but the time out may occur at any time within a machine cycle. (There are two types of machine cycles: short cycles which consist of 4 ϕ clock periods and long cycles which consist of 6 ϕ clock periods. In the multichip F8 family, there is a signal called the WRITE clock which corresponds to a machine cycle.) Interrupt requests are synchronized with the internal WRITE clock, thus giving rise to the possible $\pm 6 \phi$ error. Additional errors may arise due to the interrupt request occurring while a privileged instruction or multicycle instruction is being executed. Nevertheless, for most applications, all of the above errors are negligible, especially if the desired time interval is greater than 1 ms.

Pulse Width Measurement Mode

When ICP bit 4 is set (logic 1) and at least one prescale bit is set, the Timer operates in the Pulse Width Measurement Mode. This mode is used for accurately measuring

the duration of a pulse applied to the EXT INT pin. The Timer is stopped and the prescaler is reset whenever EXT INT is at its inactive level. The active level of EXT INT is defined by ICP bit 2: if cleared, EXT INT is active low; if set, EXT INT is active high. If ICP bit 3 is set, the prescaler and Timer will start counting when EXT INT transitions to the active level. When EXT INT returns to the inactive level, the Timer then stops, the prescaler resets, and—if ICP bit 0 is set—an external interrupt request latch is set. (Unlike timer interrupts, external interrupts are not latched, if the ICP Interrupt Enable bit is not set.)

As in the Interval Timer Mode, the Timer may be read at any time; may be stopped at any time by clearing ICP bit 3, the prescaler, and ICP bit 1 function as previously described; and, the Timer still functions as an 8-bit binary down counter with the timer interrupt request latch being set on the Timer's transition from H '01' to H 'N'. Note that the EXT INT pin has nothing to do with loading the Timer; its action is that of automatically starting and stopping the Timer and of generating external interrupts. Pulse widths longer than the prescale value times the modulo-N value are easily measured by using the timer interrupt service routine to store the number of timer interrupts in one or more scratchpad registers.

As for accuracy, the actual pulse duration is typically slightly longer than the measured value because the status of the prescaler is not readable and is reset when the Timer is stopped. Thus, for maximum accuracy, it is advisable to use a small division setting for the prescaler.

Event Counter Mode

When ICP bit 4 is cleared and all prescale bits (ICP bits 5, 6, and 7) are cleared, the Timer operates in the Event Counter Mode. This mode is used for counting pulses applied to the EXT INT pin. If ICP bit 3 is set, the Timer will decrement on each transition from the inactive level to the active level of the EXT INT pin. The prescaler is not used in this mode. But, as in the other two timer modes, the Timer may be read at any time; may be stopped at any time by clearing ICP bit 3, ICP bit 1 functions as previously described; and, the timer interrupt request latch is set on the Timer's transition from H '01' to H 'N'.

Normally, ICP bit 0 should be kept cleared in the Event Counter Mode; otherwise, external interrupts will be generated on the transition from the inactive level to the active level of the EXT INT pin.

For the Event Counter Mode, the minimum pulse width required on EXT INT is 2 ϕ clock periods and the minimum inactive time is 2 ϕ clock periods; therefore, the maximum repetition rate is 500 KHz.

External Interrupts

When the timer is in the Interval Timer Mode, the

EXT INT pin is available for nontimer-related interrupts. If ICP bit 0 is set, an external interrupt request latch is set when there is a transition from the inactive level to the active level of EXT INT. (EXT INT is an edge-triggered input.) The interrupt request is latched either until acknowledged by the CPU section or until ICP bit 0 is cleared (unlike timer interrupt requests which remain latched even when ICP bit 1 is cleared). External interrupts are handled in the same fashion when the Timer is in the Pulse Width Measurement Mode or in the Event Counter Mode—except that only in the Pulse Width Measurement Mode the external interrupt request latch is set on the trailing edge of EXT INT, that is, on the transition from the active level to the inactive level.

Interrupt Handling

When either a timer or an external interrupt request is communicated to the CPU section of the 3870, it will be acknowledged and processed at the completion of the first nonprivileged instruction, if the Interrupt Control Bit of the Status Register is set. If the Interrupt Control Bit is not set, the interrupt request will continue until either the Interrupt Control Bit is set and the CPU section acknowledges the interrupt, or until the interrupt request is cleared as previously described.

If there is both a timer interrupt request and an external interrupt request when the CPU section starts to process the requests, the timer interrupt is handled first.

When an interrupt is allowed, the CPU section will request that the interrupting element pass its interrupt vector address to the Program Counter via the data bus. The vector address for a timer interrupt is H '020'. The vector address for external interrupts is H '0A0'. After the vector address is passed to the Program Counter, the CPU section sends an acknowledge signal to the appropriate interrupt request latch which clears that latch. The execution of the interrupt service routine will then commence. The return address of the original program is automatically saved in the Stack Register, P.

Power-On Clear

When power is applied to the 3870, the Program Counter and the ICB bit of the W Status Register are cleared. Ports 4, 5, 6, and 7 are loaded with H '00' (thus the I/O pins for ports 4 and 5 are at +V unless external circuitry is forcing the pins to GND). The contents of other registers and ports are undefined. The first program instruction is then fetched from ROM location H '000'.

External Reset

When $\overline{\text{RESET}}$ is taken low, the content of the Program Counter is pushed to the Stack Register and then the Program Counter and the ICB bit of the W Status Register are cleared. The original Stack Register content is lost.

As with power-on clear, ports 4, 5, 6, and 7 are loaded with H '00'. The contents of all other registers and ports are unchanged. When $\overline{\text{RESET}}$ is taken high, the first program instruction is fetched from ROM location H '000'.

Test Logic

Special test logic is implemented to allow access to the internal main data bus for test purposes.

In normal operation the TEST pin is unconnected or is connected to GND. When TEST is placed at a TTL level (2.0 V to 2.6 V), port 4 becomes an output of the internal data bus and port 5 becomes a wired-OR input to the internal data bus. The data appearing on the port 4 pins is logically true, whereas input data forced on port 5 must be logically false. When TEST is placed at a high level (6.0 V to 7.0 V), the ports act as above and, additionally, the 2K x 8 program ROM is prevented from driving the data bus. In this mode, operands and instructions may be forced externally through port 5 instead of being accessed from the program ROM. When TEST is in either the TTL state or the high state, STROBE ceases its normal function and becomes a machine cycle clock (identical to the F8 multichip system WRITE clock, except inverted).

Timing complexities render the capabilities associated with the TEST pin impractical for use in a user's application, but these capabilities are thoroughly sufficient to enable Motorola to rapidly test the MC3870.

3870 Clocks

The time base for the 3870 may originate from one of five sources. There are four external modes and one internal mode.

If both XTL 1 and XTL 2 are grounded, the 3870 will activate its internal oscillator.

The four external configurations are shown in Figure 4. There is an internal 20 pF capacitor between XTL 1 and GND and an internal 20 pF capacitor between XTL 2 and GND. Thus, external capacitors are not required. In all external clock modes, the external time base frequency is divided by two to form the internal ϕ clock.

INSTRUCTION SET

The MC3870 executes the entire instruction set of the multichip F8 family. Of course, the STORE instruction is of little use in the 3870 because only Read-Only Memory exists in the addressing range of the Data Counter (the Data Counter will, however, be incremented if a STORE is executed).

A summary of programmable registers and ports is given in Figure 5, followed by a summary of the F8 instruction set.

Also, for convenient reference, a Programming Model of the 3870 is given in Figure 6.

SUPPLEMENTARY NOTES

The Interrupt Control Bit of the W Status Register is automatically reset when an interrupt request is acknowledged. It is then the programmer's responsibility to determine when ICB will again be set (by executing an EI instruction). This action prevents an interrupt service routine from being interrupted unless the programmer so desires.

When reading the Interrupt Control Port (port 6), bit 7 of the Accumulator is loaded with the actual logic level being applied to the EXT INT pin, regardless of the status of ICP bit 2 (the EXT INT Active Level bit). That is, if EXT INT is at +5 V, bit 7 of the Accumulator is set to a logic 1; but, if EXT INT is at GND, then Accumulator bit 7 is reset to logic 0.

In the MC3870 (F8 COMPATIBLE) INSTRUCTION SET summary, the number of cycles shown are "nominal" machine cycles. A nominal machine cycle is defined as 4 ϕ clock periods, thus requiring 2 μ s for a 2 MHz ϕ clock frequency (4 MHz external time base frequency).

Also, the summary uses an older nomenclature for register names. The translation is as follows:

PC0 = P0	Program counter
PC1 = P	Stack Register
DC0 = DC	Data Counter
DC1 = DC1	Auxiliary Data Counter

EXT INT pin is available for non-time-related interrupt. If ICB bit 0 is set, an external interrupt request is set when there is a transition from the inactive level to the active level of EXT INT. EXT INT is normally assigned to the active level of the interrupt request is loaded with logic 1.

The nomenclature is used in order to be consistent with the assembly language mnemonics.

For the MC3870, execution of an INS or OUTS instruction requires 2 machine cycles for ports 0 and 1, whereas ports 4 and 5 require 4 machine cycles.

When an external reset of the MC3870 occurs, P0 is pushed into P and the old contents of P are lost. It must be noted that an external reset is recognized at the start of a machine cycle and not necessarily at the end of an instruction. Thus, if the MC3870 is executing a multi-cycle instruction, that instruction is not completed and the contents of P upon reset may not necessarily be the address of the instruction that would have been executed next. It may, for example, point to an immediate operand if the reset occurred during the second cycle of an LI or CI instruction. Additionally, several instructions (JMP, PI, PK, LR P0,Q), as well as the interrupt acknowledge sequence, modify P0 in parts. That is, they alter P0 by first loading one part, then the other, and the entire operation takes more than one cycle. Should reset occur during this modification process, the value pushed into P will be part of the old P0 (the as yet unmodified part) and part of the new P0 (already modified part). Thus care should be taken (perhaps by external gating) to insure that reset does not occur at an undesirable time, if any significance is to be given to the contents of P after a reset occurs.

The vector address for a time interrupt is H 000. After the vector address is pushed to the Program Counter, the CPU section sends an acknowledge signal to the interrupt request input which clears that input. The prime interrupt request input which clears that input. The instruction in the interrupt service routine will then be executed. The return address to the original program is automatically loaded in the Stack Register.

Power-On Clear

When power is applied to the MC3870, the Program Counter and the ICB bit of the W Status Register are cleared. Ports 0, 1, 4, 5, and 6 are loaded with H 000. The I/O pins for ports 2 and 3 are at +5 V unless externally connected to GND. The contents of all other registers and ports are unchanged. The first program instruction is then fetched from ROM location H 000.

Hardware Reset

When RESET is taken low, the contents of the Program Counter is pushed to the Stack Register and then the Program Counter and the ICB bit of the W Status Register are cleared. The original Stack Register content is lost.

FIGURE 4 – CLOCK CONFIGURATIONS

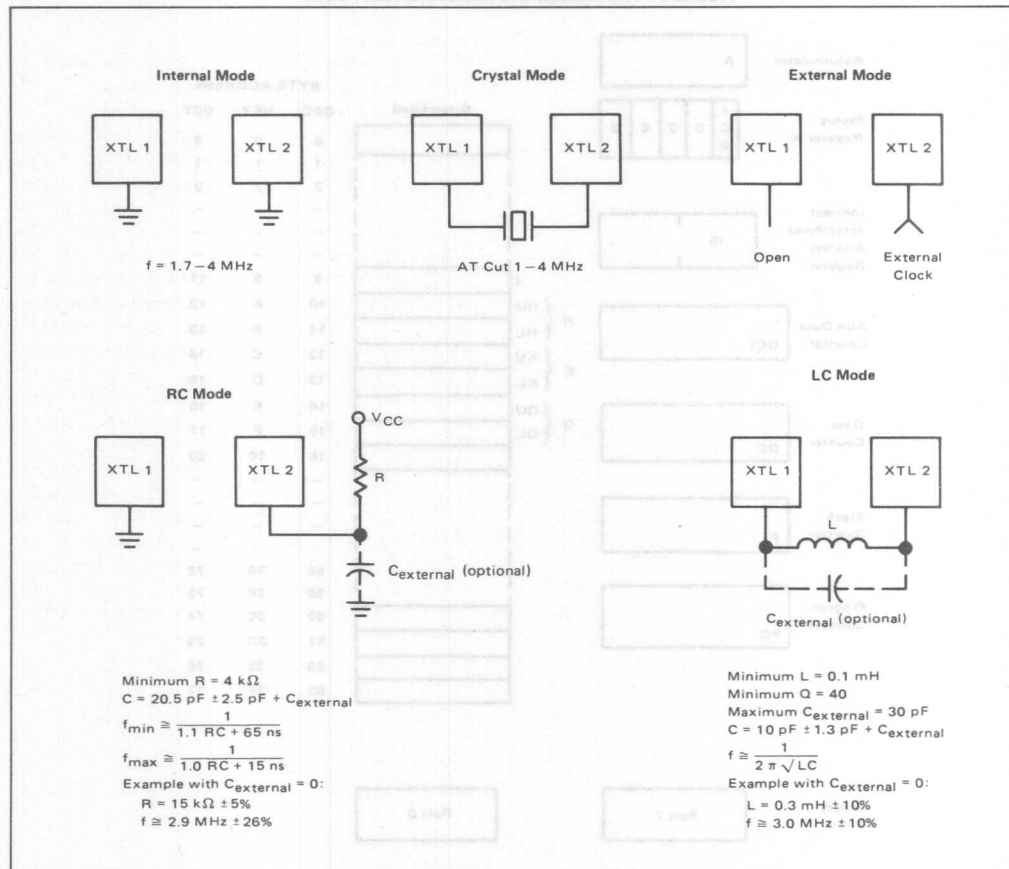
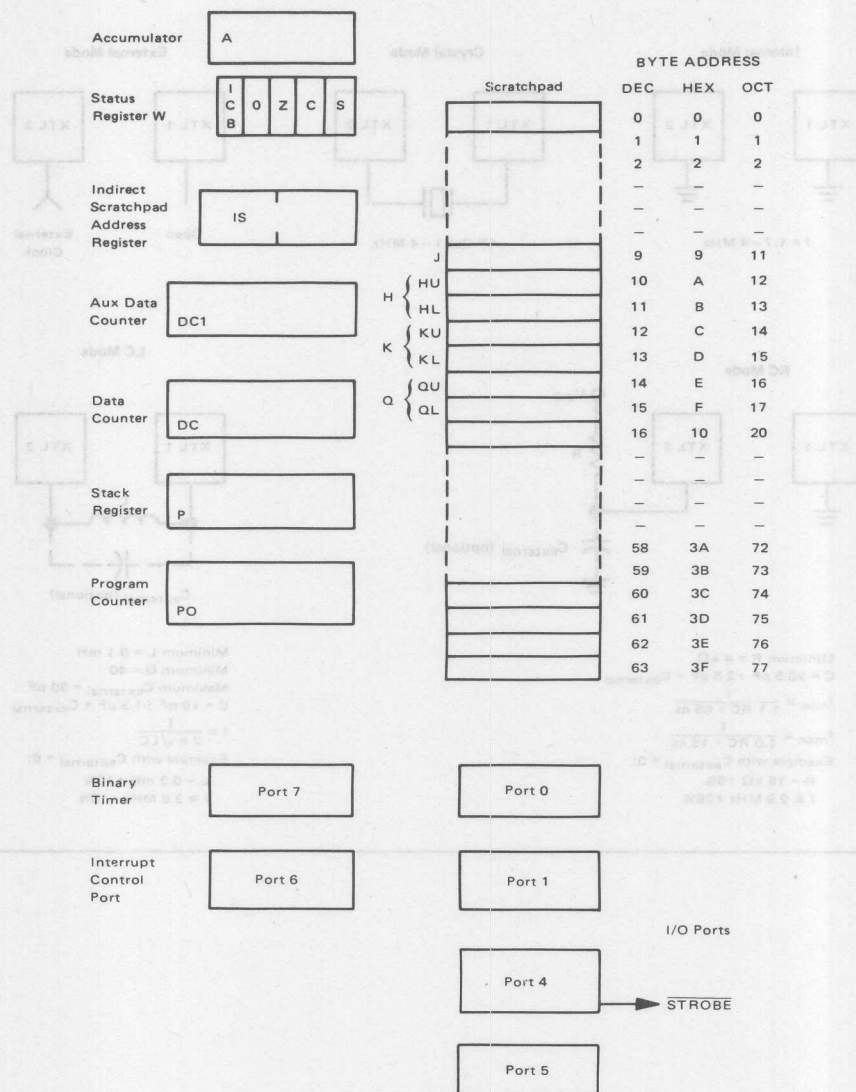


FIGURE 5 - PROGRAMMABLE REGISTERS AND PORTS



MC3870 INSTRUCTION SET
(F8 COMPATIBLE)

ACCUMULATOR GROUP INSTRUCTIONS

Operation	Mnemonic		Function	Machine				Status Bits		
	Op Code	Operand		Code	Bytes	Cycles	OVF	ZERO	CRY	SIGN
ADD CARRY	LNK		$ACC \leftarrow (ACC) + CRY$	19	1	1	1/0	1/0	1/0	1/0
ADD IMMEDIATE	AI	ii	$ACC \leftarrow (ACC) + H'ii'$	24ii	2	2.5	1/0	1/0	1/0	1/0
AND IMMEDIATE	NI	ii	$ACC \leftarrow (ACC) \wedge H'ii'$	21ii	2	2.5	0	1/0	0	1/0
CLEAR	CLR		$ACC \leftarrow H'00'$	70	1	1	—	—	—	—
COMPARE IMMEDIATE	CI	ii	$H'ii' + (\overline{ACC}) + 1$	25ii	2	2.5	1/0	1/0	1/0	1/0
COMPLEMENT	COM		$ACC \leftarrow (ACC) \oplus H'FF'$	18	1	1	0	1/0	0	1/0
EXCLUSIVE OR IMMEDIATE	XI	ii	$ACC \leftarrow (ACC) \oplus H'ii'$	23ii	2	2.5	0	1/0	0	1/0
INCREMENT	INC		$ACC \leftarrow (ACC) + 1$	1F	1	1	1/0	1/0	1/0	1/0
LOAD IMMEDIATE	LI	ii	$ACC \leftarrow H'ii'$	20ii	2	2.5	—	—	—	—
LOAD IMMEDIATE SHORT	LIS	i	$ACC \leftarrow H'0i'$	7i	1	1	—	—	—	—
OR IMMEDIATE	OI	ii	$ACC \leftarrow (ACC) \vee H'ii'$	22ii	2	2.5	0	1/0	0	1/0
SHIFT LEFT ONE	SL	1	SHIFT LEFT 1	13	1	1	0	1/0	0	1/0
SHIFT LEFT FOUR	SL	4	SHIFT LEFT 4	15	1	1	0	1/0	0	1/0
SHIFT RIGHT ONE	SR	1	SHIFT RIGHT 1	12	1	1	0	1/0	0	1
SHIFT RIGHT FOUR	SR	4	SHIFT RIGHT 4	14	1	1	0	1/0	0	1

BRANCH INSTRUCTIONS In all conditional branches $PC_0 \leftarrow (PC_0) + 2$ if the test condition is not met. Execution is complete in 3.0 cycles.

Operation	Mnemonic		Function	Machine			Status Bits			
	Op Code	Operand		Code	Bytes	Cycles	OVF	ZERO	CRY	SIGN
BRANCH ON CARRY	BC	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if CRY = 1	82aa	2	3.5	—	—	—	—
BRANCH ON POSITIVE	BP	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if SIGN = 1	81aa	2	3.5	—	—	—	—
BRANCH ON ZERO	BZ	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ZERO = 1	84aa	2	3.5	—	—	—	—
BRANCH ON TRUE	BT	taa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if any test is true	8taa	2	3.5	—	—	—	—

t = TEST CONDITION

2 ²	2 ¹	2 ⁰
ZERO	CRY	SIGN

BRANCH IF NEGATIVE	BM	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if $SIGN = 0$	91aa	2	3.5	—	—	—	—
BRANCH IF NO CARRY	BNC	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if $CRY = 0$	92aa	2	3.5	—	—	—	—
BRANCH IF NO OVERFLOW	BNO	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if $OVF = 0$	98aa	2	3.5	—	—	—	—
BRANCH IF NOT ZERO	BNZ	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if $ZERO = 0$	94aa	2	3.5	—	—	—	—
BRANCH IF FALSE TEST	BF	taa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if all false test bits	9taa	2	3.5	—	—	—	—

t = TEST CONDITION

2 ³	2 ²	2 ¹	2 ⁰
OVF	ZERO	CRY	SIGN

BRANCH IF ISAR (LOWER) $\neq 7$	BR7	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if $ISAR_L \neq 7$	8Faa	2	2.5	—	—	—	—
			$PC_0 \leftarrow (PC_0) + 2$ if $ISAR_L = 7$			2.0	—	—	—	—
BRANCH RELATIVE	BR	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$	90aa	2	3.5	—	—	—	—
JUMP*	JMP	aaaa	$PC_0 \leftarrow H'aaaa'$	29aaaa	3	5.5	—	—	—	—

*Privileged instruction.

MEMORY REFERENCE INSTRUCTIONS In all Memory Reference Instructions, the Data Counter is incremented DC←DC + 1

Operation	Mnemonic		Function	Machine			Status Bits			
	OP Code	Operand		Code	Bytes	Cycles	OVF	ZERO	CRY	SIGN
ADD BINARY	AM		ACC←(ACC) + [(DC)]	88	1	2.5	1/0	1/0	1/0	1/0
ADD DECIMAL	AMD		ACC←(ACC) + [(DC)]	89	1	2.5	1/0	1/0	1/0	1/0
AND	NM		ACC←(ACC) ∧ [(DC)]	8A	1	2.5	0	1/0	0	1/0
COMPARE	CM		[(DC)] + (ACC) + 1	8D	1	2.5	1/0	1/0	1/0	1/0
EXCLUSIVE OR	XM		ACC←(ACC) ⊕ [(DC)]	8C	1	2.5	0	1/0	0	1/0
LOAD	LM		ACC←[(DC)]	16	1	2.5	—	—	—	—
LOGICAL OR	OM		ACC←(ACC) ∨ [(DC)]	8B	1	2.5	0	1/0	0	1/0
STORE	ST		(DC)←(ACC)	17	1	2.5	—	—	—	—

ADDRESS REGISTER GROUP INSTRUCTIONS

Operation	Mnemonic		Function	Machine			Status Bits			
	OP Code	Operand		Code	Bytes	Cycles	OVF	ZERO	CRY	SIGN
ADD to DATA COUNTER	ADC		DC←(DC) + (ACC)	8E	1	2.5	—	—	—	—
CALL to SUBROUTINE*	PK		PC ₀ U←(r12); PC ₀ L←(r13); PC ₁ ←(PC ₀)	0C	1	4	—	—	—	—
CALL to SUBROUTINE IMMEDIATE*	PI	aaaa	PC ₁ ←(PC ₀); PC ₀ ←H'aaaa'	28aaaa	3	6.5	—	—	—	—
EXCHANGE DC	XDC		DC ₀ ↔DC ₁	2C	1	2	—	—	—	—
LOAD DATA COUNTER	LR	DC,Q	DCU←(r14); DCL←(r15)	0F	1	4	—	—	—	—
LOAD DATA COUNTER	LR	DC,H	DCU←(r10); DCL←(r11)	10	1	4	—	—	—	—
LOAD DC IMMEDIATE	DCI	aaaa	DC←H'aaaa'	2Aaaaa	3	6	—	—	—	—
LOAD PROGRAM COUNTER	LR	PO,Q	PC ₀ U←(r14); PC ₀ L←(r15)	0D	1	4	—	—	—	—
LOAD STACK REGISTER	LR	P,K	PC ₁ U←(r12); PC ₁ L←(r13)	09	1	4	—	—	—	—
RETURN FROM SUBROUTINE*	POP		PC ₀ ←(PC ₁)	1C	1	2	—	—	—	—
STORE DATA COUNTER	LR	Q,DC	r14←(DCU); r15←(DCL)	0E	1	4	—	—	—	—
STORE DATA COUNTER	LR	H,DC	r10←(DCU); r11←(DCL)	11	1	4	—	—	—	—
STORE STACK REGISTER	LR	K,P	r12←(PC ₁ U); r13←(PC ₁ L)	08	1	4	—	—	—	—

SCRATCHPAD REGISTER INSTRUCTIONS (Refer to Scratchpad Addressing Modes)

Operation	Mnemonic		Function	Machine			Status Bits			
	OP Code	Operand		Code	Bytes	Cycles	OVF	ZERO	CRY	SIGN
ADD BINARY	AS	r	ACC←(ACC) + (r)	Cr	1	1	1/0	1/0	1/0	1/0
ADD DECIMAL	ASD	r	ACC←(ACC) + (r)	Dr	1	2	1/0	1/0	1/0	1/0
DECREMENT	DS	r	r←(r) + H'FF'	3r	1	1.5	1/0	1/0	1/0	1/0
LOAD	LR	A,r	ACC←(r)	4r	1	1	—	—	—	—
LOAD	LR	A,KU	ACC←(r12)	00	1	1	—	—	—	—
LOAD	LR	A,KL	ACC←(r13)	01	1	1	—	—	—	—
LOAD	LR	A,QU	ACC←(r14)	02	1	1	—	—	—	—
LOAD	LR	A,QL	ACC←(r15)	03	1	1	—	—	—	—
LOAD	LR	r,A	r←(ACC)	5r	1	1	—	—	—	—
LOAD	LR	KU,A	r12←(ACC)	04	1	1	—	—	—	—
LOAD	LR	KL,A	r13←(ACC)	05	1	1	—	—	—	—
LOAD	LR	QU,A	r14←(ACC)	06	1	1	—	—	—	—
LOAD	LR	QL,A	r15←(ACC)	07	1	1	—	—	—	—
AND	NS	r	ACC←(ACC) ∧ (r)	Fr	1	1	0	1/0	0	1/0
EXCLUSIVE OR	XS	r	ACC←(ACC) ⊕ (r)	Er	1	1	0	1/0	0	1/0

*Privileged Instruction.

MISCELLANEOUS INSTRUCTIONS

Operation	Mnemonic		Function	Machine				Status Bits		
	OP Code	Operand		Code	Bytes	Cycles	OVF	ZERO	CRY	SIGN
DISABLE INTERRUPT	DI		RESET ICB	1A	1	2	—	—	—	—
ENABLE INTERRUPT*	EI		SET ICB	1B	1	2	—	—	—	—
INPUT	IN	aa	ACC←(INPUT PORT aa)	26aa	2	4	0	1/0	0	1/0
INPUT SHORT	INS	a	ACC←(INPUT PORT a)	Aa	1	4***	0	1/0	0	1/0
LOAD ISAR	LR	IS,A	ISAR←(ACC)	OB	1	1	—	—	—	—
LOAD ISAR LOWER	LISL	a	ISARL←a	1101a**	1	1	—	—	—	—
LOAD ISAR UPPER	LISU	a	ISARU←a	01100a**	1	1	—	—	—	—
LOAD STATUS REGISTER*	LR	W,J	W←(r9)	1D	1	2	1/0	1/0	1/0	1/0
NO-OPERATION	NOP		PC0←(PC0) + 1	2B	1	1	—	—	—	—
OUTPUT	OUT	aa	OUTPUT PORT aa←(ACC)	27aa	2	4	—	—	—	—
OUTPUT SHORT	OUTS	a	OUTPUT PORT a←(ACC)	8a	1	4***	—	—	—	—
STORE ISAR	LR	A,IS	ACC←(ISAR)	OA	1	1	—	—	—	—
STORE STATUS REG	LR	J,W	r9←(W)	1E	1	1	—	—	—	—

*Privileged Instruction

**3-Bit Octal Digit

***2 Machine Cycles for CPU Ports

NOTES

Each lowercase character represents a Hexadecimal digit.
Each cycle equals 4 machine clock periods.

Lowercase denotes variables specified by programmer.

Function Definitions

—	is replaced by
()	the contents of
(—)	Binary "1's complement of
+	Arithmetic Add (Binary or Decimal)
⊕	Logical OR exclusive
^	Logical AND
∨	Logical OR inclusive
H*	Hexadecimal digit

Register Names

a	Address Variable
A	Accumulator
DC	Data Counter (Indirect Address Register)
DC0	Data Counter #0 (Indirect Address Register #0)
DC1	Data Counter #1 (Indirect Address Register #1)
DCL	Least significant 8 bits of Data Counter Addressed
DCU	Most significant 8 bits of Data Counter Addressed
H	Scratchpad Register #10 and #11
i and ii	Immediate Operand
ICB	Interrupt Control Bit
IS	Indirect Scratchpad Address Register
ISAR	Indirect Scratchpad Address Register
ISARL	Least significant 3 bits of ISAR
ISARU	Most significant 3 bits of ISAR
J	Scratchpad Register #9

K	Registers #12 and #13
KL	Register #13
KU	Register #12
PC0	Program Counter
PC0L	Least significant 8 bits of Program Counter
PC0U	Most significant 8 bits of Program Counter
PC1	Stack Register
PC1L	Least significant 8 bits of Program Counter
PC1U	Most significant 8 bits of Active Stack Register
Q	Registers #14 and #15
QL	Register #15
QU	Register #14
r	Scratchpad Register (any address through 11)
W	Status Register

Scratchpad Addressing Modes (Machine Code Format)

r	C	(Hexadecimal), Register Addressed by ISAR (Unmodified)
r	D	(Hexadecimal), Register Addressed by ISAR, ISARL Incremented
r	E	(Hexadecimal), Register Addressed by ISAR, ISARL Decrement
r	F	(No operation performed)
r	O	(Hexadecimal), Register 0 through 11 addressed directly from the through B Instruction

Status Register

—	No change in condition
1/0	is set to "1" or "0" depending on conditions
CRY	Carry Flag
OVF	Overflow Flag
SIGN	Sign of Result Flag
ZERO	Zero Flag

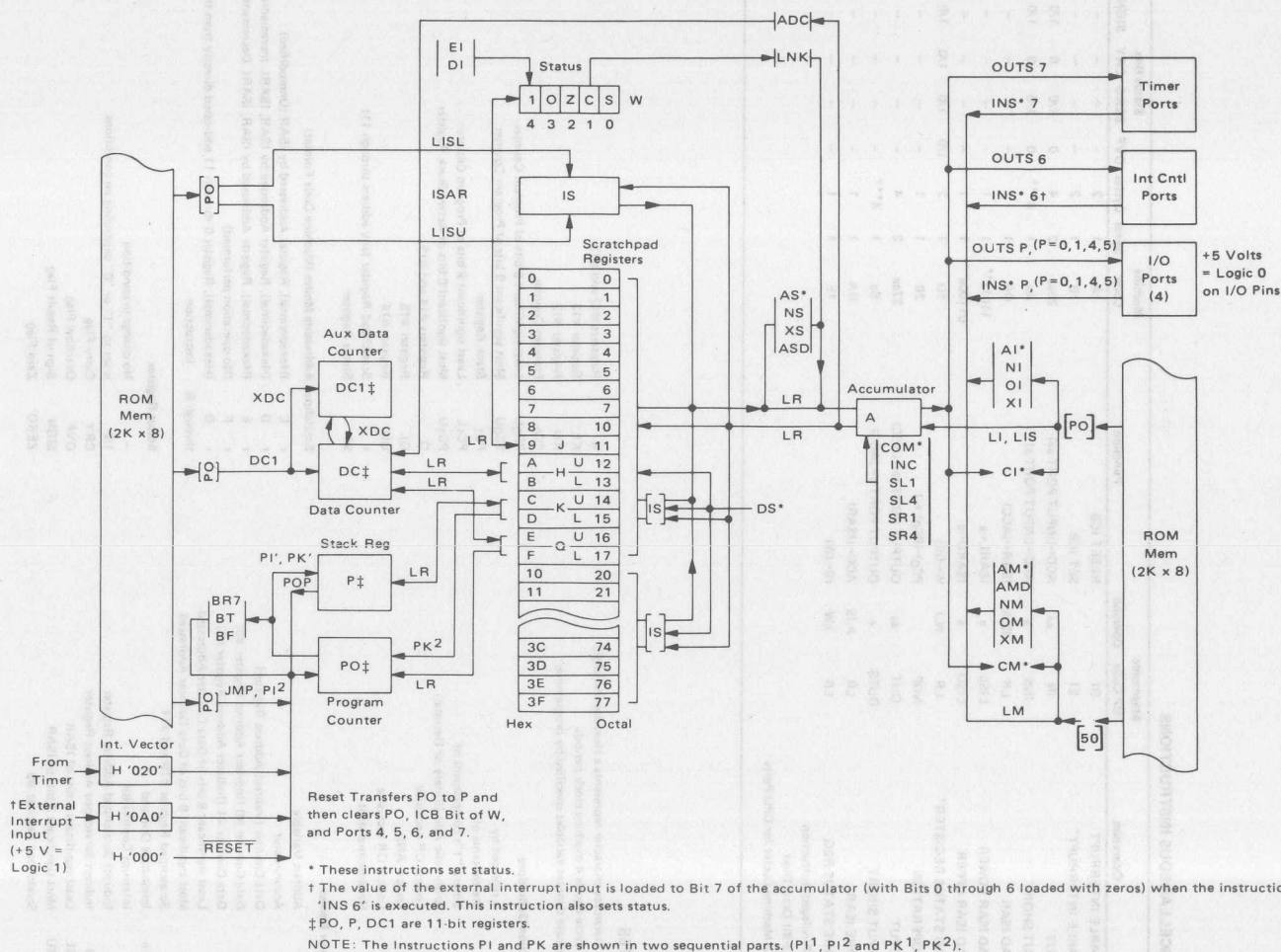


FIGURE 6 - PROGRAMMING MODEL

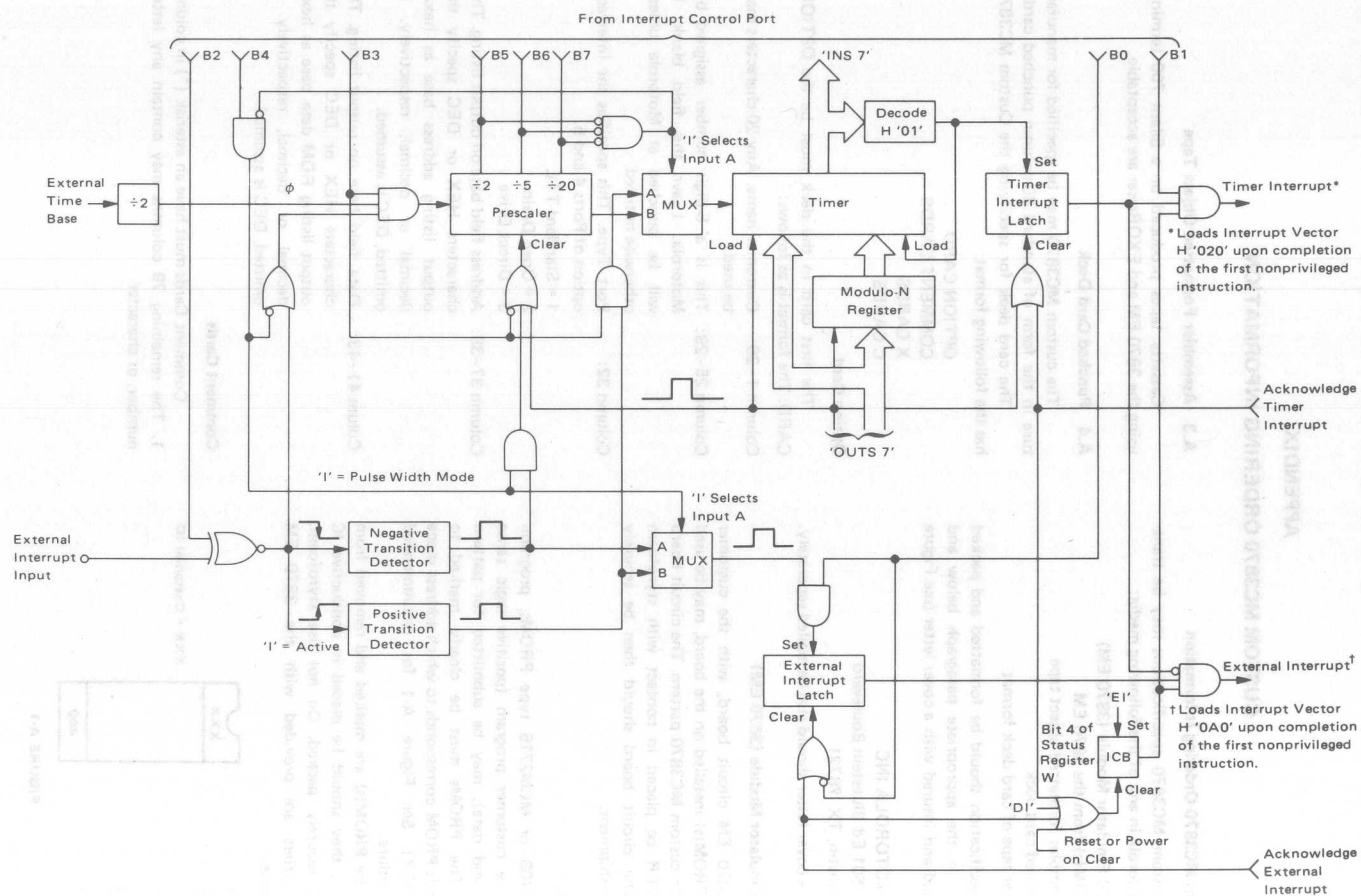


FIGURE 7 - TIMER/INTERRUPT FUNCTIONAL DIAGRAM

APPENDIX

CUSTOM MC3870 ORDERING INFORMATION

A.0 Custom MC3870 Ordering Information

The custom MC3870 specifications may be transmitted to Motorola in any of the following media:

- 1) 3870 Emulator Module (3870 EM)
- 2) PROM(s) from the 3870 EM
- 3) Assembler formatted object tape
- 4) Punched card deck
- 5) Paper tape of card deck format

The specification should be formatted and packed as indicated in the appropriate paragraph below and mailed prepaid and insured with a cover letter (see Figure A-2) to:

MOTOROLA INC.
3501 Ed Bluestein Boulevard
Austin, TX 78721

A copy of the cover letter should also be mailed separately.

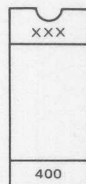
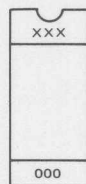
A.1 3870 Emulator Module (3870 EM)

The 3870 EM circuit board, with the customer program in PROM(s) installed on the board, may be used to specify the custom MC3870 pattern. The circuit board should NEVER be placed in contact with styrofoam materials. The circuit board should then be securely packaged for shipment.

A.2 PROMs

MCM2708 or MCM2716 type PROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. The PROMs must be clearly marked to indicate which PROM corresponds to which address space (000-3FF HEX). See Figure A-1 for recommended marking procedure.

After the PROM(s) are marked and removed from the Emulator, they should be placed in conductive IC carriers and securely packed. Do not use styrofoam. Black IC carriers are provided with the 3870 EM for this purpose.



xxx = Customer ID

FIGURE A-1

A.3 Assembler Formatted Object Tape

Cassette tapes produced on a Silent 700 terminal using the 3870 EM and EXORciser are acceptable.

A.4 Punched Card Deck

The custom MC3870 may be specified for manufacture in the form of standard 80-column punched cards.

The card deck for specifying the Custom MC3870 has the following format:

OPTION CARD
COMMENT CARDS
X CARDS
C CARDS

Option Card

The first card in the deck must be the OPTION CARD. The format is as follows:

- Column 1-20: Customer name. Any 20 characters may be used.
- Column 25-29: This is a 5-digit number assigned by Motorola. Leave this field blank. It will be punched at Motorola unless otherwise notified.
- Column 32: Port Type. This specifies the interface option of Ports 4 and 5.
1 = Standard TTL
2 = Open Drain
3 = Direct Drive
- Column 37-39: Address field base on output listing. The characters HEX or DEC specify the output listing address base as hexadecimal or decimal, respectively. If omitted, DEC is assumed.
- Column 41-43: Data field base on output listing. The characters HEX or DEC specify the output listing ROM data base as hexadecimal or decimal, respectively. If omitted, DEC is assumed.

Comment Cards

Comment Cards must have an asterisk (*) in column 1. The remaining 79 columns may contain any letter, number, or character.

X Cards

Five X cards are possible. All X cards have an X in column 1 and one or three or more words each separated by one blank space.

The possibilities are:

- 1) X SEQUENCE
- 2) X BASE DEC DEC
- 3) X BASE DEC HEX
- 4) X BASE HEX DEC
- 5) X BASE HEX HEX

Card 1 specifies that there are sequence numbers on each data card that follows. The sequence numbers must be in columns 77-79 of the data cards (C Cards) and must be in decimal, right justified. The numbers must start with 1 (one) and must be in order. The X SEQUENCE Card may appear anywhere within the deck after the Option Card. If it appears within the data card section, data cards encountered before the X SEQUENCE Card will not be checked for sequence numbers. All following cards will be checked. If no X SEQUENCE Card is used, no sequence numbers will be checked.

It is initially assumed that the address and byte count as well as the data specified on the C Cards will be in decimal. An X BASE Card can be used to override this specification. The second word on the card (that following BASE) specifies the base (either DEC or HEX) of the address and byte count on all following C cards. The last word specifies the base of the data fields on the C Cards. An X BASE card may appear anywhere within the deck following the OPTION Card. It may be overridden by another X BASE Card. All data cards (C Cards) following an X BASE Card will be interpreted as per that X BASE Card unless another X BASE Card is encountered. If no X BASE Cards are used, it is assumed that all fields on the C Cards are in decimal.

NOTE: Once an X SEQUENCE Card is encountered, all successive cards will be checked for the proper sequence number and unlike X BASE Cards this option cannot thereafter be altered by another X SEQUENCE Card.

C Cards

These cards contain the actual ROM data. All fields are right-justified.

Column 1: C (the letter C)

Column 2-9: ADD

Column 10-12: BYTE

Column 14-16: DATA 1

Column 17-19: DATA 2

Column 76-78: DATA 21

Column 77-79: DATA 22 or SEQUENCE NUMBER

ADD is the address of the first byte of data (DATA 1) contained on that card. Byte is the number of bytes of data to be read from that card. BYTE must be greater than zero and less than 23 (1-22) if no sequence numbers are used, and less than 22 (1-21) if sequence numbers are used. If, for example, there are ten data fields punched on the card, but BYTE = 2, only the first two will be read. Also, if there are two punched data fields, for example, and BYTE = 6, six ROM locations will be filled from that card. The four unspecified fields will be decoded as zero. ADD and BYTE are always in the same base (HEX or DECIMAL). DATA 1 through DATA N is the data to be placed in the ROM at addresses ADD through ADD + (N-1), respectively.

Any ROM address not filled as a result of reading data from a C Card will be filled with zero. If a particular location has already been specified by a C Card, but a successive C Card also has the data which is to be placed in that location, the second C Card will override the first.

A.5 Paper Tape of Card Deck Format

Punched Paper tape (ASCII) in the same format as cards can also be accepted. However, your order will be processed faster if the data is in card format. After the tape leader there should be a <CR><LF>. Data records should be a full 80 columns, each terminated by a <CR><LF>. Following the last Data record, there should be one more record with the first three characters being EOF, followed by 77 blanks and a <CR><LF>.

<CR> = Carriage Return

<LF> = Line Feed

CUSTOMER NAME _____	
ADDRESS _____	
CITY _____	STATE _____ ZIP _____
PHONE (____) _____	EXTENSION _____
CONTACT MS/MR _____	
CUSTOMER PART # _____	
PORT OPTION (NOTE 1) <input type="checkbox"/> Standard TTL	
<input type="checkbox"/> Open Drain	
<input type="checkbox"/> Direct Drive	
PATTERN MEDIA <input type="checkbox"/> 3870 EM	
<input type="checkbox"/> 2708 PROM	
<input type="checkbox"/> 2716 PROM	
<input type="checkbox"/> Paper Object Tape	
<input type="checkbox"/> Silent 700 Cassette	
<input type="checkbox"/> Card Deck	
<input type="checkbox"/> Tape of Card Deck	
<input type="checkbox"/> (Note 2) _____	
NOTES: (1) Ports 4 and 5 Only	
(2) Other Media Require Prior Factory Approval	
SIGNATURE _____	
TITLE _____	

FIGURE A-2

MC6805P2

Advance Information

8-BIT MICROCOMPUTER UNIT

The MC6805P2 Microcomputer Unit (MCU) is a member of the M6805 Family of microcomputers. This 8-bit microcomputer contains a CPU, on-chip clock, ROM, RAM, I/O and timer. It is designed for the user who needs an economical microcomputer with the proven capabilities of the M6800-based instruction set. Table 9 compares the key features of the M6805 Family of microcomputers. The following are some of the hardware and software highlights of the MCU.

HARDWARE FEATURES:

- 8-Bit Architecture
- 64 Bytes of RAM
- Memory Mapped I/O
- 1100 Bytes of User ROM
- Internal 8-Bit Timer with 7-Bit Prescaler
- Vectored Interrupts — External and Timer
- 20 TTL/CMOS Compatible I/O Lines; 8 Lines LED Compatible
- On-Chip Clock Circuit
- Self-Check Mode
- Master Reset
- Low Voltage Inhibit
- Complete Development System Support on EXORciser
- 5 Vdc Single Supply

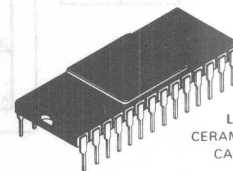
SOFTWARE FEATURES:

- Similar to M6800
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instructions
- Versatile Interrupt Handling
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Branches
- Memory Usable as Registers/Flags
- Single Instruction Memory Examine/Change
- 10 Powerful Addressing Modes
- All Addressing Modes Apply to ROM, RAM and I/O

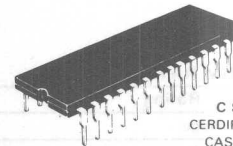
HMOS

(HIGH DENSITY
N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

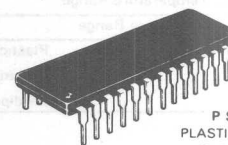
8-BIT MICROCOMPUTER



L SUFFIX
CERAMIC PACKAGE
CASE 719-03



C SUFFIX
CERP PACKAGE
CASE 733-02



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

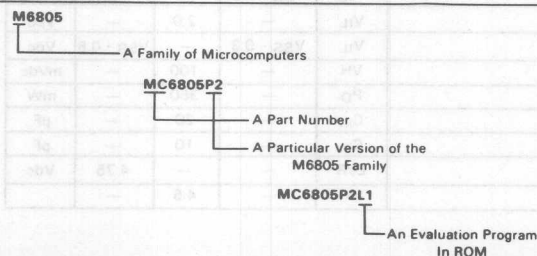


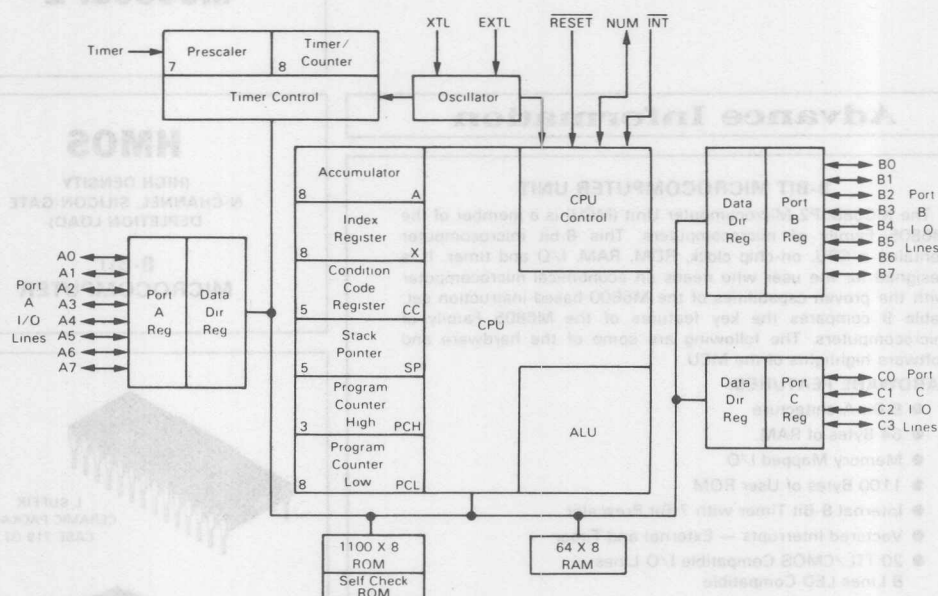
FIGURE 1 — PIN ASSIGNMENTS

1	V _{SS}	RESET	28
2	INT	A7	27
3	V _{CC}	A6	26
4	XTL	A5	25
5	EXTL	A4	24
6	NUM	A3	23
7	TIMER	A2	22
8	CO	A1	22
9	C1	A0	20
10	C2	B7	19
11	C3	B6	18
12	B0	B5	17
13	B1	B4	16
14	B2	B3	15

This is advance information and specifications are subject to change without notice

MC6805P2

FIGURE 2 — MC6805P2 HMOS MICROCOMPUTER BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	Vdc
Input Voltage	V _{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T _A	0 to 70	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Thermal Resistance	θ _{JA}	85	°C/W
		50	
		51	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} (V_{in} or V_{out}) + V_{CC}.

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.25 Vdc, V_{dc}, V_{SS} = GND, T_A = 0 — 70 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	RESET	V _{IH}	4.0	—	V _{CC}	V _{dc}
	INT	V _{IH}	—	2.2	—	V _{dc}
	All Other	V _{IH}	V _{SS} + 2.0	—	V _{CC}	V _{dc}
Input High Voltage Timer	Timer Mode	V _{IH}	V _{SS} + 2.0	—	V _{CC}	V _{dc}
	Self-Check Mode	V _{IH}	—	9.0	15.0	V _{dc}
Input Low Voltage	RESET	V _{IL}	V _{SS} - 0.3	—	0.8	V _{dc}
	INT	V _{IL}	—	2.0	—	V _{dc}
	All Other	V _{IL}	V _{SS} - 0.3	—	V _{SS} + 0.8	V _{dc}
INT Hysteresis		V _H	—	100	—	mV _{dc}
Power Dissipation		P _D	—	350	—	mW
Input Capacitance	EXTL	C _{in}	—	20	—	pF
	All Other	C _{in}	—	10	—	pF
Low Voltage Recover		LVR	—	—	4.75	V _{dc}
Low Voltage Inhibit		LVI	—	4.5	—	

SWITCHING CHARACTERISTICS ($V_{CC} = +5.25 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ - 70^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{cl}	0.4	—	4.0	MHz
Cycle Time	t_{CYC}	1.0	—	10	μs
INT Pulse Width	t_{iWL}	$t_{CYC} + 250$	—	—	ns
RESET Pulse Width	t_{RWL}	$t_{CYC} + 250$	—	—	ns
Delay Time Reset (External Cap. = 0.47 μF)	t_{RHL}	20	50	—	ms

PORT ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.25 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ$ to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A					
Output Low Voltage $I_{load} = 1.6 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output High Voltage $I_{load} = -100 \mu\text{A}$	V_{OH}	2.4	—	—	Vdc
Output High Voltage $I_{load} = -10 \mu\text{A}$	V_{OH}	3.5	—	—	Vdc
Input High Voltage $I_{load} = -300 \mu\text{A}$ (max)	V_{IH}	$V_{SS} + 2.0$	—	V_{CC}	Vdc
Input Low Voltage $I_{load} = -500 \mu\text{A}$ (max)	V_{IL}	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	Vdc
Port B					
Output Low Voltage $I_{load} = 3.2 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output Low Voltage $I_{load} = 10 \text{ mA}$ (sink)	V_{OL}	—	—	1.0	Vdc
Output High Voltage $I_{load} = -200 \mu\text{A}$	V_{OH}	2.4	—	—	Vdc
Darlington Current Drive (Source) $V_O = 1.5 \text{ Vdc}$	I_{OH}	-1.0	—	-10	mA
Input High Voltage	V_{IH}	$V_{SS} + 2.0$	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	Vdc
Port C					
Output Low Voltage $I_{load} = 1.6 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output High Voltage $I_{load} = -100 \mu\text{A}$	V_{OH}	2.4	—	—	Vdc
Input High Voltage	V_{IH}	$V_{SS} + 2.0$	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	Vdc
Off-State Input Current					
Three-State Ports B & C	I_{TSI}	—	2	20	μA
Input Current					
Timer at $V_{in} = (0.4 \text{ to } 2.4 \text{ Vdc})$	I_{in}	—	—	20	μA

FIGURE 3 — TTL EQUIV. TEST LOAD (PORT B)

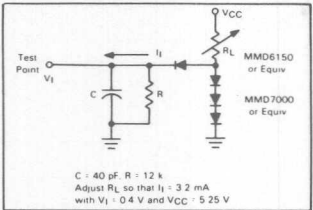


FIGURE 4 — CMOS EQUIV. TEST LOAD (PORT A)

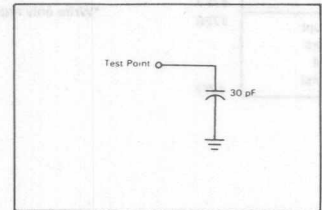
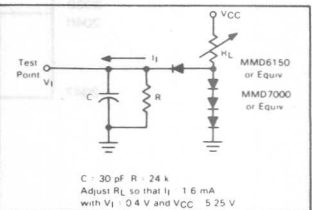


FIGURE 5 — TTL EQUIV. TEST LOAD (PORTS A AND C)



SIGNAL DESCRIPTION

The input and output signals for the MCU shown in Figure 1 are described in the following paragraphs.

V_{CC} AND V_{SS} — Power is supplied to the MCU using these two pins. V_{CC} is +5.25 Vdc ±0.5 V. V_{SS} is the ground connection.

INT — This pin provides the capability for applying an external interrupt to the MCU. Refer to **INTERRUPTS** for additional information.

XTAL AND EXTAL — These pins provide control input for the on-chip clock circuit. A crystal (AT cut, 4 MHz maximum) or a resistor can be connected to these pins to provide the internal oscillator with varying degrees of stability. Refer to **INTERNAL OSCILLATOR OPTIONS** for recommendations about these inputs.

TIMER — This pin allows an external input to be used to decrement the internal timer circuitry. Refer to **TIMER** for additional information about the timer circuitry.

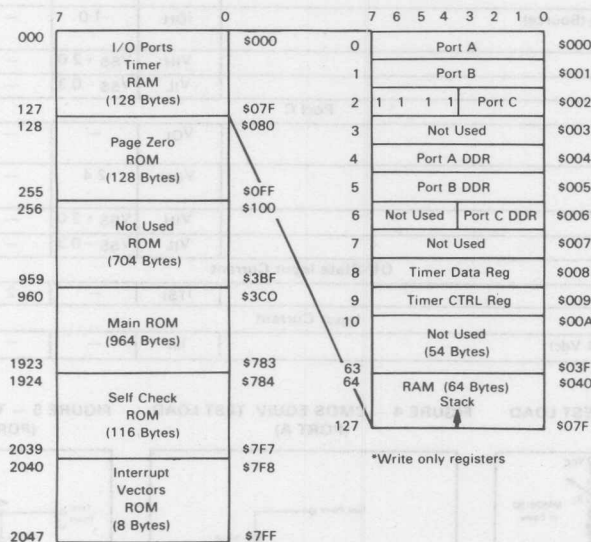
RESET — This pin allows resetting of the MCU at times other than the automatic resetting capability already in the MCU. Refer to **RESETS** for additional information.

NUM — This pin is not for user application and should be connected to ground.

INPUT/OUTPUT LINES (A0-A7, B0-B7, C0-C3) — These 20 lines are arranged into two 8-bit ports (A and B) and one 4-bit port (C). All lines are programmable as either inputs or outputs under software control of the data direction registers. Refer to **INPUTS/OUTPUTS** for additional information.

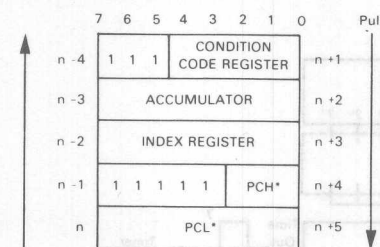
MEMORY

The MCU memory is configured as shown in Figure 6. During the processing of an interrupt, the contents of the MCU registers are pushed onto the stack in the order shown in Figure 7. Since the stack pointer decrements during pushes, the low order byte (PCL) of the program counter is stacked first; then the high order three bits (PCH) are stacked. This ensures that the program counter is loaded correctly as the stack pointer increments when it pulls data from the stack. A subroutine call will cause only the program counter (PCH, PCL) contents to be pushed onto the stack.

FIGURE 6 — MCU MEMORY CONFIGURATION

*Write only registers

FIGURE 7 — INTERRUPT STACKING ORDER



* For subroutine calls, only PCH and PCL are stacked

REGISTERS

The MCU has five registers available to the programmer. They are shown in Figure 8 and are explained in the following paragraphs.

ACCUMULATOR (A) — The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

INDEX REGISTER (X) — The index register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit address that may be added to an offset value to create an effective address. The index register can also be used for limited calculations and data manipulations when using read/modify write instructions. When not required by a code sequence being executed, the index register can be used as a temporary storage area.

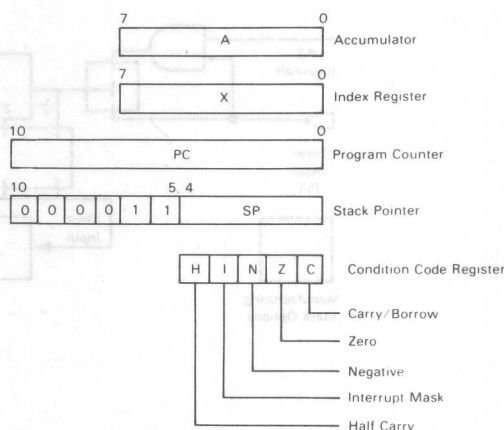
PROGRAM COUNTER (PC) — The program counter is an 11-bit register that contains the address of the next instruction to be executed.

STACK POINTER (SP) — The stack pointer is an 11-bit register that contains the address of the next free location on the stack. Initially, the stack pointer is set to location \$07F and is decremented as data is being pushed onto the stack and incremented as data is being pulled from the stack. The six most significant bits of the stack pointer are permanently set to 000011. During a MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location \$07F. Subroutines and interrupts may be nested down to location \$061 which allows the programmer to use up to 15 levels of subroutine calls.

CONDITION CODE REGISTER (CC) — The condition code register is a 5-bit register in which each bit is used to indicate or flag the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each individual condition code register bit is explained in the following paragraphs.

Half Carry (H) — Used during arithmetic operations (ADD and ADC) to indicate that a carry occurred between bits 3 and 4.

FIGURE 8 — PROGRAMMING MODEL



Interrupt (I) — This bit is set to mask the timer and external interrupt (INT). If an interrupt occurs while this bit is set it is latched and will be processed as soon as the interrupt bit is reset.

Negative (N) — Used to indicate that the result of the last arithmetic, logical or data manipulation was negative (bit 7 in result equal to a logical one).

Zero (Z) — Used to indicate that the result of the last arithmetic, logical or data manipulation was zero.

Carry/Borrow (C) — Used to indicate that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

TIMER

The MCU timer circuitry is shown in Figure 9. The 8-bit counter is loaded under program control and counts down toward zero as soon as the clock input is applied. When the timer reaches zero the timer interrupt request bit (bit 7) in the timer control register is set. The MCU responds to this interrupt by saving the present MCU state in the stack, fetching the timer interrupt vector from locations \$7F8 and \$7F9 and executing the interrupt routine. The timer interrupt can be masked by setting the timer interrupt mask bit (bit 6) in the timer control register. The interrupt bit (I bit) in the condition code register will also prevent a timer interrupt from being processed.

The clock input to the timer can be from an external source applied to the TIMER input pin or it can be the internal $\phi 2$ signal. Note that when the $\phi 2$ signal is used as the source it can be gated by an input applied to the TIMER input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is one

FIGURE 9 — TIMER BLOCK DIAGRAM

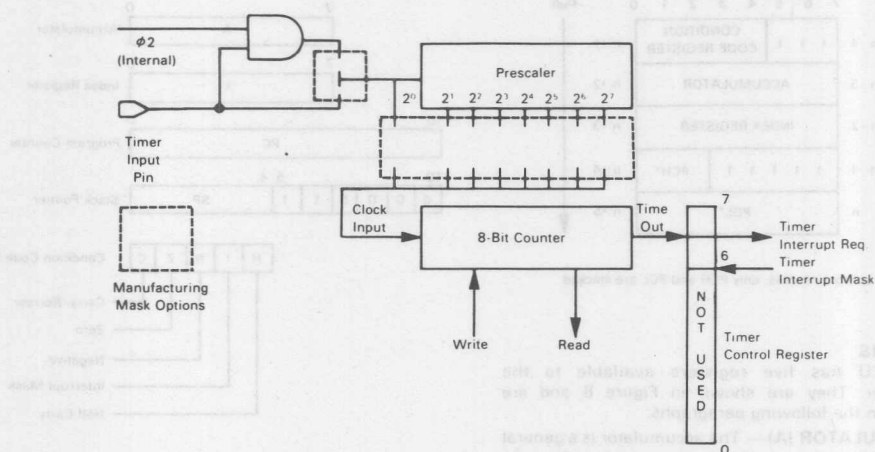
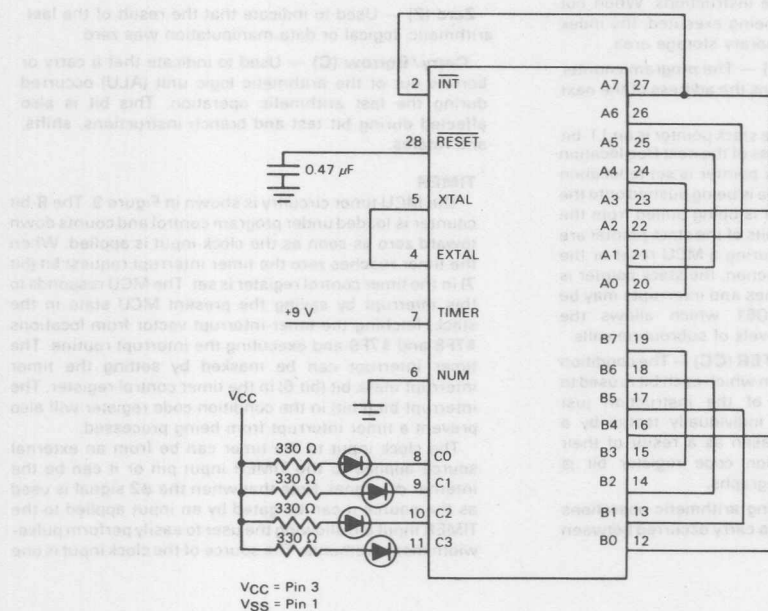


FIGURE 10 — SELF CHECK CONNECTIONS



of the options that has to be specified before manufacture of the MCU. A prescaler option can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before being applied to the counter. This prescaling option must also be specified before manufacturing begins. The timer continues to count past zero and its present count can be monitored at any time by monitoring the timer data register. This allows a program to determine the length of time since a timer interrupt has occurred and not disturb the counting process.

At power up or reset the prescaler and counter are initialized with all logical ones; the timer interrupt request bit (bit 7) is cleared and the timer interrupt request mask bit (bit 6) is set.

SELF CHECK

The self check capability of the MCU provides an internal check to determine if the part is functional. Connect the MCU as shown in Figure 10 and monitor the output of port C bit 3 for an oscillation of approximately three hertz.

RESETS

The MCU can be reset three ways: by the external reset input (RESET), by an internal low voltage detect circuit, and during the power up time. See Figure 11.

Upon power up, a minimum of 20 milliseconds is needed before allowing the reset input to go high. This time allows the internal oscillator to stabilize. Connecting a capacitor to the RESET input as shown in Figure 12 will provide sufficient delay.

INTERNAL OSCILLATOR OPTIONS

The internal oscillator circuit has been designed to require a minimum of external components. The use of a crystal (AT cut, 4 MHz max) or a resistor is sufficient to drive the internal oscillator with varying degrees of stability. A manufacturing mask option is available to provide better matching between the external components and the internal oscillator.

The different connection methods are shown in Figure 13. Crystal specifications are given in Figure 14. A resistor selection graph is given in Figure 15.

FIGURE 11 — POWER UP AND RESET TIMING

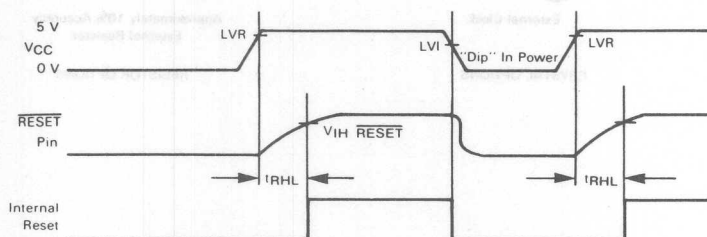


FIGURE 12 — POWER UP RESET DELAY CIRCUIT

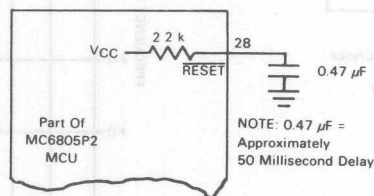
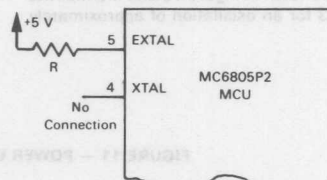
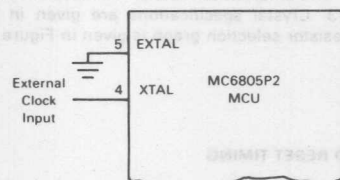
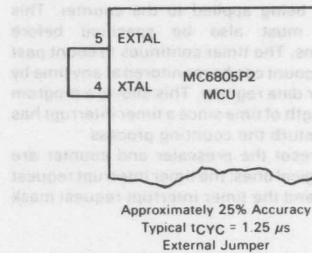
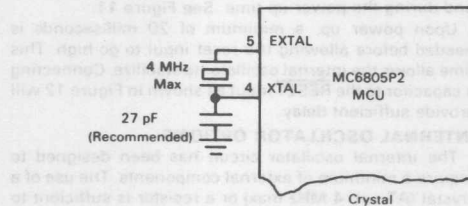


FIGURE 13 — INTERNAL OSCILLATOR OPTIONS



CRYSTAL OPTIONS

RESISTOR OPTIONS

FIGURE 14 — CRYSTAL PARAMETERS

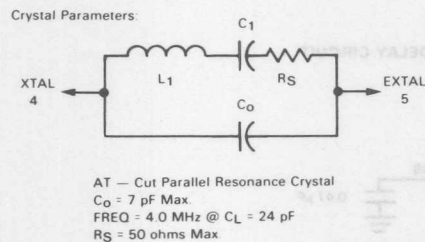
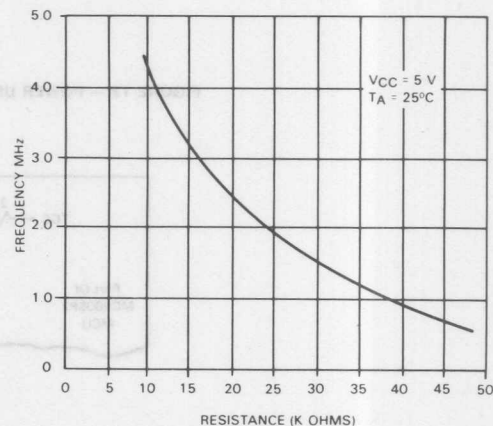


FIGURE 15 — TYPICAL RESISTOR SELECTION GRAPH



INTERRUPTS

The MCU can be interrupted three different ways: through the external interrupt (INT) input pin, the internal timer interrupt request, and a software interrupt instruction (SWI). When any interrupt occurs, processing is suspended, the present MCU state is pushed onto the stack, the interrupt bit (I) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. The interrupt service routines normally end with a return from interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt. Table 1 provides a listing of the interrupts, their priority, and the vector address that contain the starting address of the appropriate interrupt routine.

A sinusoidal signal (1 kHz maximum) can be used to generate an external interrupt (INT) as shown in Figure 16.

A flowchart of the interrupt processing sequence is given in Figure 17.

TABLE 1 — INTERRUPT PRIORITIES

Interrupt	Priority	Vector Address
RESET	1	\$7FE and \$7FF
SWI	2	\$7FC and \$7FD
INT	3	\$7FA and \$7FB
Timer	4	\$7F8 and \$7F9

INPUT/OUTPUT

There are 20 input/output pins. All pins are programmable as either inputs or outputs under software control of the data direction registers. When programmed as outputs, all I/O pins read latched output data regardless of the logic level at the output pin due to output loading (see Figure 18). When port B is programmed for outputs, it is capable of sinking 10 milliamperes on each pin (one volt maximum). All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs while port B and C lines are CMOS compatible as inputs. Figure 19 provides some examples of port connections.

FIGURE 16 — TYPICAL SINUSODIAL INTERRUPT CIRCUITS

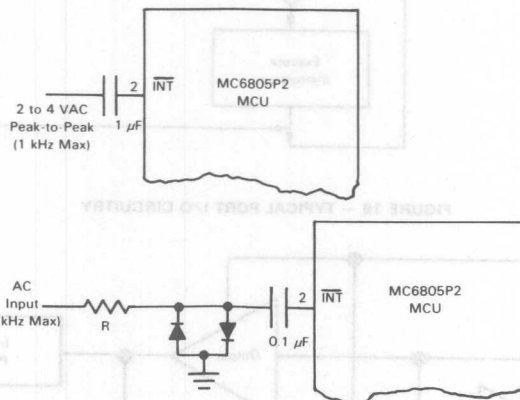


FIGURE 17 — INTERRUPT PROCESSING FLOWCHART

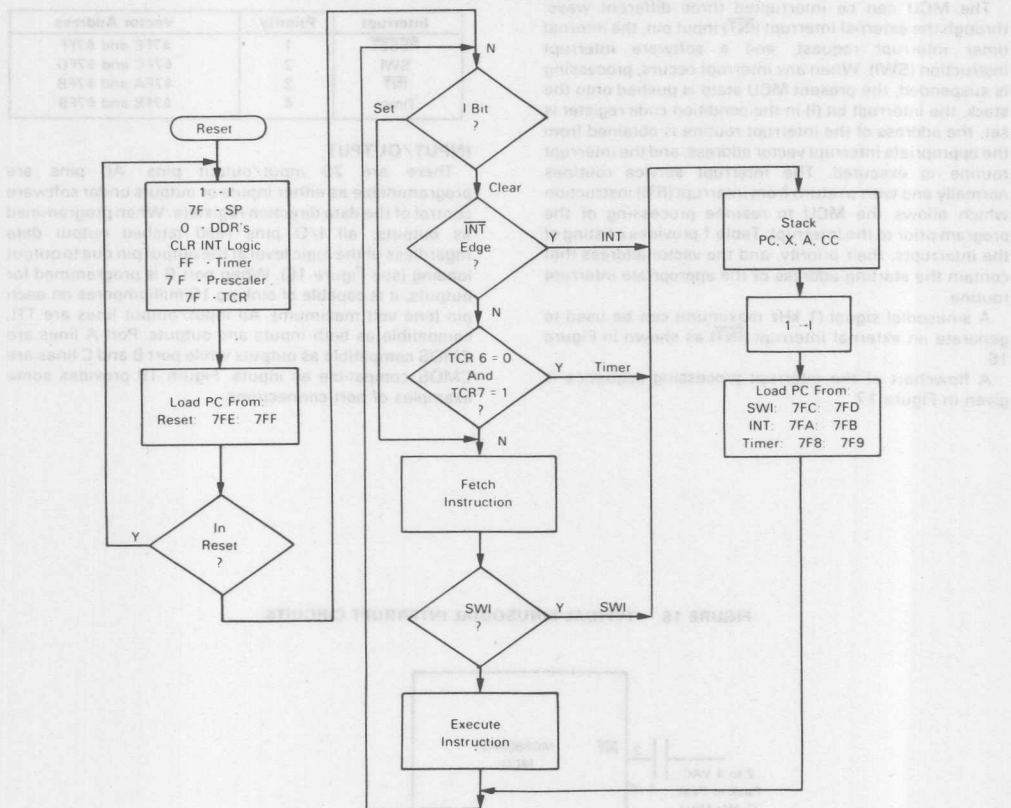


FIGURE 18 — TYPICAL PORT I/O CIRCUITRY

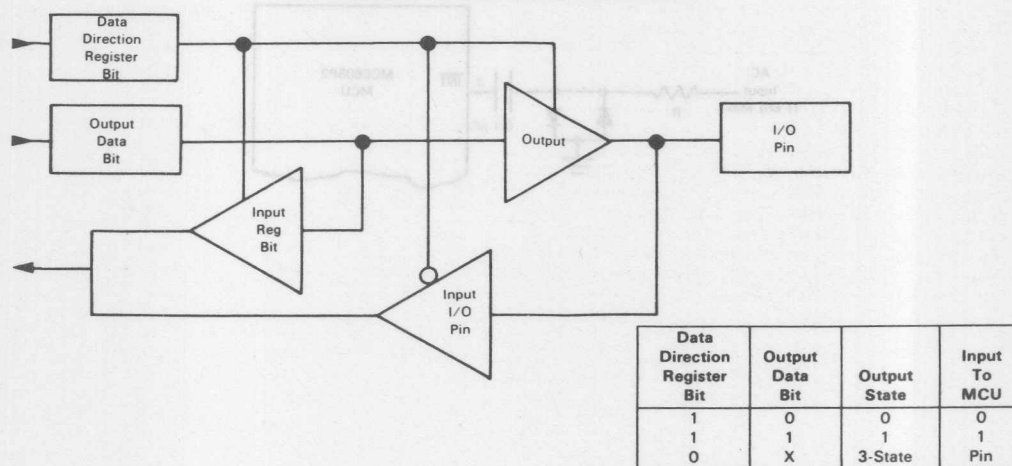
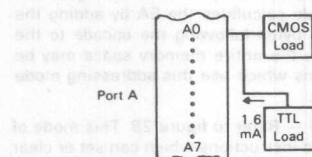
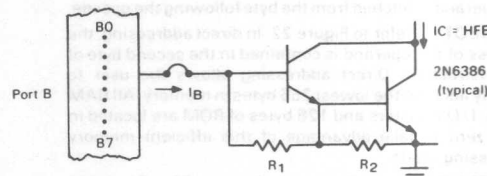
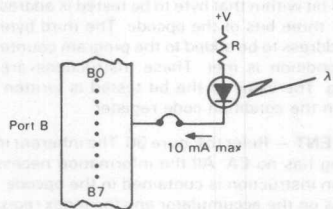
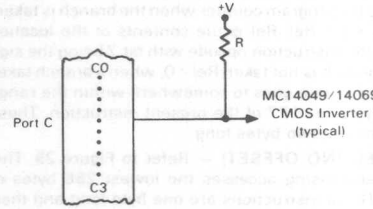


FIGURE 19 — TYPICAL PORT CONNECTIONS

Port A Programmed as output(s) driving CMOS and TTL Load directly.
(a)Port B Programmed as output(s) driving Darlington base directly.
(b)Port B Programmed as output(s) driving LED(s) directly.
(c)Port C Programmed as output(s) driving CMOS using external pull-up resistors
(d)

BIT MANIPULATION

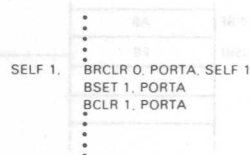
The MCU has the ability to set or clear any single random access memory or input/output bit (except the data direction registers) with a single instruction (BSET, BCLR). Any bit in the page zero read only memory can be tested, using the BRSET and BRCLR instructions, and the program branches as a result of its state. This capability to work with any bit in RAM, ROM or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines. The example in Figure 20 illustrates the usefulness of the bit manipulation and test instructions. Assume that bit 0 of port A is connected to a zero crossing detector circuit and that bit 1 of port A is connected to the trigger of a TRIAC which powers the controlled hardware.

This program, which uses only seven ROM locations, provides turn-on of the TRIAC within 14 microseconds of the zero crossing. The timer could also be incorporated to

provide turn-on at some later time which would permit pulse-width modulation of the controlled power.

ADDRESSING MODES The MCU has ten addressing modes available for use by the programmer. They are explained and illustrated briefly in the following paragraphs.

FIGURE 20 — BIT MANIPULATION EXAMPLE



IMMEDIATE — Refer to Figure 21. The immediate addressing mode accesses constants which do not change during program execution. Such instructions are two bytes long. The effective address (EA) is the PC and the operand is fetched from the byte following the opcode.

DIRECT — Refer to Figure 22. In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in memory. All RAM space, I/O registers and 128 bytes of ROM are located in page zero to take advantage of this efficient memory addressing mode.

EXTENDED — Refer to Figure 23. Extended addressing is used to reference any location in memory space. The EA is the contents of the two bytes following the opcode. Extended addressing instructions are three bytes long.

RELATIVE — Refer to Figure 24. The relative addressing mode applies only to the branch instructions. In this mode the contents of the byte following the opcode is added to the program counter when the branch is taken. $EA = (PC) + 2 + Rel$. Rel is the contents of the location following the instruction opcode with bit 7 being the sign bit. If the branch is not taken $Rel = 0$, when a branch takes place, the program goes to somewhere within the range of +129 bytes to -127 of the present instruction. These instructions are two bytes long.

INDEXED (NO OFFSET) — Refer to Figure 25. This mode of addressing accesses the lowest 256 bytes of memory. These instructions are one byte long and their EA is the contents of the index register.

INDEXED (8-BIT OFFSET) — Refer to Figure 26. The EA is calculated by adding the contents of the byte

following the opcode to the contents of the index register. In this mode, 511 low memory locations are accessible. These instructions occupy two bytes.

INDEXED (16-BIT OFFSET) — Refer to Figure 27. This addressing mode calculates the EA by adding the contents of the two bytes following the opcode to the index register. Thus, the entire memory space may be accessed. Instructions which use this addressing mode are three bytes long.

BIT SET/CLEAR — Refer to figure 28. This mode of addressing applies to instructions which can set or clear any bit on page zero. The lower three bits in the opcode specify the bit to be set or cleared while the byte following the opcode specifies the address in page zero.

BIT TEST AND BRANCH — Refer to Figure 29. This mode of addressing applies to instructions which can test any bit in the first 256 locations (\$00-\$FF) and branch to any location relative to the PC. The byte to be tested is addressed by the byte following the opcode. The individual bit within that byte to be tested is addressed by the lower three bits of the opcode. The third byte is the relative address to be added to the program counter if the branch condition is met. These instructions are three bytes long. The value of the bit tested is written to the carry bit in the condition code register.

INHERENT — Refer to Figure 30. The inherent mode of addressing has no EA. All the information necessary to execute an instruction is contained in the opcode. Direct operations on the accumulator and the index register are included in this mode of addressing. In addition, control instructions such as SWI, RTI belong to this group. All inherent addressing instructions are one byte long.

FIGURE 21 — IMMEDIATE ADDRESSING EXAMPLE

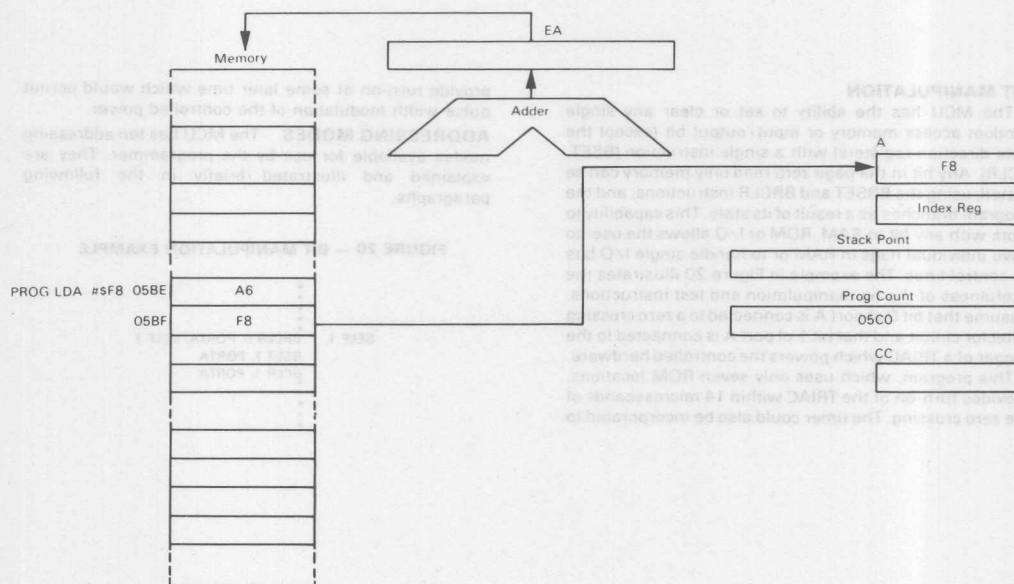


FIGURE 22 — DIRECT ADDRESSING EXAMPLE

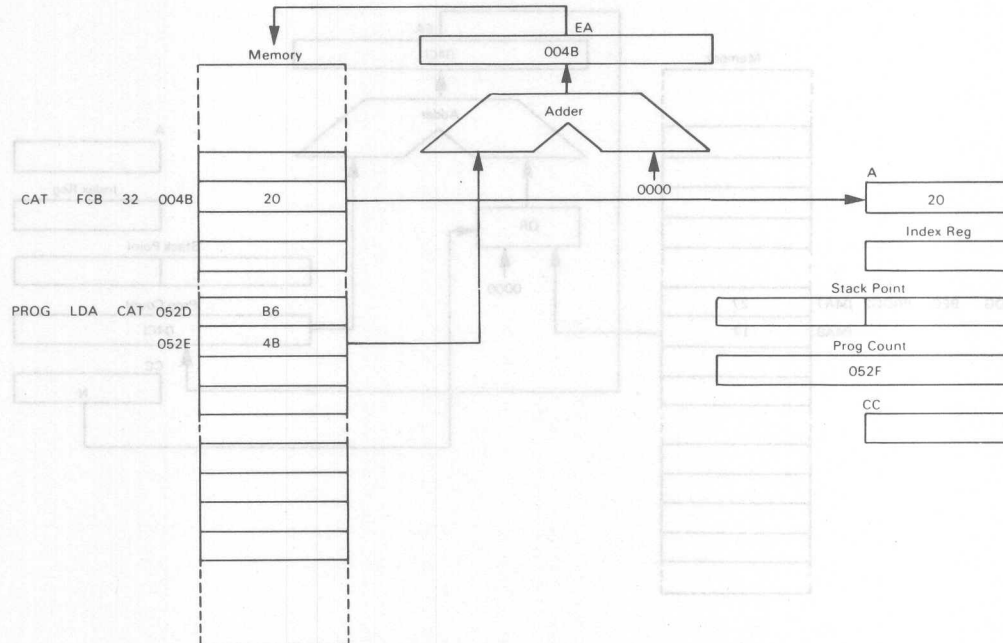


FIGURE 23 — EXTENDED ADDRESSING EXAMPLE

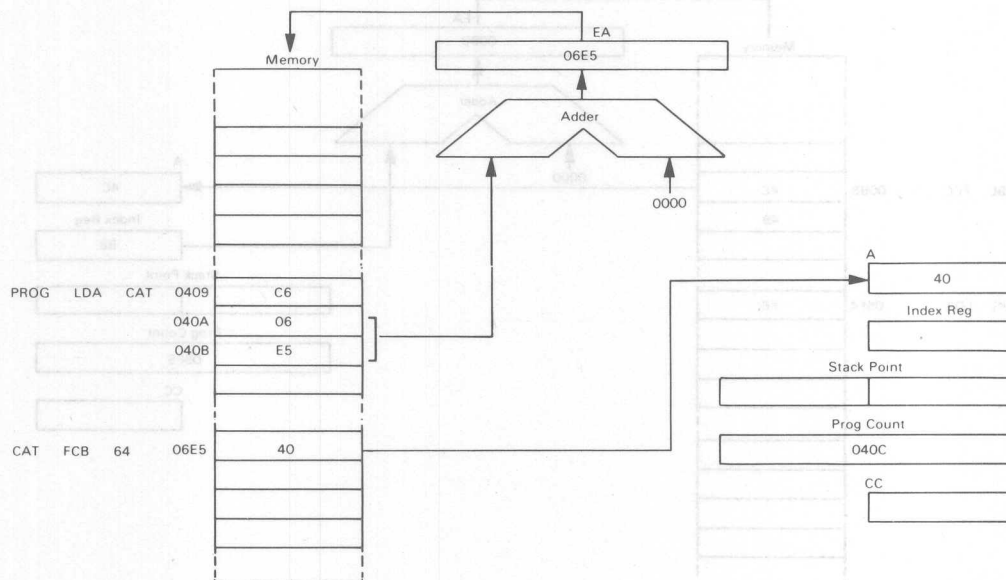


FIGURE 24 — RELATIVE ADDRESSING EXAMPLE

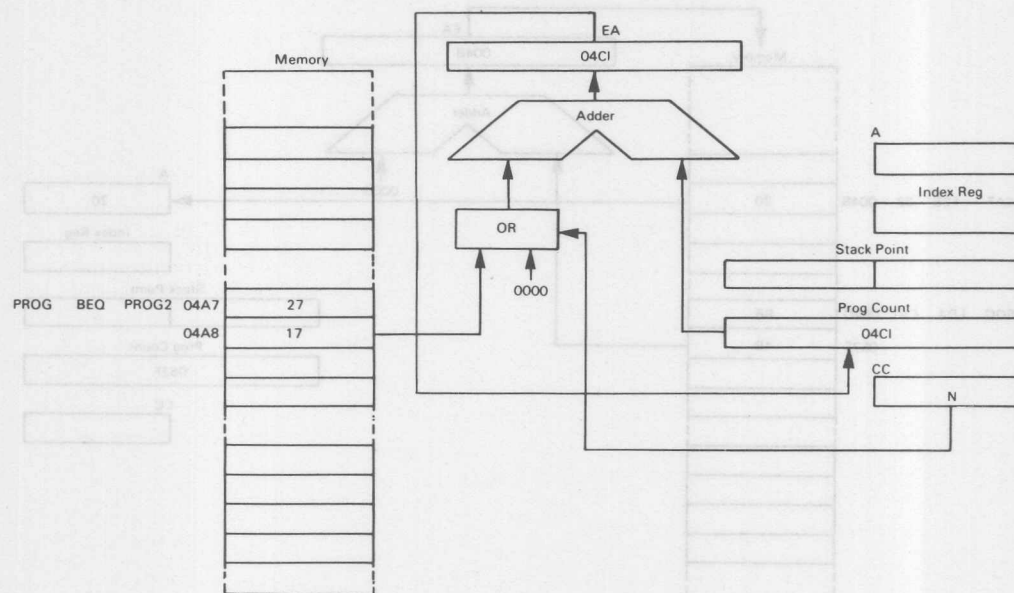


FIGURE 25 — INDEXED (NO OFFSET) ADDRESSING EXAMPLE

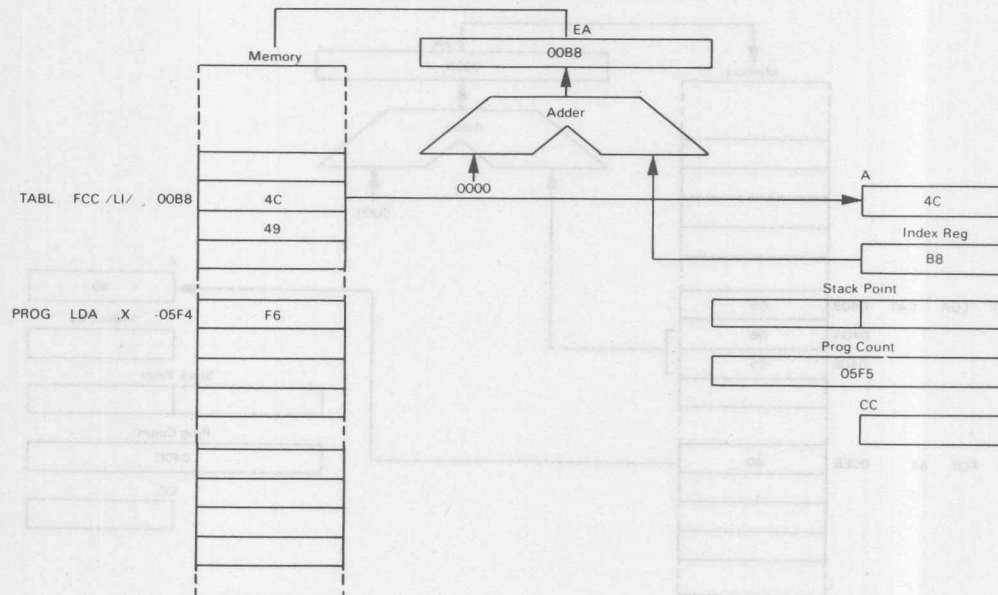


FIGURE 26 — INDEXED (8-BIT OFFSET) ADDRESSING EXAMPLE

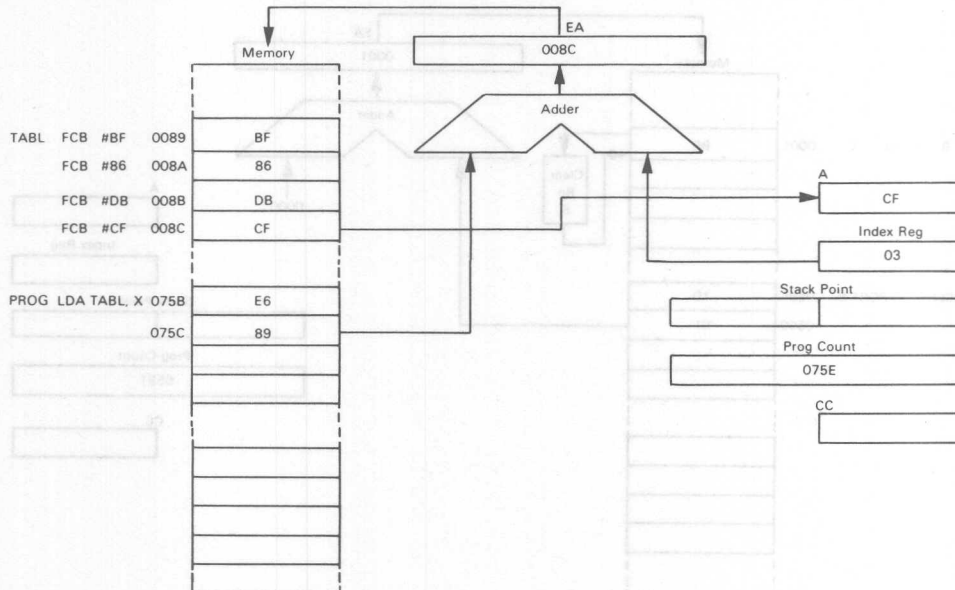


FIGURE 27 — INDEXED (16-BIT OFFSET) ADDRESSING EXAMPLE

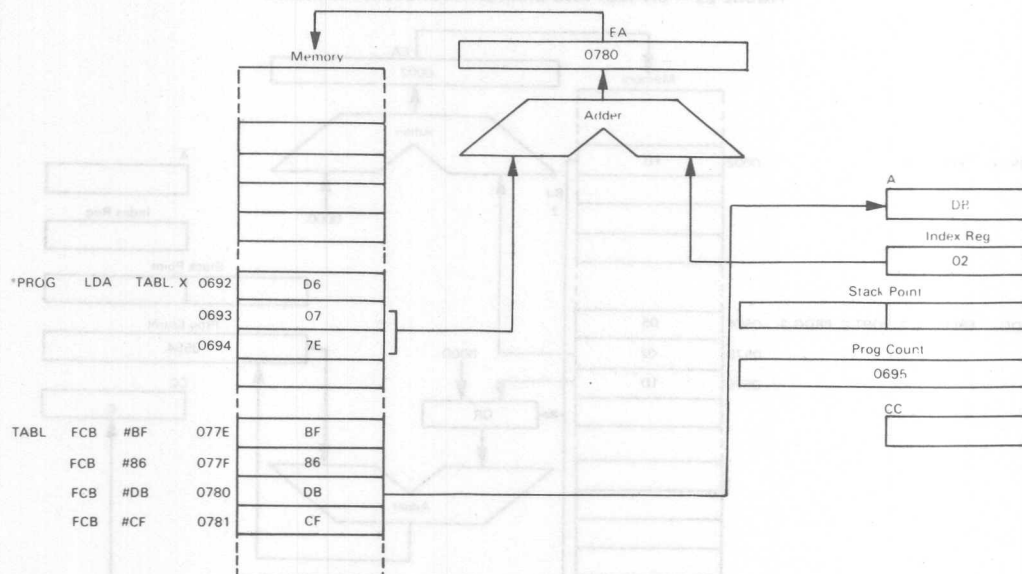


FIGURE 28 — BIT SET/CLEAR ADDRESSING EXAMPLE

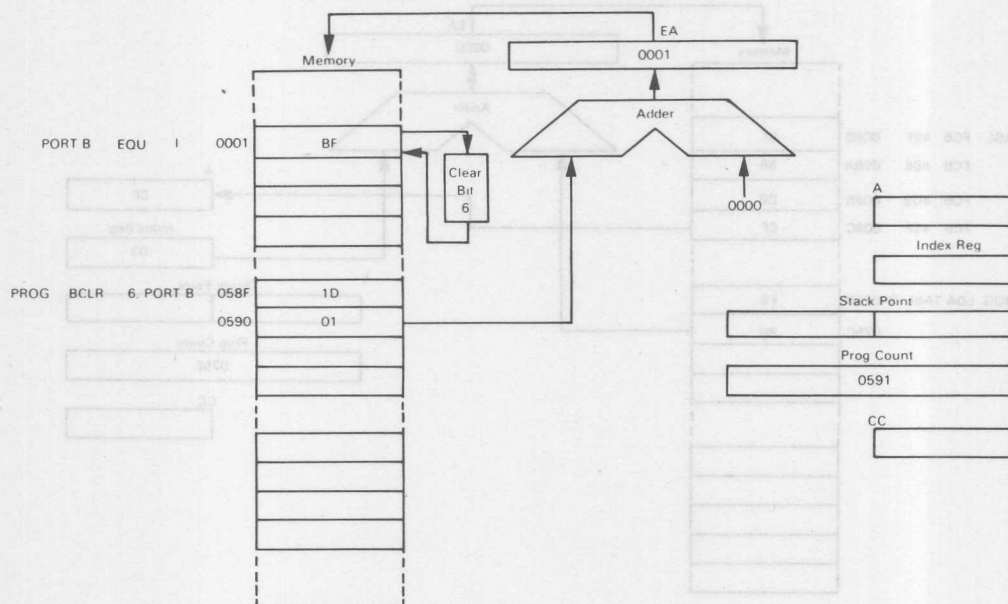


FIGURE 29 — BIT TEST AND BRANCH ADDRESSING EXAMPLE

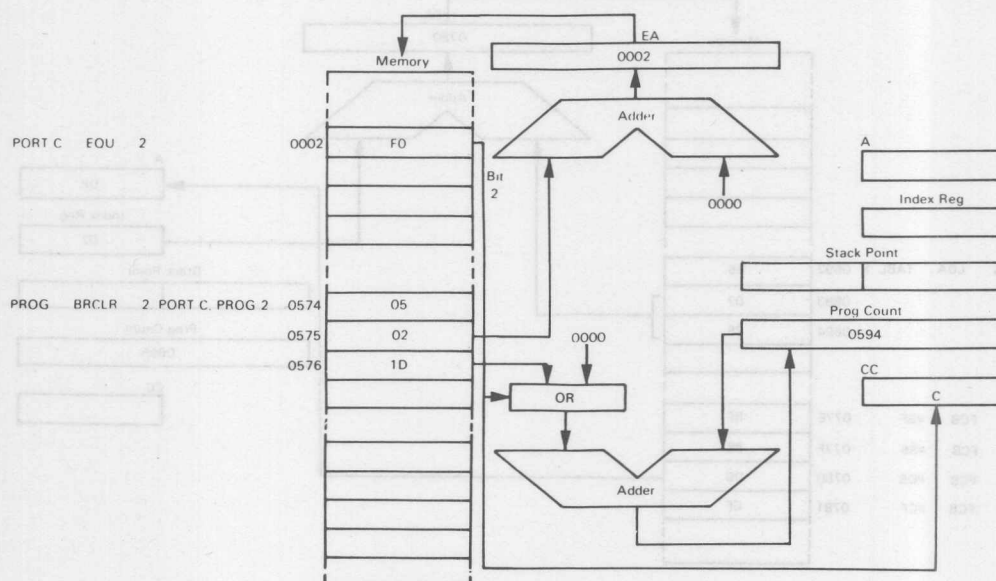
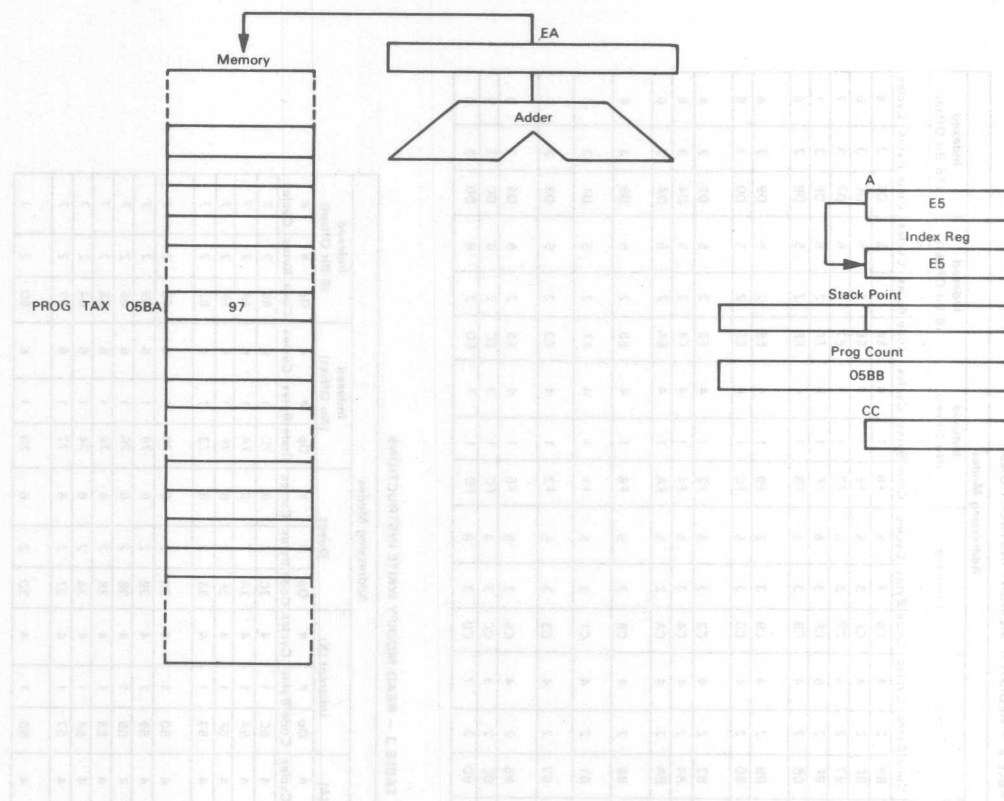


FIGURE 30 — INHERENT ADDRESSING EXAMPLE

**INSTRUCTION SET**

The MCU has a set of 59 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS — Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 2.

READ/MODIFY/WRITE INSTRUCTIONS — These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/

write instructions since it does not perform the write. Refer to Table 3.

BRANCH INSTRUCTIONS — The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 4.

BIT MANIPULATION INSTRUCTIONS — These instructions are used on any bit in the first 256 bytes of the memory. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 5.

CONTROL INSTRUCTIONS — The control instructions control the MCU operations during program execution. Refer to Table 6.

ALPHABETICAL LISTING — The complete instruction set is given in alphabetical order in Table 7.

OPCODE MAP — Table 8 is an opcode map for the instructions used on the MCU.

TABLE 2 — REGISTER-MEMORY INSTRUCTIONS

Function	Mnemonic	Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
Load X from Memory	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
Store A in Memory	STA	—	—	—	B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
Store X in Memory	STX	—	—	—	BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
Add Memory to A	ADD	AB	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
Add Memory and Carry to A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
Subtract Memory	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
AND Memory to A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
OR Memory with A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	4	C8	3	5	FA	1	4	EA	2	5	DA	3	6
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
Jump Unconditional	JMP	—	—	—	BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
Jump to Subroutine	JSR	—	—	—	BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9

TABLE 3 — READ-MODIFY-WRITE INSTRUCTIONS

Function	Mnemonic	Addressing Modes											
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6
Decrement	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6
Clear	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6
Complement	COM	43	1	4	53	1	4	33	2	6	73	1	6
Negate (2's Complement)	NEG	40	1	4	50	1	4	30	2	6	70	1	6
Rotate Left Thru Carry	ROL	49	1	4	59	1	4	39	2	6	79	1	6
Rotate Right Thru Carry	ROR	46	1	4	56	1	4	36	2	6	76	1	6
Logical Shift Left	LSL	48	1	4	58	1	4	38	2	6	78	1	6
Logical Shift Right	LSR	44	1	4	54	1	4	34	2	6	74	1	6
Arithmetic Shift Right	ASR	47	1	4	57	1	4	37	2	6	77	1	6
Test for Negative or Zero	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6

TABLE 4 — BRANCH INSTRUCTIONS

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	4
Branch Never	BRN	21	2	4
Branch IFF Higher	BHI	22	2	4
Branch IFF Lower or Same	BLS	23	2	4
Branch IFF Carry Clear	BCC	24	2	4
(Branch IFF Higher or Same)	(BHS)	24	2	4
Branch IFF Carry Set	BCS	25	2	4
(Branch IFF Lower)	(BLO)	25	2	4
Branch IFF Not Equal	BNE	26	2	4
Branch IFF Equal	BEQ	27	2	4
Branch IFF Half Carry Clear	BHCC	28	2	4
Branch IFF Half Carry Set	BHCS	29	2	4
Branch IFF Plus	BPL	2A	2	4
Branch IFF Minus	BMI	2B	2	4
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	4
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	4
Branch IFF Interrupt Line is Low	BIL	2E	2	4
Branch IFF Interrupt Line is High	BIH	2F	2	4
Branch to Subroutine	BSR	AD	2	8

TABLE 5 — BIT MANIPULATION INSTRUCTIONS

Function	Mnemonic	Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is set	BRSET n (n = 0-7)	—	—	—	2 · n	3	10
Branch IFF Bit n is clear	BRCLR n (n = 0-7)	—	—	—	01 + 2 · n	3	10
Set Bit n	BSET n (n = 0-7)	10 + 2 · n	2	7	—	—	—
Clear bit n	BCLR n (n = 0-7)	11 + 2 · n	2	7	—	—	—

TABLE 6 — CONTROL INSTRUCTIONS

Function	Mnemonic	Inherent		
		Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	11
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No Operation	NOP	9D	1	2

TABLE 7 — INSTRUCTION SET

Mnemonic	Addressing Modes								Bit Set/Clear	Bit Test & Branch	Condition Code				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)			H	I	N	Z	C
ADC		X	X	X		X	X	X			△	●	△	△	△
ADD		X	X	X		X	X	X			△	●	△	△	△
AND		X	X	X		X	X	X			●	●	△	△	●
ASL	X		X			X	X				●	●	△	△	△
ASR	X		X			X	X				●	●	△	△	△
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	△	△	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI											●	●	●	●	●
BMS											●	●	●	●	●
BNE											●	●	●	●	●
BPL											●	●	●	●	●
BRA											●	●	●	●	●
BRN											●	●	●	●	●
BRCLR										X	●	●	●	●	△
BRSET										X	●	●	●	●	△
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLC	X										●	●	●	●	O
CLI	X										●	O	●	●	●
CLR	X					X	X				●	●	O	1	●
CMP		X	X	X		X	X	X			●	●	△	△	△
COM	X		X			X	X				●	●	△	△	1
CPX		X	X	X		X	X	X			●	●	△	△	△
DEC	X		X			X	X				●	●	△	△	●
EOR		X	X	X		X	X	X			●	●	△	△	●
INC	X		X			X	X				●	●	△	△	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	△	△	●
LDX		X	X	X		X	X	X			●	●	△	△	●
LSL	X		X			X	X				●	●	△	△	△
LSR	X		X			X	X				●	●	O	△	△
NEQ	X		X			X	X				●	●	△	△	△
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	△	△	●
ROL	X		X			X	X				●	●	△	△	△
RSP	X										●	●	●	●	●

Condition Code Symbols:

H Half Carry (From Bit 3)
 I Interrupt Mask
 N Negative (Sign Bit)
 Z Zero

C Carry/Borrow
 △ Test and Set if True, Cleared Otherwise
 ● Not Affected

TABLE 7 — INSTRUCTION SET
(CONT.)

Mnemonic	Addressing Modes								Bit Set/ Clear	Bit Test & Branch	Condition Code				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)			H	I	N	Z	C
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	●	●	●
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	●	●	●
STX			X	X		X	X	X			●	●	●	●	●
SUB		X	X	X		X	X	X			●	●	●	●	●
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	●	●	●
TXA	X										●	●	●	●	●

Condition Code Symbols

- | | |
|---------------------------|---|
| H Half Carry (From Bit 3) | C Carry/Borrow |
| I Interrupt Mask | △ Test and Set if True, Cleared Otherwise |
| N Negative (Sign Bit) | ● Not Affected |
| Z Zero | ? Load CC Register From Stack |

TABLE 8 — OPCODE MAP

Bit Manipulation		Branch	Read/Modify/Write					Control		Register/Memory							
Test & Branch	Set/ Clear		Rel	DIR	A	X	.X1	.X0	INH	INH	IMM	DIR	EXT	.X2	.X1	.X0	
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		← High
BRSET0	BSET0	BRA				NEQ			RTI*	—				SUB			0
1	BRCLR0	BCLR0	BRN			—			RTS*	—				CMP			1
2	BRSET1	BSET1	BHI			—			—	—				SBC			2
3	BRCLR1	BCLR1	BLS			COM			SWI*	—				CMPX/CPX			3
4	BRSET2	BSET2	BCC			LSR			—	—				AND			4
5	BRCLR2	BCLR2	BCS			—			—	—				BIT			5
6	BRSET3	BSET3	BNE			ROR			—	—				LDA			6
7	BRCLR3	BCLR3	BEQ			ASR			—	TAX	—			STA (+1)			7
8	BRSET4	BSET4	BHCC			LSL/ASL			—	CLC				EOR			8
9	BRCLR4	BCLR4	BHCS			ROL			—	SEC				ADC			9
A	BRSET5	BSET5	BPL			DEC			—	CLI				ORA			A
B	BRCLR5	BCLR5	BMI			—			—	SEI				ADD			B
C	BRSET6	BSET6	BMC			INC			—	RSP	—			JMP (-1)			C
D	BRCLR6	BCLR6	BMS			TST			—	NOP	BSR*			JSR (+3)			D
E	BRSET7	BSET7	BIL			—			—	—				LDX			E
F	BRCLR7	BCLR7	BIH			CLR			—	TXA	—			STX (+1)			F
3/10	2/7	2/4	2/6	1/4	1/4	2/7	1/6	1/*	1/2	2/2	2/4	3/5	3/6	2/5	1/4		

Notes:

Undefined opcodes are marked with "—".

The numbers at the bottom of each column denote the number of bytes and the number of cycles required. (Bytes/Cycles)

Mnemonics followed by a "*" require a different number of cycles as follows:

- RTI 9
RTS 6
SWI 11
BSR 8

() indicate that the number in parenthesis must be added to the cycle count for that instruction.

ORDERING INFORMATION

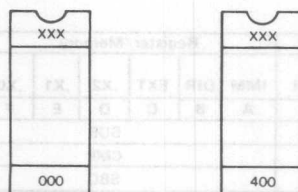
The following information is required when ordering a custom MCU. This information may be transmitted to Motorola in any of the following media:

- PROM(s)
- Assembler formatted object tape
- Punched card deck
- Paper tape of card deck format
- MDOS disk file

To initiate a ROM pattern for the MCU it is necessary to first contact your local field service office, local sales person or your local Motorola representative.

PROMS — The MCM2708 or MCM2716 type PROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. The PROMs must be clearly marked to indicate which PROM corresponds to which address space (000-3FF HEX). See Figure 31 for recommended marking procedure.

After the PROM(s) are marked they should be placed in conductive IC carriers and securely packed. Do not use styrofoam.

FIGURE 31 — PROM MARKING

XXX = Customer ID

ASSEMBLER FORMATTED OBJECT TAPE — Cassette tapes produced on a Silent 700 terminal and EXORciser are acceptable.

PUNCHED CARD DECK — The custom MCU may be specified for manufacture in the form of standard 80-column punched cards.

The card deck for specifying the custom MCU has the following format:

- OPTION CARD
- COMMENT CARDS
- X CARDS
- C CARDS

Option Card — The first card in the deck must be the OPTION CARD. The format is as follows:

- Column 1-20: Customer name. Any 20 characters may be used.
- Column 25-29: This is a 5-digit number assigned by Motorola. Leave this field blank. It will be punched at Motorola unless otherwise notified.
- Column 37-39: Address field base on output listing. The characters HEX or DEC specify the output listing address base as hexadecimal or decimal, respectively. If omitted, DEC is assumed.

Column 41-43: Data field base on output listing. The characters HEX or DEC specify the output listing ROM data base as hexadecimal or decimal, respectively. If omitted, DEC is assumed.

COMMENT CARDS — Comment Cards must have an asterisk (*) in column 1. The remaining 79 columns may contain any letter, number, or character.

X Cards — Five X cards are possible. All X cards have an X in column 1 and one or three or more words, each separated by one blank space.

The possibilities are:

- 1) X SEQUENCE
- 2) X BASE DEC DEC
- 3) X BASE DEC HEX
- 4) X BASE HEX DEC
- 5) X BASE HEX HEX

Card 1 specifies that there are sequence numbers on each data card that follows. The sequence numbers must be in columns 77-79 of the data cards (C Cards) and must be in decimal, right justified. The numbers must start with 1 (one) and must be in order. The X SEQUENCE Card may appear anywhere within the deck after the Option Card. If it appears within the data card section, data cards encountered before the X SEQUENCE Card will not be checked for sequence numbers. All following cards will be checked. If no X SEQUENCE Card is used, no sequence numbers will be checked.

It is initially assumed that the address and byte count as well as the data specified on the C cards will be in decimal. An X BASE card can be used to override this specification. The second word on the card (that following BASE) specifies the base (either DEC or HEX) of the address and byte count on all following C cards. The last word specifies the base of the data fields on the C cards. An X BASE card may appear anywhere within the deck following the OPTION card. It may be overridden by another X BASE card. All data cards (C cards) following an X BASE card will be interpreted as per that X BASE card unless another X BASE card is encountered. If no X BASE cards are used, it is assumed that all fields on the C cards are in decimal.

NOTE:

Once an X SEQUENCE card is encountered, all successive cards will be checked for the proper sequence number; and, unlike X BASE cards, this option cannot thereafter be altered by another X SEQUENCE card.

C Cards — These cards contain the actual ROM data. All fields are right-justified.

- Column 1: C (the letter C)
- Column 2-9: ADD
- Column 10-12: BYTE
- Column 14-16: DATA 1
- Column 17-19: DATA 2

- Columns 76-78: DATA 21
- Column 77-79: DATA 22 or SEQUENCE NUMBER

ADD is the address of the first byte of data (DATA 1) contained on that card. Byte is the number of bytes of data to be read from that card. BYTE must be greater than zero

and less than 23 (1-22) if no sequence numbers are used, and less than 22 (1-21) if sequence numbers are used. If, for example, there are ten data fields punched on the card, by BYTE = 2, only the first two will be read. Also, if there are two punched data fields, for example, and BYTE = 6, six ROM locations will be filled from that card. The four unspecified fields will be decoded as zero. ADD and BYTE are always in the same base (HEX or DECIMAL). DATA 1 through DATA N is the data to be placed in the ROM at address ADD through ADD + (N-1), respectively.

Any ROM address not filled as a result of reading data from a C card will be filled with zero. If a particular location has already been specified by a C card, but a successive C card also has the data which is to be placed in that location, the second C card will override the first.

PAPER TAPE OF CARD DECK FORMAT — Punched Paper tape (ASCII) in the same format as cards can also be accepted. However, your order will be processed faster if the data is in card format. After the tape leader there should be a CR LF. Data records should be a full 80 columns, each terminated by a CR LF. Following the last Data record, there should be one more record with the first three characters being EOF, followed by 77 blanks and a CR LF.

CR = Carriage Return

LF = Line Feed

OPTION LIST

Select the options for your MCU from the following list. A manufacturing mask will be generated from this information.

☐ ROM Mask

Timer Clock Source

☐ Internal $\phi 2$ clock

☐ TIMER input pin (7)

Timer Prescaler

☐ 2^0 (divide by 1)

☐ 2^4 (divide by 16)

☐ 2^1 (divide by 2)

☐ 2^5 (divide by 32)

☐ 2^2 (divide by 4)

☐ 2^6 (divide by 64)

☐ 2^3 (divide by 8)

☐ 2^7 (divide by 128)

Internal Oscillator Input

☐ Crystal

☐ Resistor

Low Voltage Inhibit

☐ Disable

☐ Enable

Customer Name _____

Address _____

City _____ State _____ Zip _____

Phone (_____) _____ Extension _____

Contact Ms/Mr _____

Customer Part Number _____

Pattern Media

2708 PROM

2716 PROM

Paper Object Tape

Silent 700 Cassette

Card Deck

Tape of Card Deck

MDOS Disk File

(Note 2)

Notes: (2) Other media require prior factory approval.

Signature _____

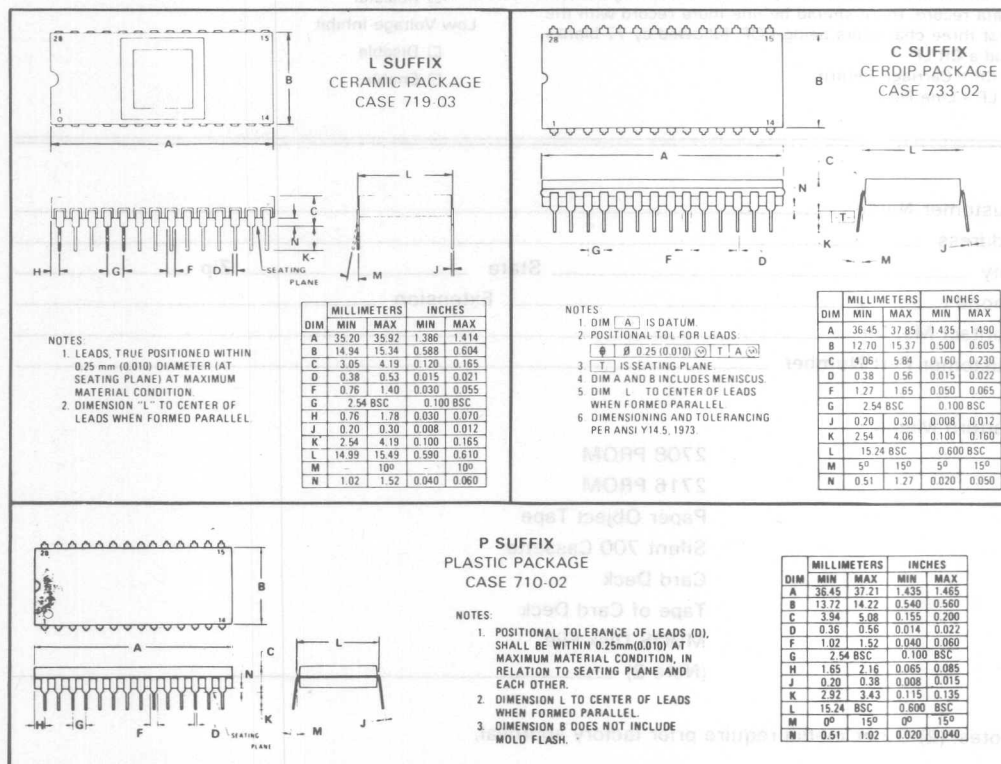
Title _____

TABLE 9 — THE GROWING M6805 FAMILY

M6805 Family
System Configuration
And Programming
Features

	MC6805P2	MC146805E2	MC6805R2	MC146805G2
Technology	NMOS	CMOS	NMOS	CMOS
Number of Pins	28	40	40	40
On Chip RAM (bytes)	64	112	64	112
On Chip User ROM (bytes)	1 1k	None	2k	2 2k
Expansion Bus	None	Yes	None	Yes
Bidirectional I/O Lines	20	16	32	32
I/O Options	None	None	A/D Converter	None
Software Compatibility	Similar to M6800		Similar M6800	
True Bit Manipulation	Yes	Yes	Yes	Yes
Instructions	59	61	59	61
Ten Addressing Modes	Yes	Yes	Yes	Yes

PACKAGE DIMENSIONS



Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

Advance Information

8-BIT MICROCOMPUTER UNIT WITH A/D

The MC6805R2 Microcomputer Unit (MCU) is a member of the M6805 Family of Microcomputers. This 8-bit microcomputer contains a CPU, on-chip clock, ROM, RAM, I/O, 4 channel 8-bit A/D, and timer. It is designed for the user who needs an economical microcomputer with the proven capabilities of the M6800-based instruction set. A comparison of the key features of the M6805 Family of Microcomputers is shown in the table on the last page of this data sheet. The following are some of the hardware and software highlights of the MCU. Some of the hardware options are mask programmable.

Hardware Features:

- 8-Bit Architecture
- 64 Bytes of RAM
- Memory Mapped I/O
- 2048 Bytes of User ROM
- Internal 8-Bit Timer with 7-Bit Prescaler
- 4 Vectored Interrupts; Timer, Software and Two External
- 24 TTL/CMOS Compatible I/O Lines with 8 of these LED Compatible
- 8 Input Lines
- A/D Converter
 - 8-Bit Conversion
 - 4 Multiplexed Analog Inputs
 - $\pm 1/2$ LSB Quantizing Error
 - $\pm 1/2$ LSB All Other Errors
 - ± 1 LSB Total Error (max)
 - Ratiometric Conversion
- Zero-Crossing Detection
- On-Chip Clock Generator
- Self-Check Mode
- Master Reset
- Low Voltage Inhibit
- Complete Development System Support on EXORciser
- 5 Vdc Single Supply

Software Features:

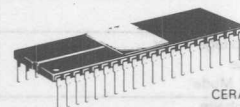
- Similar to M6800
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instructions
- Versatile Interrupt Handling
- Versatile Index Register
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Branches
- Memory Usable as Registers/Flags
- Single Instruction Memory Examine/Change
- 10 Powerful Addressing Modes
- All Addressing Modes Apply to ROM, RAM, and I/O
- User Callable Self-Check Subroutines

MC6805R2

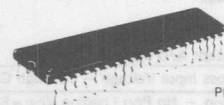
HMOS

(HIGH DENSITY
N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

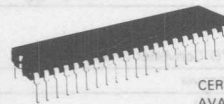
8-BIT MICROCOMPUTER WITH A/D



L SUFFIX
CERAMIC PACKAGE
CASE 715



P SUFFIX
PLASTIC PACKAGE
CASE 711



S SUFFIX
CERDIP PACKAGE ALSO
AVAILABLE - CASE 734

FIGURE 1 - PIN ASSIGNMENTS

VSS	1	40	PA7	
RESET	2	39	PA6	
INT	3	38	PA5	
VCC	4	37	PA4	
EXTAL	5	36	PA3	
XTAL	6	35	PA2	
NUM	7	34	PA1	
TIMER	8	33	PA0	
PC0	9	32	PB7	
PC1	10	31	PB6	
PC2	11	30	PB5	
PC3	12	29	PB4	
PC4	13	28	PB3	
PC5	14	27	PB2	
PC6	15	26	PB1	
PC7	16	25	PB0	
PD7	17	AN0 24	PD0	
PD6	18	INT2	AN1 23	PD1
PD5	19	V _{RH}	AN2 22	PD2
PD4	20	V _{RL}	AN3 21	PD3

MC6805R2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Junction Temperature	T_J		
Plastic Package		150	°C
Ceramic Package		175	
Cerdip		175	
Thermal Resistance	ϕ_{JA}		
Plastic Package		100	°C/W
Ceramic Package		50	
Cerdip		60	

Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.25 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ - 70^\circ \text{C}$ Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	4.0	—	V_{CC}	Vdc
RESET		4.0	2.2*		
INT		—	—		
All Other		+2.0	—		
Input High Voltage Timer	V_{IH}	+2.0	—	V_{CC}	Vdc
Timer Mode		—	9.0	15.0	
Self-Check Mode		—	—	—	
Input Low Voltage	V_{IL}	-0.3	—	0.8	Vdc
RESET		-0.3	2.0*	+1.5	
INT		-0.3	—	+0.8	
All Other (Except A/D Inputs)		-0.3	—	—	
INT Zero — Cross Input Voltage — Through Capacitor	V_{INT}	2	—	4	V_{acPP}
Power Dissipation — No Port Loading $V_{CC} = 5.25 \text{ V}$, $T_J = 0^\circ \text{C}$	P_D	—	600	—	mW
Input Capacitance	C_{in}	—	25	—	pF
EXTAL		—	10	—	
All Other (A/D Converter Characteristics)		—	—	—	
Low Voltage Recover	LVR	—	—	4.75	Vdc
Low Voltage Inhibit	LVI	—	3.5	—	Vdc

Note: Port D Analog Inputs, when selected, $C_{in} = 25 \text{ pF}$ for the first 5 out of 30 cycles.

*Due to internal biasing only.

A/D CONVERTER CHARACTERISTICS ($V_{CC} = +5.25 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ - 70^\circ \text{C}$ Unless Otherwise Noted)

Characteristic	Min	Typ	Max	Unit	Comments
Resolution	8	8	8	Bits	
Non-Linearity	—	—	$\pm 1/2$	LSB	
Quantizing Error	—	—	$\pm 1/2$	LSB	
Conversion Range	V_{RL}	—	V_{RH}	V	
V_{RH}	4	—	5	V	A/D Accuracy may decrease proportionately as V_{RH} is reduced below 4.0 V. The sum of V_{RH} and V_{RL} must not exceed 5.0 V.
V_{RL}	0.0	—	0.2	V	
Conversion Time	30	30	30	t_{cyc}	Includes Sampling Time
Monotonicity	Inherent				
Zero Input Reading	00	00	01	hexadecimal	$V_{in} = 0$
Ratiometric Reading	FF	FF	FF	hexadecimal	$V_{in} = V_{RH}$
Sample Time	5	5	5	t_{cyc}	
Sample/Hold Capacitance, Input	—	—	25	pF	
Analog Input Voltage	V_{RL}	—	V_{RH}	V	Neg. transients not allowed at any time during conversion

SWITCHING CHARACTERISTICS ($V_{CC} = +5.25 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ - 70^\circ \text{C}$ Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	f_{osc}	0.4	—	4.2	MHz
Cycle Time ($4/f_{osc}$)	t_{cyc}	0.95	—	10	μs
INT Pulse Width	t_{IWL} , t_{IWH}	$t_{cyc} + 250$	—	—	ns
RESET Pulse Width	t_{RWL}	$t_{cyc} + 250$	—	—	ns
Delay Time Reset (External Cap = $1 \mu\text{F}$ (for $\pm 5^\circ$ Accuracy)	t_{RHL}	—	100	—	ms
INT Zero Cross Detect Input Frequency	f_{INT}	0.03	—	1	kHz
External Clock Input Duty Cycle (Pin 5)	—	40	50	60	%

PORT ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.25 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ \text{ to } 70^\circ \text{C}$ Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A					
Output Low Voltage $I_{load} = 1.6 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output High Voltage $I_{load} = -100 \text{ } \mu\text{Adc}$	V_{OH}	2.4	—	—	Vdc
Output High Voltage $I_{load} = -10 \text{ } \mu\text{Adc}$	V_{OH}	$V_{CC} - 1$	—	—	Vdc
Input High Voltage $I_{load} = -300 \text{ } \mu\text{Adc}$ (max)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage $I_{load} = -500 \text{ } \mu\text{Adc}$ (max)	V_{IL}	-0.3	—	+0.8	Vdc
Off-State Input Current, Input 0.8 V	I_{IH}	—	—	-300	μAdc
Off-State Input Current, Input 0.2 V	I_{IL}	—	—	-500	μAdc
Port B					
Output Low Voltage $I_{load} = 3.2 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output Low Voltage $I_{load} = 10 \text{ mAdc}$ (sink)	V_{OL}	—	—	1.0	Vdc
Output High Voltage $I_{load} = -200 \text{ } \mu\text{Adc}$	V_{OH}	2.4	—	—	Vdc
Darlington Current Drive (Source) $V_O = 1.5 \text{ Vdc}$	I_{OH}	-1.0	—	-10	mAdc
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Off-State Input Current	I_{TSI}	—	2	50	μAdc
Port C					
Output Low Voltage $I_{load} = 1.6 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output High Voltage $I_{load} = -100 \text{ } \mu\text{Adc}$	V_{OH}	2.4	—	—	Vdc
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Off-State Input Current	I_{TSI}	—	2	50	μAdc
Port D (Input Only)					
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	V_{RL}	—	+0.8	Vdc
Input Current					
Timer at $V_{in} = (0.4 \text{ to } 2.4 \text{ Vdc})$	I_{in}	—	—	20	μAdc

POWER CONSIDERATIONS

The average chip junction temperature, T_J , in $^\circ\text{C}$ can be obtained from

$$T_J = T_A + [(P_D + P_{IO}) \cdot \theta_{JA}] \quad (1)$$

Where

T_A = ambient temperature, $^\circ\text{C}$,

θ_{JA} = package thermal resistance, $^\circ\text{C}/\text{watt}$,

P_{IO} = output port power dissipation, watts,

$$= \Sigma(V_{CC} - V_{OH})(|I_{OH}|) + \Sigma(V_{OL})(|I_{OL}|) + \Sigma(V_{CC} - V_{IL})(|I_{IL}|) + \Sigma(V_{CC} - V_{IH})(|I_{IH}|)$$

P_D = chip internal power dissipation, watts.

An approximate relationship between P_D and T_J is

$$P_D = K(T_J + 273) - 0.96 \quad (2)$$

where K is a constant pertaining to the particular part, which may be determined from measurement of P_D immediately after turn-on (i.e., $T_J = T_A$). Using this value of K , then, for any T_A , P_{IO} , and θ_{JA} , the values of P_D and T_J may be obtained for a particular part by an iterative procedure using these two equations. For example, assume that $\theta_{JA} = 50^\circ\text{C}/\text{W}$, maximum $P_{IO} = 150 \text{ mW}$, and P_D is measured for the part to be 400 mW at turn-on at room temperature (25°C). To determine the T_J at a $T_A = 40^\circ\text{C}$, the following iterative procedure is used. First,

$$\text{Calculate } K \text{ from equation (2): } K = (0.400)/(25 + 273) - 0.96 = 94.9.$$

$$\text{Estimate } T_J \text{ from equation (1): } T_J = 40 + [(0.400 + 0.150) \cdot 50] = 67.5^\circ\text{C}$$

$$\text{Substitute this } T_J \text{ into eq. (2): } P_D = 94.9(67.5 + 273) - 0.96 = 0.352 \text{ W.}$$

$$\text{Substitute this } P_D \text{ into eq. (1): } T_J = 40 + [(0.352 + 0.150) \cdot 50] = 65.1^\circ\text{C.}$$

$$\text{Substitute this } T_J \text{ into eq. (2): } P_D = 94.9(65.1 + 273) - 0.96 = 0.345 \text{ W.}$$

$$\text{Substitute this } P_D \text{ into eq. (1): } T_J = 40 + [(0.354 + 0.150) \cdot 50] = 65.2^\circ\text{C.}$$

Since the last two values obtained for T_J are essentially the same, the iterative process is complete, with the solution $T_J = 65.2^\circ\text{C}$.

FIGURE 2 — MC6805R2 HMOS MICROCOMPUTER BLOCK DIAGRAM

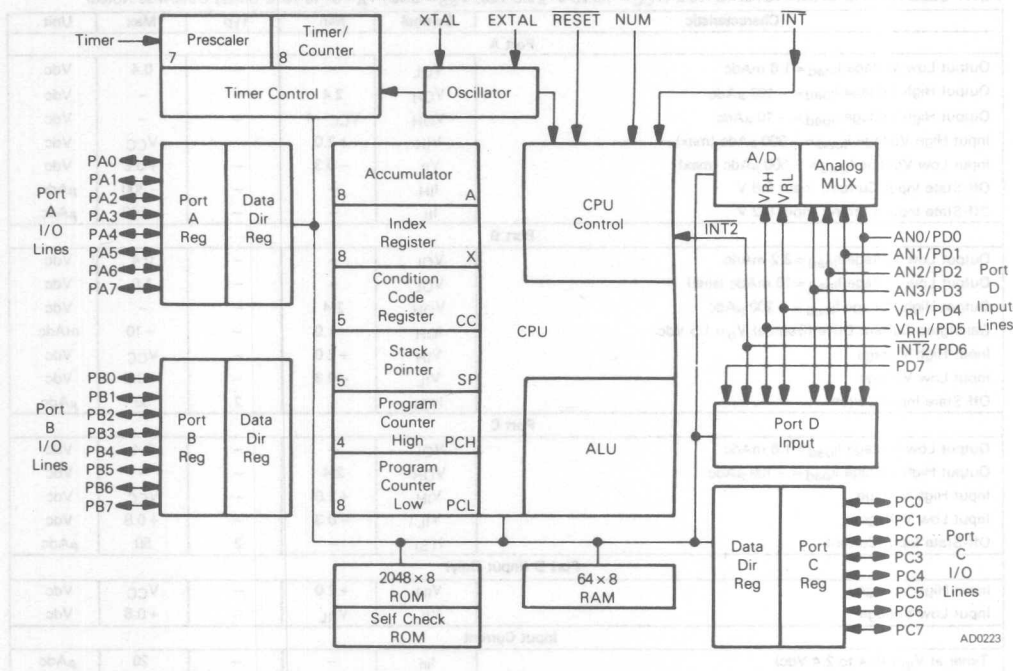


FIGURE 3 — TTL EQUIV. TEST LOAD (PORT B)

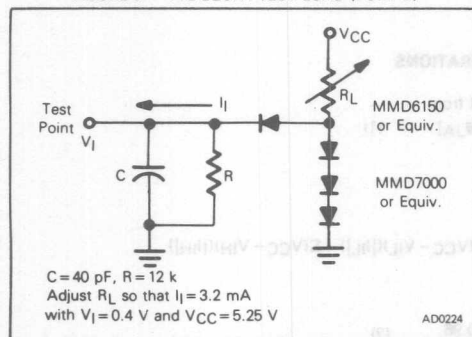


FIGURE 4 — CMOS EQUIV. TEST LOAD (PORT A)

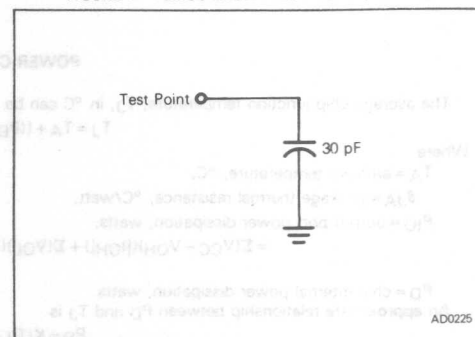
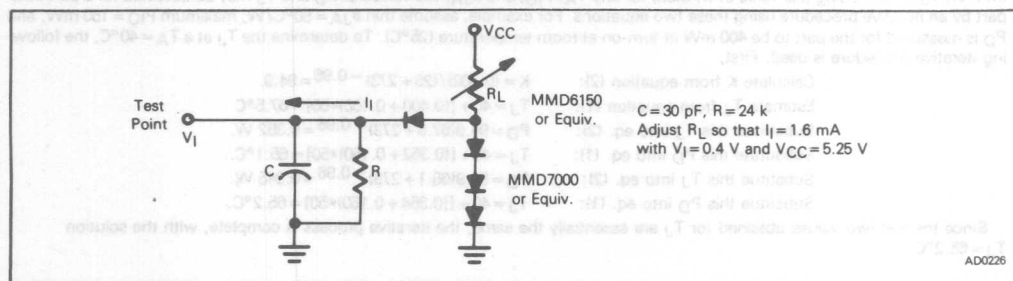


FIGURE 5 — TTL EQUIV. TEST LOAD (PORTS A AND C)



SIGNAL DESCRIPTION — The input and output signals for the MCU, shown in Figure 1, are described in the following paragraphs.

VCC AND VSS — Power is supplied to the MCU using these two pins. VCC is +5.25 Vdc \pm 0.5 V. VSS is the ground connection.

INT — This pin provides the capability for applying an external interrupt to the MCU. Refer to INTERRUPTS for additional information.

XTAL AND EXTAL — These pins provide control input for the on-chip clock circuit. A crystal (AT cut, 4.0 MHz maximum) or a resistor, depending on manufacturing mask option, can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Refer to INTERNAL CLOCK GENERATOR OPTIONS for recommendations about these inputs.

TIMER — This pin allows an external input to be used to decrement the internal timer circuitry. Refer to TIMER for additional information about the timer circuitry.

RESET — This pin allows resetting of the MCU at times other than the automatic resetting capability already in the MCU. Refer to RESETS for additional information.

NUM (Non-User Mode) — This pin is not for user application and should be connected to ground.

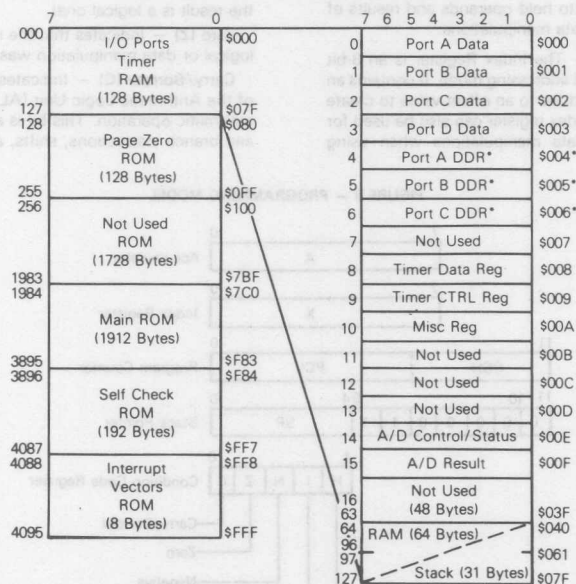
INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7) — These 32 lines are arranged into four 8-bit ports (A, B, C, and D). Ports A, B, and C are programmable as

either inputs or outputs, under software control of the data direction registers. Port D has four analog inputs, two voltage reference inputs (VRH, VRL), an INT2 input, and a digital input. All port D lines can also be directly read and used as binary inputs. If any analog input is used, then the voltage reference pins (VRH, VRL) must be used in the analog mode. Refer to INPUT/OUTPUT, A/D CONVERTER, and INTERRUPTS for additional information.

MEMORY — The MCU is capable of addressing 4096 bytes of memory and I/O registers with its program counter. The MCU has implemented 2316 of these bytes. This consists of: 2048 user ROM bytes, 192 self test ROM bytes, 64 user RAM bytes, and 12 I/O bytes; see Figure 6 for the Memory Map. The user ROM has been split into three areas. The first area is memory locations \$080 to \$0FF, and allows the user to access these ROM locations utilizing the direct addressing mode. The main user ROM area is from \$7C0 to \$F37. The last 8 ROM memory locations at the top of memory are for the interrupt vectors.

The MCU reserves the first 16 memory locations for I/O features, of which 12 have been implemented. These locations are used for the ports, the port DDRs, the timer, the INT2 miscellaneous register and the A/D. Refer to Table 3 for the register configuration of these locations. Sixty-four bytes of user RAM are provided. The last 31 bytes of user RAM \$061 to \$07F are SHARED with the stack area. The stack area must be used with care if data is stored there.

FIGURE 6 — MCU MEMORY MAP

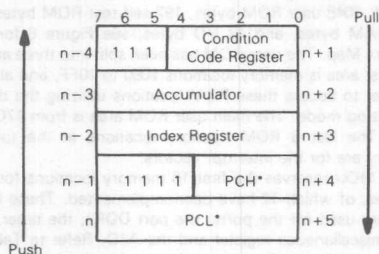


*Caution: Data Direction Registers (DDRs) are write-only; they read as \$FF.

AD0227

The shared stack area is used during the processing of an interrupt. The contents of the MCU registers are pushed on to the stack in the order shown in Figure 7. Since the Stack Pointer decrements during pushes, the low order byte (PCL) of the Program Counter is stacked first; then the high order four bits (PCH) are stacked. This ensures that the program counter is loaded correctly as the stack pointer increments when it pulls data from the stack. A subroutine call will cause only the Program Counter (PCL, PCH) contents to be pushed onto the stack.

FIGURE 7 — INTERRUPT STACKING ORDER



*For subroutine calls, only PCH and PCL are stacked

AD0228

REGISTERS — The MCU has five registers available to the programmer. They are shown in Figure 8 and are explained in the following paragraphs.

ACCUMULATOR (A) — The Accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

INDEX REGISTER (X) — The Index Register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit address that may be added to an offset value to create an effective address. The index register can also be used for limited calculations and data manipulations when using

read/modify/write instructions. When not required for Index Addressing, the Index Register can be used as a temporary storage area.

PROGRAM COUNTER (PC) — The Program Counter is a 12-bit register that contains the address of the next instruction to be executed.

STACK POINTER (SP) — The Stack Pointer is a 12-bit register that contains the address of the next free location on the stack. During an MCU reset, or the Reset Stack Pointer (RSP) instruction, the Stack Pointer is set to location \$07F. The Stack Pointer is then decremented as data is pushed on to the stack and incremented as data is then pulled from the stack. The seven most significant bits of the Stack Pointer are permanently set to 000011. Subroutines and interrupts may be nested down to location \$061 which allows the programmer to use up to 15 levels of subroutine calls (less if interrupts are allowed).

CONDITION CODE REGISTER (CC) — The Condition Code Register is a 5-bit register in which each bit is used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each bit is explained in the following paragraphs.

Half Carry (H) — Set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

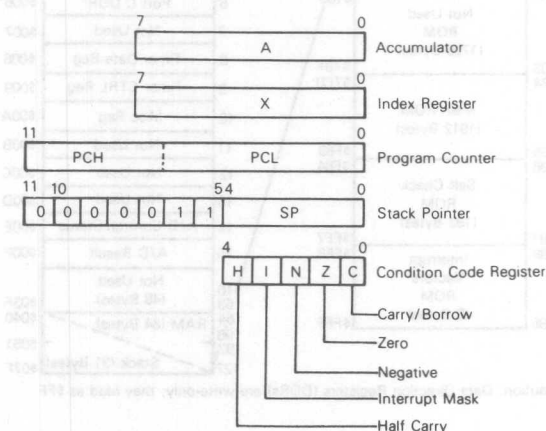
Interrupt (I) — When this bit is set, the timer and external interrupts (INT and INT2) are masked. If an interrupt occurs while this bit is set, the interrupt is latched and will be processed as soon as the interrupt bit is cleared.

Negative (N) — Indicates that the result of the last arithmetic, logical or data manipulation was negative (bit 7 in the result is a logical one).

Zero (Z) — Indicates that the result of the last arithmetic, logical or data manipulation was zero.

Carry/Borrow (C) — Indicates that a carry or borrow out of the Arithmetic Logic Unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

FIGURE 8 — PROGRAMMING MODEL



AD0229

TIMER — The MCU timer circuitry is shown in Figure 9. The 8-bit counter is loaded under program control and is decremented toward zero by the clock input. When the timer reaches zero, the timer interrupt request bit (bit 7) in the Timer Control/Status Register (TCSR) is set. The timer interrupt can be masked by setting the timer interrupt mask bit (bit 6) in the TCSR. The interrupt bit (I-bit) in the Condition Code Register will also prevent a timer interrupt from being processed. The MCU responds to this interrupt by saving the present MCU state in the stack, fetching the timer interrupt vector from locations \$FF8 and \$FF9 and executing the interrupt routine (see Figure 16). **THE TIMER INTERRUPT REQUEST BIT MUST BE CLEARED BY SOFTWARE.** The timer and INT2 share the same interrupt vector. **THE INTERRUPT ROUTINE MUST CHECK THE REQUEST BITS TO DETERMINE THE SOURCE OF THE INTERRUPT.**

The clock input to the timer can be from an external source (decrementing of Timer Counter occurs on a positive transition of the external source) applied to the TIMER input pin or it can be the internal $\phi 2$ signal. When the $\phi 2$ signal is used as the source, it can be gated by an input applied to the TIMER input pin allowing the user to easily perform pulse-width measurements. (Note: For ungated $\phi 2$ clock input to the timer prescaler, the timer pin should be tied to V_{CC} .) The source of the clock input is one of the options that has to be specified before manufacture of the MCU. A prescaler option can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before decrementing the counter. This prescaling option must also be specified before manufacturing begins. To avoid truncation errors, the prescaler is cleared when bit 3 of timer control register is written to a logic 1 (this bit always reads as a logic 0). The timer continues to count past zero, falling through to FF16 and then continuing the count. The count can be read at any time by monitoring the Timer Data Register (TDR). This allows a program to determine the length of time since a timer interrupt has occurred, and not disturb the counting process.

At Power-up or Reset, the prescaler and counter are ini-

tialized with all logical ones; the timer interrupt request bit (bit 7) is cleared and the timer interrupt request mask bit (bit 6) is set. Refer to Table 3 for MCU Register Configuration.

SELF CHECK — The self check capability of the MCU provides an internal check to determine if the part is functional. Connect the MCU as shown in Figure 10 and monitor the output of Port C, bit 3 for an oscillation of approximately 7 Hz. A 9 volt level on the timer input, Pin 8, energizes the ROM based self check feature.

Several of the self check subroutines can be called by a user program. They are the RAM, ROM and 4 channel A/D test. The timer routine may also be called if the timer input is the internal clock.

RAM Self Check Subroutine — Returns with the Z-bit clear if any error is detected; otherwise the Z-bit is set.

The RAM test must be called with the stack pointer at \$07F. When run, the test checks every RAM cell except for \$07F and \$07E which are assumed to contain the return address.

A and X are modified. All RAM locations except the top 2 are modified.

ROM Checksum Subroutine — Returns with Z-bit cleared if any error was found; otherwise Z = 1. X = 0 on return, and A will be zero if the test passed. RAM locations \$040-\$043 are overwritten.

A to D Converter Test — Returns with Z-bit cleared if any error was found; otherwise Z = 1.

A and X register contents are lost; X must be set to 4 before the call. X = 8 on return and A/D channel 7 is selected.

Timer Test — Return with Z-bit cleared if any error was found; otherwise Z = 1.

This runs a simple test on the timer. In order to work correctly as a user subroutine, the internal clock must be the clocking source and interrupts must be disabled. Also, on exit, the clock will be running and the interrupt mask not set so the caller must protect himself from interrupts if necessary.

FIGURE 9 — TIMER BLOCK DIAGRAM

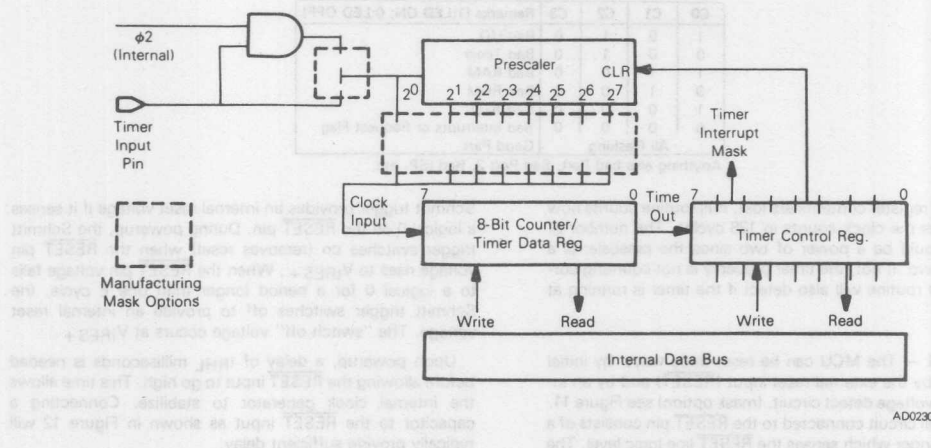
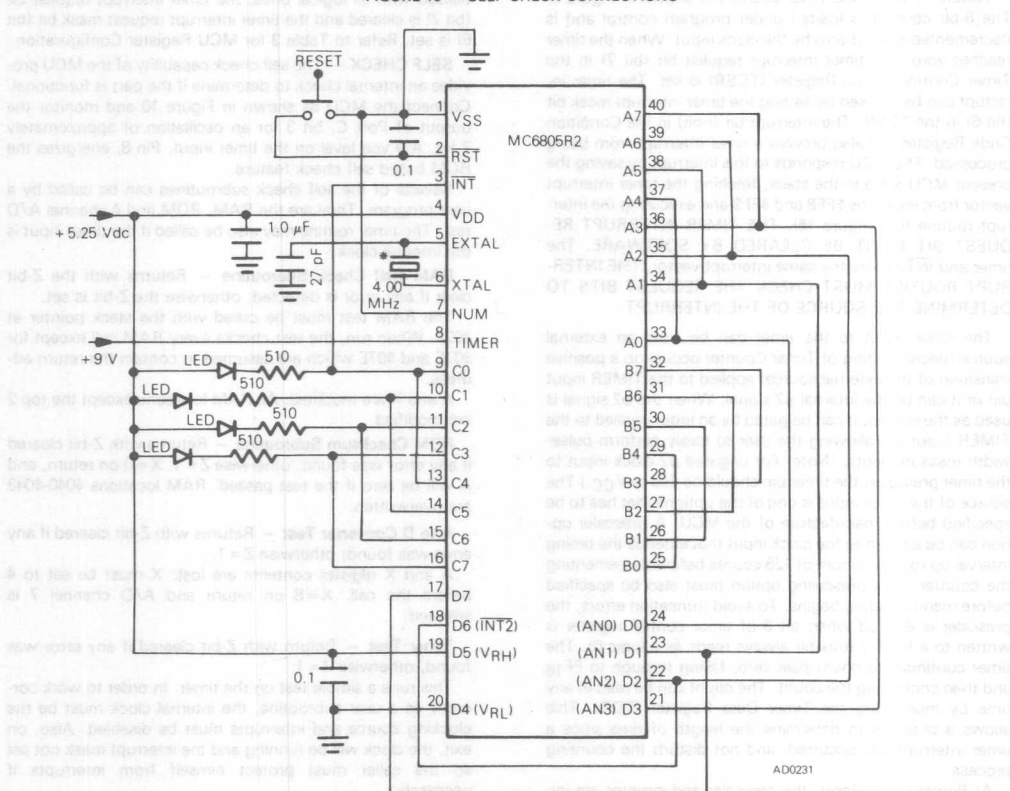


FIGURE 10 — SELF CHECK CONNECTIONS



*Use jumper if RC mask option is selected. This connection depends on clock oscillator mask option.

LED Meanings

C0	C1	C2	C3	Remarks [1:LED ON; 0:LED OFF]
1	0	1	0	Bad I/O
0	0	1	0	Bad Timer
1	1	0	0	Bad RAM
0	1	0	0	Bad ROM
1	0	0	0	Bad A/D
0	0	0	0	Bad Interrupts or Request Flag
All Flashing				Good Part

Anything else bad Part, Bad Port 3, Bad ISP, etc.

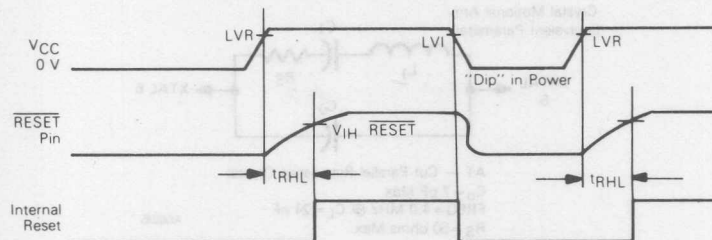
A and X register contents are lost, this routine counts how many times the clock counts in 128 cycles. The number of counts should be a power of two since the prescaler is a power of two. If not, the timer probably is not counting correctly. The routine will also detect if the timer is running at all.

RESETS — The MCU can be reset three ways: by initial powerup, by the external reset input (RESET) and by an internal low voltage detect circuit, (mask option) see Figure 11. The internal circuit connected to the RESET pin consists of a Schmitt trigger which senses the RESET line logic level. The

Schmitt trigger provides an internal reset voltage if it senses a logical 0 on the RESET pin. During powerup, the Schmitt trigger switches on (removes reset) when the RESET pin voltage rises to V_{RES+} . When the RESET pin voltage falls to a logical 0 for a period longer than one E cycle, the Schmitt trigger switches off to provide an internal reset voltage. The "switch off" voltage occurs at V_{RES+} .

Upon powerup, a delay of t_{RHL} milliseconds is needed before allowing the RESET input to go high. This time allows the internal clock generator to stabilize. Connecting a capacitor to the RESET input as shown in Figure 12 will typically provide sufficient delay.

FIGURE 11 — POWER AND RESET TIMING



AS0232

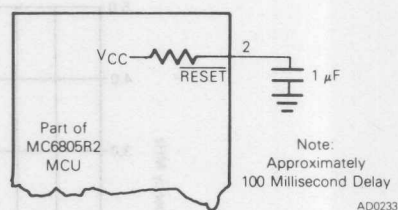
INTERNAL CLOCK GENERATOR OPTIONS — The internal clock generator circuit is designed to require a minimum of external components. A crystal or a resistor may be used to control the internal clock generator with varying degrees of stability. A manufacturing mask option is used to select the crystal or resistor operation.

The different connection methods are shown in Figure 13. Crystal specifications are given in Figure 14. A resistor selection graph is shown in Figure 15.

The crystal oscillator start-up time is a function of many variables: crystal parameters — especially R_s , oscillator load capacitances, IC parameters, ambient temperature, supply voltage, and supply voltage turn-on time.

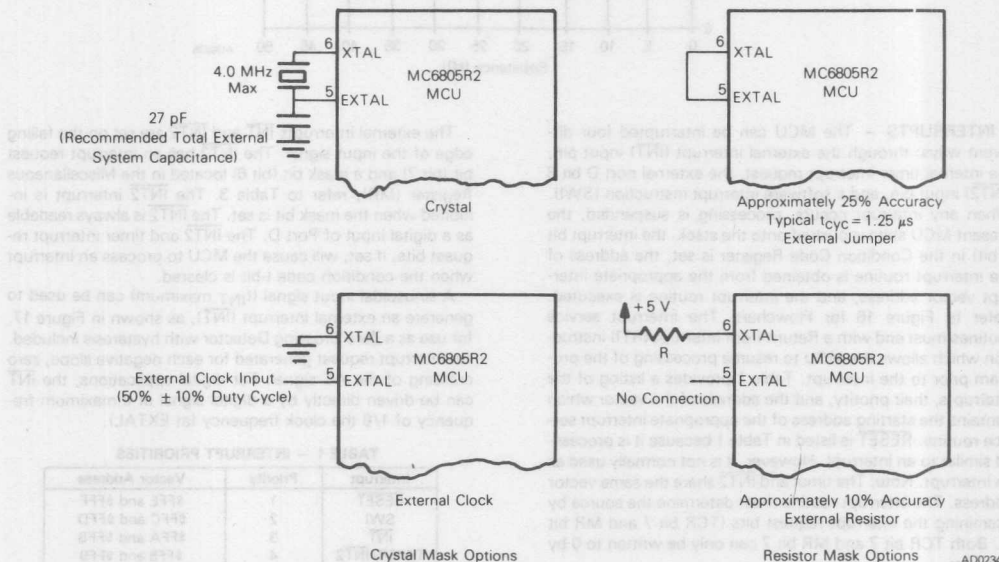
To ensure rapid oscillator start-up, the crystal characteristics should not exceed those recommended and the load capacitances should not exceed recommendations.

FIGURE 12 — POWERUP RESET DELAY CIRCUIT



AD0233

FIGURE 13 — INTERNAL CLOCK GENERATOR



AD0234

FIGURE 14 — CRYSTAL PARAMETERS

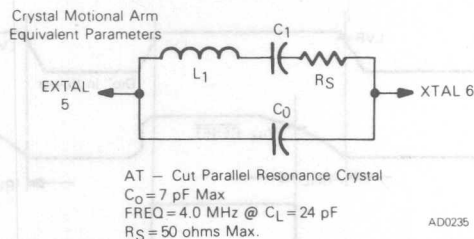
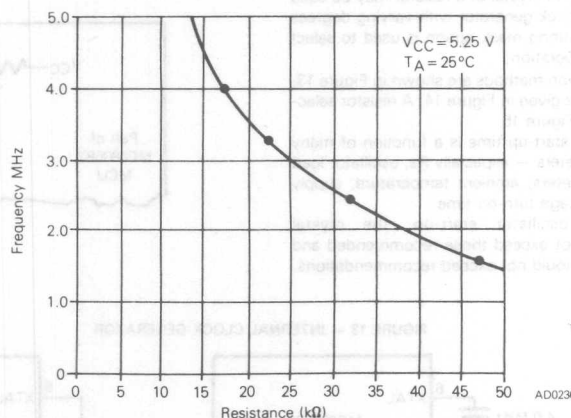


FIGURE 15 — TYPICAL RESISTOR SELECTION GRAPH



INTERRUPTS — The MCU can be interrupted four different ways: through the external interrupt ($\overline{\text{INT}}$) input pin, the internal timer interrupt request, the external port D bit 6 ($\overline{\text{INT2}}$) input pin, and a software interrupt instruction (SWI). When any interrupt occurs, processing is suspended, the present MCU state is pushed onto the stack, the interrupt bit (I-bit) in the Condition Code Register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. Refer to Figure 16 for Flowchart. The interrupt service routines must end with a Return from Interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt. Table 1 provides a listing of the interrupts, their priority, and the address of the vector which contains the starting address of the appropriate interrupt service routine. **RESET** is listed in Table 1 because it is processed similar to an interrupt. However, it is not normally used as an interrupt. Note: The timer and $\overline{\text{INT2}}$ share the same vector address. The interrupt routine must determine the source by examining the interrupt request bits (TCR bit 7 and MR bit 7). Both TCR bit 7 and MR bit 7 can only be written to 0 by software.

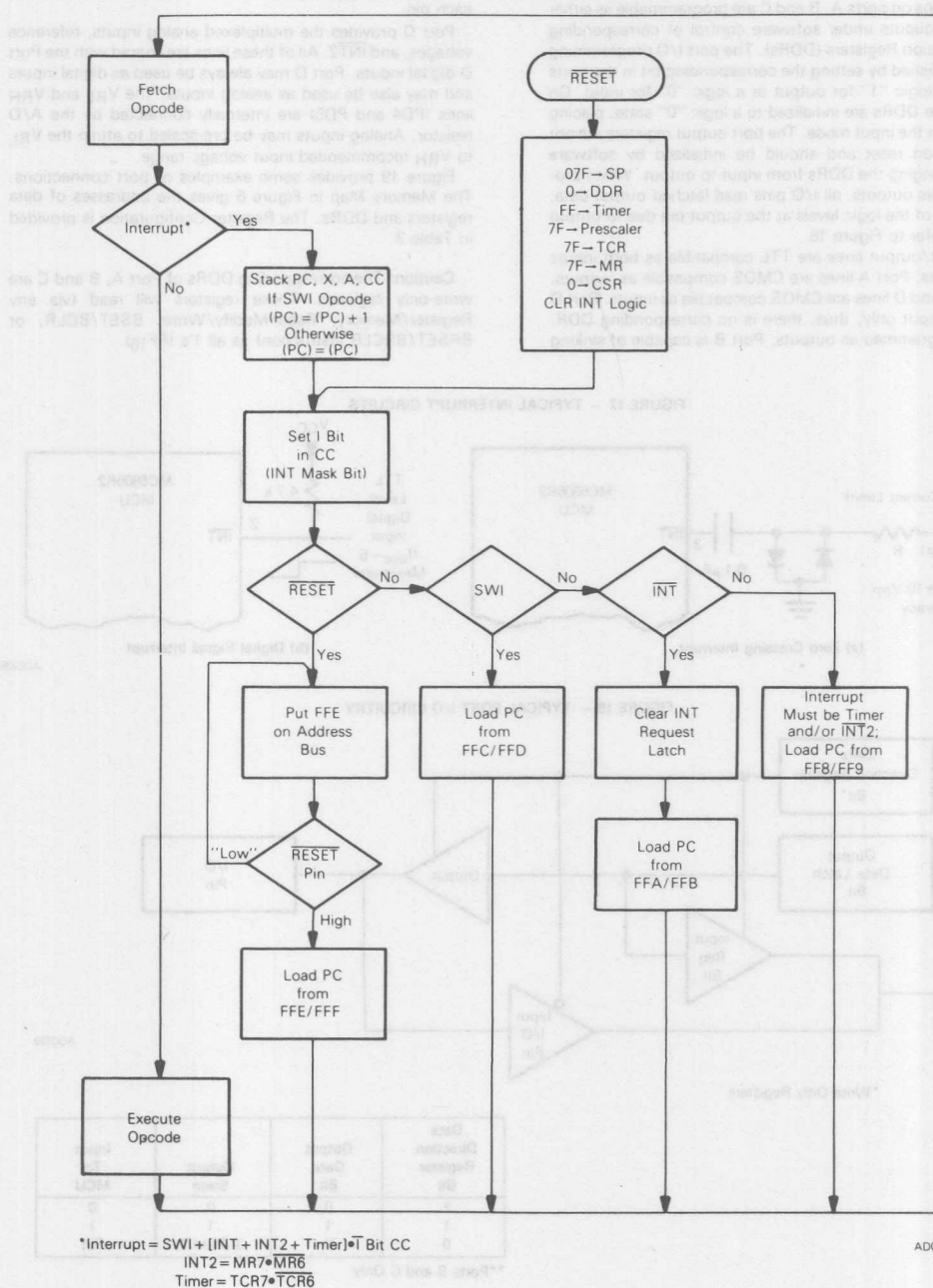
The external interrupts $\overline{\text{INT}}$ and $\overline{\text{INT2}}$ are set on the falling edge of the input signal. The $\overline{\text{INT2}}$ has an interrupt request bit (bit 7) and a mask bit (bit 6) located in the Miscellaneous Register (MR), refer to Table 3. The $\overline{\text{INT2}}$ interrupt is inhibited when the mask bit is set. The $\overline{\text{INT2}}$ is always readable as a digital input of Port D. The $\overline{\text{INT2}}$ and timer interrupt request bits, if set, will cause the MCU to process an interrupt when the condition code I-bit is cleared.

A sinusoidal input signal (f_{INT} maximum) can be used to generate an external interrupt ($\overline{\text{INT}}$), as shown in Figure 17, for use as a Zero Crossing Detector with hysteresis included. An interrupt request generated for each negative slope, zero crossing of the AC signal. For digital applications, the $\overline{\text{INT}}$ can be driven directly by a digital signal at a maximum frequency of 1/8 the clock frequency (at XTAL).

TABLE 1 — INTERRUPT PRIORITIES

Interrupt	Priority	Vector Address
RESET	1	\$FFE and \$FFF
SWI	2	\$FFC and \$FFD
$\overline{\text{INT}}$	3	\$FFA and \$FFB
TIMER/ $\overline{\text{INT2}}$	4	\$FF8 and \$FF9

FIGURE 16 — INTERRUPT PROCESSING FLOW CHART



AD0237

INPUT/OUTPUT — There are 32 input or input/output pins. All pins on ports A, B and C are programmable as either inputs or outputs under software control of corresponding Data Direction Registers (DDRs). The port I/O programming is accomplished by setting the corresponding bit in the ports DDR to a logic "1" for output or a logic "0" for input. On reset all the DDRs are initialized to a logic "0" state, placing the ports in the input mode. The port output registers are not initialized on reset and should be initialized by software before changing the DDRs from input to output. When programmed as outputs, all I/O pins read latched output data, regardless of the logic levels at the output pin due to output loading; refer to Figure 18.

All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs. Port B, C and D lines are CMOS compatible as inputs. Port D lines are input only; thus, there is no corresponding DDR. When programmed as outputs, Port B is capable of sinking

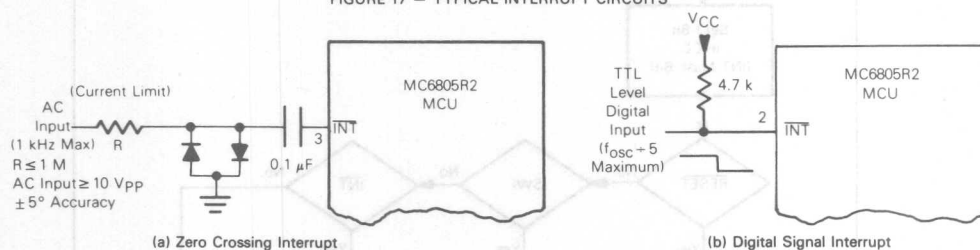
10 milliamperes on each pin and sourcing 1.0 milliamperes on each pin.

Port D provides the multiplexed analog inputs, reference voltages, and INT2. All of these lines are shared with the Port D digital inputs. Port D may always be used as digital inputs and may also be used as analog inputs. The V_{RL} and V_{RH} lines (PD4 and PD5) are internally connected by the A/D resistor. Analog inputs may be pre-scaled to attain the V_{RL} to V_{RH} recommended input voltage range.

Figure 19 provides some examples of port connections. The Memory Map in Figure 6 gives the addresses of data registers and DDRs. The Register Configuration is provided in Table 3.

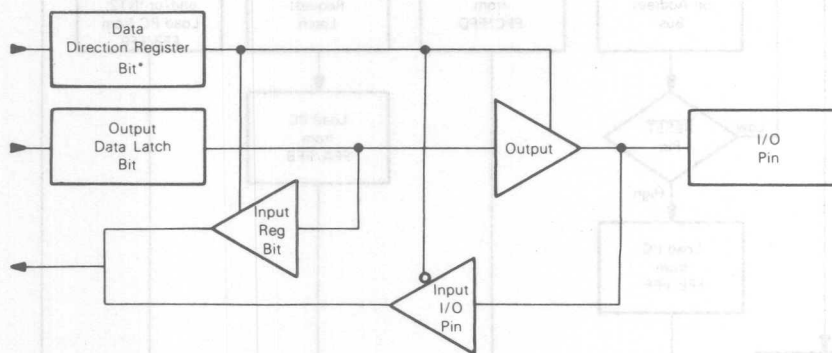
Caution: The corresponding DDRs of Port A, B and C are write-only registers. These registers will read (via any Register/Memory, Read/Modify/Write, BSET/BCLR, or BRSET/BRCLR instruction) as all 1's (FF16).

FIGURE 17 — TYPICAL INTERRUPT CIRCUITS



AD0238

FIGURE 18 — TYPICAL PORT I/O CIRCUITRY



AD0239

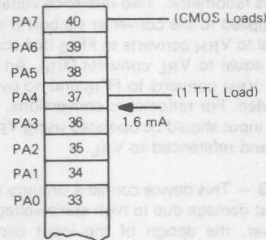
*Write Only Registers

Data Direction Register Bit	Output Data Bit	Output State	Input To MCU
1	0	0	0
1	1	1	1
0	X	3-State**	Pin

**Ports B and C Only

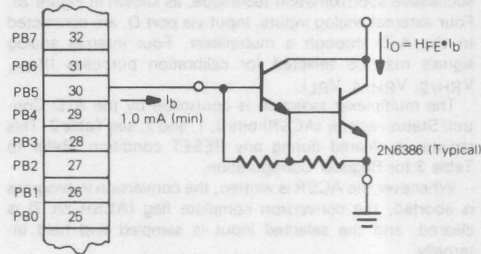
FIGURE 19 — TYPICAL PORT CONNECTIONS

Output Modes



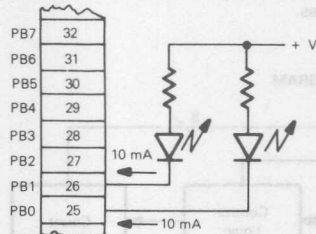
Port A, Bit 7 Programmed as Output, Driving CMOS Loads and Bit 4 Driving one TTL Load Directly.

(a)



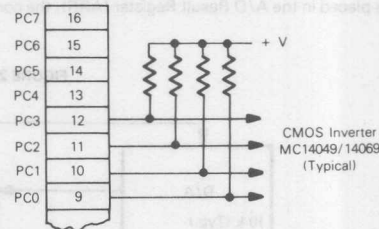
Port B, Bit 5 Programmed as Output, Driving Darlington-Base Directly.

(b)



Port B, Bit 0 and Bit 1 Programmed as Output, Driving LEDs Directly.

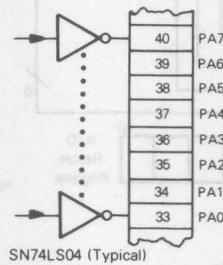
(c)



Port C, Bits 0-3 Programmed as Output, Driving CMOS Loads, Using External Pullup Resistors.

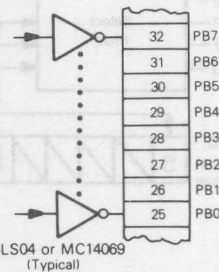
(d)

Input Modes



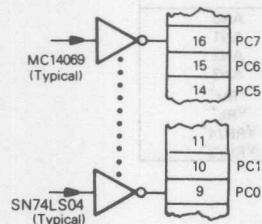
TTL Driving Port A Directly.

(e)



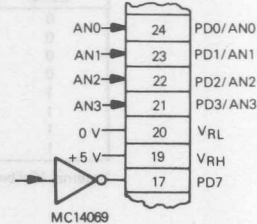
CMOS or TTL Driving Port B Directly.

(f)



CMOS and TTL Driving Port C Directly.

(g)



Port D used as 4-Channel A/D Input with Bit 7 used as CMOS Digital Input.

(h)

ANALOG TO DIGITAL CONVERTER (A/D) — The MCU has an 8-bit A/D converter implemented on the chip using a successive approximation technique, as shown in Figure 20. Four external analog inputs, input via port D, are connected to the A/D through a multiplexer. Four internal analog signals may be selected for calibration purposes (V_{RH} , $V_{RH}/2$, $V_{RH}/4$, V_{RL}).

The multiplexer selection is controlled by the A/D Control/Status register (ACSR) bits 0, 1, and 2, see Table 2. This register is cleared during any RESET condition. Refer to Table 3 for Register Configuration.

Whenever the ACSR is written, the conversion in progress is aborted, the conversion complete flag (ACSR bit 7) is cleared, and the selected input is sampled and held internally.

The converter operates continuously using 30 machine cycles to complete a conversion of the sampled analog input. When conversion is complete, the digitized sample or digital value is placed in the A/D Result Register (ARR), the conver-

sion complete flag is set, the selected input is sampled again, and a new conversion is started.

The A/D is ratiometric. Two reference voltages (V_{RH} and V_{RL}) are supplied to the converter via port D pins. An input voltage equal to V_{RH} converts to FF₁₆ (full scale) and an input voltage equal to V_{RL} converts to 00₁₆. An input voltage greater than V_{RH} converts to FF₁₆ and no overflow indication is provided. For ratiometric conversions, the source of each analog input should be operated using V_{RH} as the supply voltage and referenced to V_{RL} .

WARNING — This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, the design of the input circuitry for the analog reference voltage pins (19 and 20) does not offer the SAME level of protection. Precautions should be taken to avoid applications of any voltage higher than maximum rated voltage or handled in any environment producing high static voltages.

FIGURE 20 — A/D BLOCK DIAGRAM

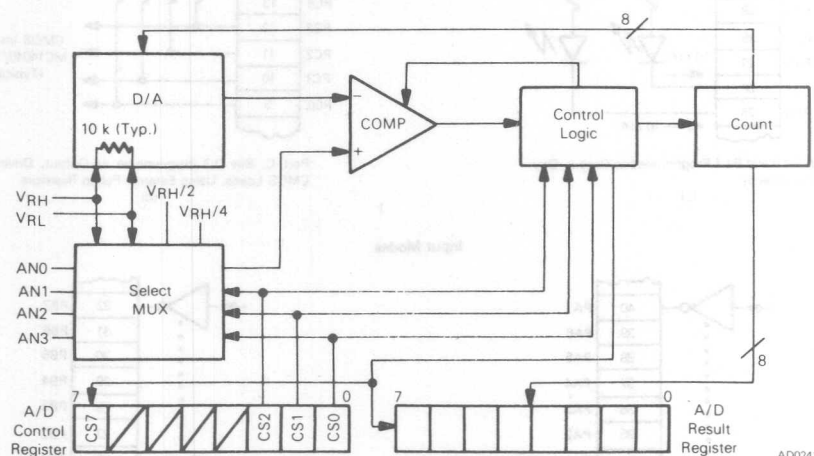


TABLE 2 — A/D INPUT MUX SELECTION

Control Status Register			Input Selected
CSR2	CSR1	CSR0	
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	V_{RH}^*
1	0	1	V_{RL}^*
1	1	0	$V_{RH}/4^*$
1	1	1	$V_{RH}/2^*$

*Internal (Calibration) levels

BIT MANIPULATION — The MCU has the ability to set or clear any single RAM or input/output bit (except the data direction registers, see Caution on page 12) with a single instruction (BSET, BCLR). Any bit in the page zero including ROM, except the DDRs, can be tested using the BRSET and BRCLR instructions and the program branches as a result of its state. The Carry bit (C) will equal the value of the bit referenced by BRSET or BRCLR. The capability to work with any bit in RAM, ROM or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines. The coding example in Figure 21 illustrates the usefulness of the bit manipulation and test instructions. Assume that the MCU is to communicate with an external serial device. The external device has a data ready signal, a data output line, and a clock line to clock data one bit at a time, LSB first, out of the device. The MCU waits until the data is ready, clocks the external device, picks up the data in the Carry Flag (C-bit), clears the clock line and finally accumulates the data bits in a RAM location.

ADDRESSING MODES

The M6805 Family has ten addressing modes available for use by the programmer. They are explained briefly in the following paragraphs. For additional details and graphical illustrations, refer to the M6805, M146805 Family Users Manual.

The term "effective address" (EA) is sometimes used in describing the addressing modes and it is defined as the address from which the argument for an instruction is fetched or stored.

IMMEDIATE — In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

DIRECT — In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes all on-chip RAM and I/O registers and up to 128 bytes of ROM. Direct addressing is an effective use of both memory and speed.

EXTENDED — In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler will automatically select the shortest form of the instruction.

RELATIVE — The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte following the opcode (the offset) is added

to the PC if, and only if, the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is limited to +129, -126 from the opcode address. The programmer need not worry about calculating the correct offset if he uses the Motorola assembler, since it calculates the proper offset and checks to see if it is within the span of the branch.

INDEXED, NO OFFSET — In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long and are therefore fast. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

INDEXED, 8-BIT OFFSET — In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. This addressing mode is useful in selecting the kth element in an n element table.

INDEXED, 16-BIT OFFSET — In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed, 8-bit offset; except that this three byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). As with direct and extended, the Motorola assembler will determine the shortest form of indexed addressing.

BIT SET/CLEAR — In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode and the byte following the opcode specifies the address of the byte in which the specified bit is to be set or cleared. Thus, any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two byte instruction. See Caution on page 12.

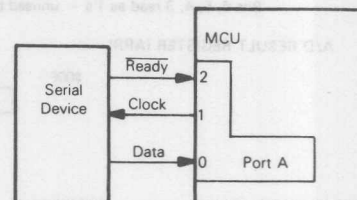
BIT TEST AND BRANCH — Bit test and branch is a combination of direct addressing and relative addressing. The bit and condition (set or clear) to be tested is part of the opcode and the address of the byte to be tested is in the single byte immediately following the opcode byte. The signed relative 8-bit offset is in the third byte and is added to the PC if the specified bit is set or clear in the specified memory location. This single three byte instruction allows the program to branch based on the condition of any readable bit in the first 256 location of memory. The span of branching is +130, -125 from the opcode address. See Caution on page 12.

INHERENT — In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are also included in this mode.

FIGURE 21 — BIT MANIPULATION EXAMPLE

```

*      BRSET  2,PORTA,* WAIT FOR READY
      BSET   1,PORTA  CLOCK NEXT BIT IN
      BRCLR  0,PORTA,NEXT PICKUP BIT IN C-BIT
NEXT   BCLR   1,PORTA  RETURN CLOCK LINE HIGH
      ASR    RAMLOC  MOVE C-BIT INTO RAM
  
```



AD0242

TABLE 3 — MCU REGISTER CONFIGURATION

PORT DATA DIRECTION REGISTER (DDR)

- (1) Write Only; reads as all 1's
 (2) 1 = Output, 0 = Input
 (3) Port A ADDR = \$0004
 Port B ADDR = \$0005
 Port C ADDR = \$0006
 Port D ADDR = None; Port D is Input only

PORT DATA REGISTER

- Port A ADDR = \$0004
 Port B ADDR = \$0005
 Port C ADDR = \$0006
 Port D ADDR = \$0007

TIMER CONTROL/STATUS REGISTER (TCSR)

7	6	5	4	3	2	1	0

- Bit 7 — Timer Interrupt Request Status Bit Set when TDR goes to zero; must be cleared by software
 Bit 6 — Timer Interrupt Mask Bit, 1 = timer masked (disabled)
 Bit 3 — Always reads as a 0; clears prescaler when written to a logic 1
 Bits 5, 4, 2, 1, 0 read 1's — unused bits

TIMER DATA REGISTER (TDR)

7	6	5	4	3	2	1	0
MSB							LSB

MISCELLANEOUS REGISTER (MR)

7	6	5	4	3	2	1	0

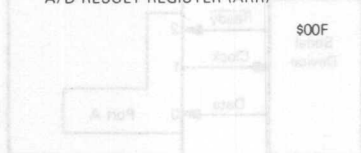
- Bit 7 — INT2 Interrupt Request Bit Set when falling edge detected on INT2 pin must be cleared by software
 Bit 6 — INT2 Interrupt Mask Bit 1 = INT2 Interrupt masked (disabled)
 Bit 5 — 0 Read as 1's — unused bits

A/D CONTROL/STATUS REGISTER (ACSR)

7	6	5	4	3	2	1	0

- Bit 7 — Conversion complete status FLAG Set when conversion is complete; Cleared ONLY ON A WRITE TO ACSR
 READABLE, NOT WRITABLE
 Bits 2, 1, 0 — A/D input Mux Selection (see Table 2)
 Bits 6, 5, 4, 3 read as 1's — unused bits

A/D RESULT REGISTER (ARR)



7	6	5	4	3	2	1	0
MSB							LSB

INSTRUCTION SET

The MCU has a set of 59 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

BRANCH INSTRUCTIONS — The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 4.

BIT MANIPULATION INSTRUCTIONS — These instructions are used on any bit in the first 256 bytes of the memory, see Caution on page 12. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 5.

REGISTER/MEMORY INSTRUCTIONS — Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is ob-

tained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 6.

READ/MODIFY/WRITE INSTRUCTIONS — These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register, see Caution on page 12. The test for negative or zero (TST) instruction is included in the read/modify/write instruction even though it does not perform the write. Refer to Table 7.

CONTROL INSTRUCTIONS — The control instructions control the MCU operations during program execution. Refer to Table 8.

ALPHABETICAL LISTING — The complete instruction set is given in alphabetical order in Table 9.

OPCODE MAP — Table 10 is an opcode map for the instructions used on the MCU.

TABLE 4 — BRANCH INSTRUCTIONS

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	HMOS/CMOS # Of Cycles
Branch Always	BRA	20	2	4/3
Branch Never	BRN	21	2	4/3
Branch IFF Higher	BHI	22	2	4/3
Branch IFF Lower or Same	BLS	23	2	4/3
Branch IFF Carry Clear	BCC	24	2	4/3
(Branch IFF Higher or Same)	(BHS)	24	2	4/3
Branch IFF Carry Set	BCS	25	2	4/3
(Branch IFF Lower)	(BLO)	25	2	4/3
Branch IFF Not Equal	BNE	26	2	4/3
Branch IFF Equal	BEQ	27	2	4/3
Branch IFF Half Carry Clear	BHCC	28	2	4/3
Branch IFF Half Carry Set	BHCS	29	2	4/3
Branch IFF Plus	BPL	2A	2	4/3
Branch IFF Minus	BMI	2B	2	4/3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	4/3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	4/3
Branch IFF Interrupt Line is Low	BIL	2E	2	4/3
Branch IFF Interrupt Line is High	BIH	2F	2	4/3
Branch to Subroutine	BSR	AD	2	8/6

TABLE 5 — BIT MANIPULATION INSTRUCTIONS

Function	Mnemonic	Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	HMOS/CMOS # of Cycles
Branch IFF Bit n is set	BRSET n (n = 0...7)	—	—	—	2 • n	3	10/5
Branch IFF Bit n is clear	BRCLR n (n = 0...7)	—	—	—	01 + 2 • n	3	10/5
Set Bit n	BSET n (n = 0...7)	10 + 2 • n	2	7/5	—	—	—
Clear bit n	BCLR n (n = 0...7)	11 + 2 • n	2	7/5	—	—	—

TABLE 6 — REGISTER/MEMORY INSTRUCTIONS

Function	Mnem.	Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
		Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)
Load A from Memory	LDA	A6	2	2/2	B6	2	4/3	C6	3	5/4	F6	1	4/3	E6	2	5/4	D6	3	6/5
Load X from Memory	LDX	AE	2	2/2	BE	2	4/3	CE	3	5/4	FE	1	4/3	EE	2	5/4	DE	3	6/5
Store A in Memory	STA	—	—	—	B7	2	5/4	C7	3	6/5	F7	1	5/4	E7	2	6/5	D7	3	7/6
Store X in Memory	STX	—	—	—	BF	2	5/4	CF	3	6/5	FF	1	5/4	EF	2	6/5	DF	3	7/6
Add Memory to A	ADD	AB	2	2/2	BB	2	4/3	CB	3	5/4	FB	1	4/3	EB	2	5/4	DB	3	6/5
Add Memory and Carry to A	ADC	A9	2	2/2	B9	2	4/3	C9	3	5/4	F9	1	4/3	E9	2	5/4	D9	3	6/5
Subtract Memory	SUB	A0	2	2/2	B0	2	4/3	C0	3	5/4	F0	1	4/3	E0	2	5/4	D0	3	6/5
Subtract Memory from A with Borrow	SBC	A2	2	2/2	B2	2	4/3	C2	3	5/4	F2	1	4/3	E2	2	5/4	D2	3	6/5
AND Memory to A	AND	A4	2	2/2	B4	2	4/3	C4	3	5/4	F4	1	4/3	E4	2	5/4	D4	3	6/5
OR Memory with A	ORA	AA	2	2/2	BA	2	4/3	CA	3	5/4	FA	1	4/3	EA	2	5/4	DA	3	6/5
Exclusive OR Memory with A	EOR	A8	2	2/2	B8	2	4/3	C8	3	5/4	F8	1	4/3	E8	2	5/4	D8	3	6/5
Arithmetic Compare A with Memory	CMP	A1	2	2/2	B1	2	4/3	C1	3	5/4	F1	1	4/3	E1	2	5/4	D1	3	6/5
Arithmetic Compare X with Memory	CPX	A3	2	2/2	B3	2	4/3	C3	3	5/4	F3	1	4/3	E3	2	5/4	D3	3	6/5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2/2	B5	2	4/3	C5	3	5/4	F5	1	4/3	E5	2	5/4	D5	3	6/5
Jump Unconditional	JMP	—	—	—	BC	2	3/2	CC	3	4/3	FC	1	3/2	EC	2	4/3	DC	3	5/4
Jump to Subroutine	JSR	—	—	—	BD	2	7/6	CD	3	8/6	FD	1	7/5	ED	2	8/7	DD	3	9/7

NOTE: The cycles column actually shows the number of HMOS/CMOS cycles (e.g., 4/3 indicates 4 HMOS cycles or 3 CMOS cycles).

TABLE 7 — READ/MODIFY/WRITE INSTRUCTIONS

Function	Mnem.	Addressing Modes											
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)		
		Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)
Increment	INC	4C	1	4/3	5C	1	4/3	3C	2	6/5	7C	1	6/5
Decrement	DEC	4A	1	4/3	5A	1	4/3	3A	2	6/5	7A	1	6/5
Clear	CLR	4F	1	4/3	5F	1	4/3	3F	2	6/5	7F	1	6/5
Complement	COM	43	1	4/3	53	1	4/3	33	2	6/5	73	1	6/5
Negate (2's complement)	NEG	40	1	4/3	50	1	4/3	30	2	6/5	70	1	6/5
Rotate Left Thru Carry	ROL	49	1	4/3	59	1	4/3	39	2	6/5	79	1	6/5
Rotate Right Thru Carry	ROR	46	1	4/3	56	1	4/3	36	2	6/5	76	1	6/5
Logical Shift Left	LSL	48	1	4/3	58	1	4/3	38	2	6/5	78	1	6/5
Logical Shift Right	LSR	44	1	4/3	54	1	4/3	34	2	6/5	74	1	6/5
Arithmetic Shift Right	ASR	47	1	4/3	57	1	4/3	37	2	6/5	77	1	6/5
Test for Negative or Zero	TST	4D	1	4/3	5D	1	4/3	3D	2	6/4	7D	1	6/4

NOTE: The cycles column actually shows the number of HMOS/CMOS cycles (e.g., 4/3 indicates 4 HMOS cycles or 3 CMOS cycles).

TABLE 8 — CONTROL INSTRUCTIONS

Function	Mnemonic	Inherent		
		Op Code	# Bytes	HMOS/CMOS # of Cycles
Transfer A to X	TAX	97	1	2/2
Transfer X to A	TXA	9F	1	2/2
Set Carry Bit	SEC	99	1	2/2
Clear Carry Bit	CLC	98	1	2/2
Set Interrupt Mask Bit	SEI	9B	1	2/2
Clear Interrupt Mask Bit	CLI	9A	1	2/2
Software Interrupt	SWI	83	1	11/10
Return from Subroutine	RTS	81	1	6/6
Return from Interrupt	RTI	80	1	9/9
Reset Stack Pointer	RSP	9C	1	2/2
No-Operation	NOP	9D	1	2/2
Enable IRQ, Stop Oscillator*	STOP	8E	1	-/2
Enable Interrupt, Stop Processor*	WAIT	8F	1	-/2

*CMOS Instructions

TABLE 9 — INSTRUCTION SET

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	*	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	*	Λ	Λ	Λ
AND		X	X	X		X	X	X			*	*	Λ	Λ	*
ASL	X		X			X	X				*	*	Λ	Λ	Λ
ASR	X		X			X	X				*	*	Λ	Λ	Λ
BCC					X						*	*	*	*	*
BCLR									X		*	*	*	*	*
BCS					X						*	*	*	*	*
BEQ					X						*	*	*	*	*
BHCC					X						*	*	*	*	*
BHCS					X						*	*	*	*	*
BHI					X						*	*	*	*	*
BHS					X						*	*	*	*	*
BIH					X						*	*	*	*	*
BIL					X						*	*	*	*	*
BIT		X	X	X		X	X	X			*	*	Λ	Λ	*
BLO					X						*	*	*	*	*
BLS					X						*	*	*	*	*
BMC					X						*	*	*	*	*
BMI					X						*	*	*	*	*
BMS					X						*	*	*	*	*
BNE					X						*	*	*	*	*
BPL					X						*	*	*	*	*
BRA					X						*	*	*	*	*
BRN					X						*	*	*	*	*
BRCLR										X	*	*	*	*	Λ
BRSET										X	*	*	*	*	Λ
BSET									X		*	*	*	*	*
BSR					X						*	*	*	*	*
CLC	X										*	*	*	*	0
CLI	X										*	0	*	*	*
CLR	X		X			X	X				*	*	0	1	*
CMP		X	X	X		X	X	X			*	*	Λ	Λ	Λ
COM	X		X			X	X				*	*	Λ	Λ	1
CPX		X	X	X		X	X	X			*	*	Λ	Λ	Λ

TABLE 9 — INSTRUCTION SET (CONTINUED)

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/Clear	Bit Test & Branch	H	I	N	Z	C
DEC	X		X			X	X				•	•	Δ	Δ	•
EOR		X	X	X		X	X	X			•	•	Δ	Δ	•
INC	X		X			X	X				•	•	Δ	Δ	•
JMP			X	X		X	X	X			•	•	•	•	•
JSR			X	X		X	X	X			•	•	•	•	•
LDA		X	X	X		X	X	X			•	•	Δ	Δ	•
LDX		X	X	X		X	X	X			•	•	Δ	Δ	•
LSL	X		X			X	X				•	•	Δ	Δ	Δ
LSR	X		X			X	X				•	•	0	Δ	Δ
NEQ	X		X			X	X				•	•	Δ	Δ	Δ
NOP	X										•	•	•	•	•
ORA		X	X	X		X	X	X			•	•	Δ	Δ	•
ROL	X		X			X	X				•	•	Δ	Δ	Δ
RSP	X										•	•	•	•	•
RTI	X										?	?	?	?	?
RTS	X										•	•	•	•	•
SBC		X	X	X		X	X	X			•	•	Δ	Δ	Δ
SEC	X										•	•	•	•	1
SEI	X										•	1	•	•	•
STA			X	X		X	X	X			•	•	Δ	Δ	•
STX			X	X		X	X	X			•	•	Δ	Δ	•
STOP*	X										•	1	•	•	•
SUB		X	X	X		X	X	X			•	•	Δ	Δ	Δ
SWI	X										•	0	•	•	•
TAX	X										•	•	•	•	•
TST	X		X			X	X				•	•	Δ	Δ	•
TXA	X										•	•	•	•	•
WAIT*	X										•	0	•	•	•

*CMOS Instructions Only

Condition Code Symbols

- H

Half Carry (From Bit 3)
- I

Interrupt Mask
- N

Negative (Sign Bit)
- Z

Zero
- C

Carry/Borrow
- Δ

Test and Set if True, Cleared Otherwise
- Not Affected
- ?

Load CC Register From Stack

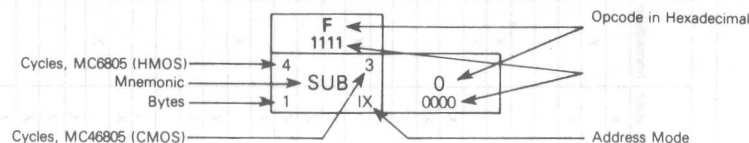
TABLE 10 — MC6805/MC146805 INSTRUCTION SET OPCODE MAP

		Bit Manipulation		Branch		Read/Modify/Write				Control		Register/Memory									
		BTB	BSC	REL	DJR	INH(A)	INH(X)	IX1	IX	INH	INH	IMM	DJR	EXT	IX2	IX1	IX				
Low	Hi	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	Hi	Low		
0	0000	BRSET0	BSET0	BRA	NEG	NEGA	NEGX	NEG	NEG	RTI		SUB	SUB	SUB	SUB	SUB	SUB		0		
1	0001	BCLR0	BCLR0	BRN						RTS		CMP	CMP	CMP	CMP	CMP	CMP		1		
2	0010	BRSET1	BSET1	BHI								SBC	SBC	SBC	SBC	SBC	SBC		2		
3	0011	BCLR1	BCLR1	BLS	COM	COMA	COMX	COM	COM	SWI		CPX	CPX	CPX	CPX	CPX	CPX		3		
4	0100	BRSET2	BSET2	BCC	LSR	LSRA	LSRX	LSR	LSR			AND	AND	AND	AND	AND	AND		4		
5	0101	BCLR2	BCLR2	BCS								BIT	BIT	BIT	BIT	BIT	BIT		5		
6	0110	BRSET3	BSET3	BNE	ROR	RORA	RORX	ROR	ROR			LDA	LDA	LDA	LDA	LDA	LDA		6		
7	0111	BCLR3	BCLR3	BEQ	ASR	ASRA	ASRX	ASR	ASR	TAX		STA	STA	STA	STA	STA	STA		7		
8	1000	BRSET4	BSET4	BHCC	LSL	LSLA	LSLX	LSL	LSL	CLC		EOR	EOR	EOR	EOR	EOR	EOR		8		
9	1001	BCLR4	BCLR4	BHCS	ROL	ROLA	ROLX	ROL	ROL	SEC		ADC	ADC	ADC	ADC	ADC	ADC		9		
A	1010	BRSET5	BSET5	BPL	DEC	DECA	DECX	DEC	DEC	CLI		ORA	ORA	ORA	ORA	ORA	ORA		A		
B	1011	BCLR5	BCLR5	BMI						SEI		ADD	ADD	ADD	ADD	ADD	ADD		B		
C	1100	BRSET6	BSET6	BMC	INC	INCA	INCX	INC	INC	RSP		JMP	JMP	JMP	JMP	JMP	JMP		C		
D	1101	BCLR6	BCLR6	BMS	TST	TSTA	TSTX	TST	TST	NOP		BSR	JSR	JSR	JSR	JSR	JSR		D		
E	1110	BRSET7	BSET7	BIL						STOP		LDX	LDX	LDX	LDX	LDX	LDX		E		
F	1111	BCLR7	BCLR7	BIH	CLR	CLRA	CLR X	CLR	CLR	WAIT		STX	STX	STX	STX	STX	STX		F		

Abbreviations for Address Modes

INH	Inherent
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset

LEGEND



A/D STANDALONE EVALUATION PROGRAM

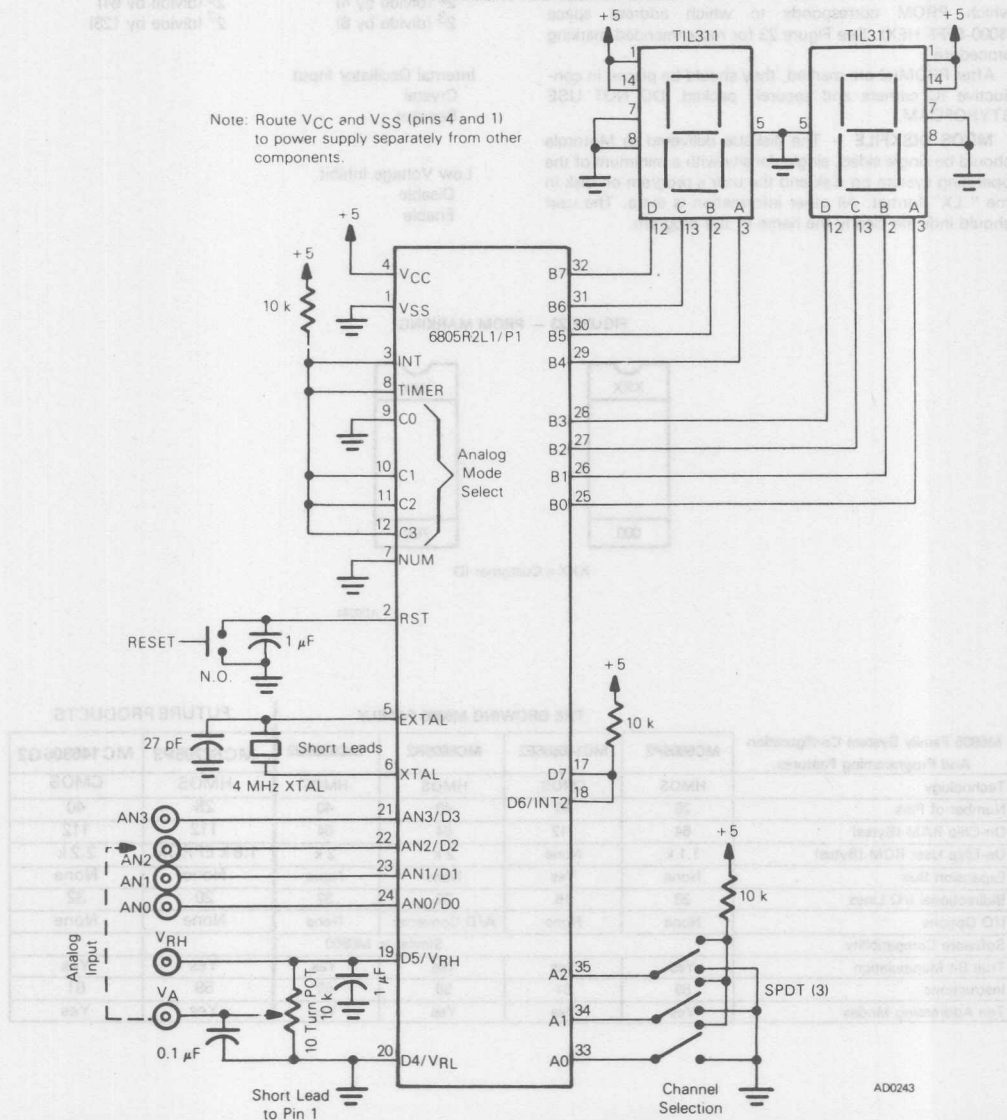
The MC6805R2L1/P1 is a device containing a separate, ROM program which can be used to evaluate the A/D section of an MC6805R2. This device, when connected as shown in Figure 22, allows the user to evaluate the standard A/D section and ascertain its feasibility in his own system.

The circuit in Figure 22 allows the user to select the analog input by setting the three switches (connected to A0, A1, A2) in various open-close combinations (refer to Table 2).

The parts required in Figure 22 are standard components

except for the 7-segment display and the 10-turn potentiometer. The two 7-segment displays (with decoders) are Texas Instruments TIL-311 displays and are connected to display the result in hexadecimal. The 10-turn potentiometer is connected across the voltage reference input. It allows for the application of a controlled voltage to one of the analog inputs. This connection can be made using pin-and-jack jumpering from the 10-turn potentiometer to one of the AN0-AN3 inputs.

FIGURE 22 — M6805R2L1/P1 EVALUATION CHIP —
STANDALONE A/D TEST DIAGRAM



ORDERING INFORMATION

The following information is required when ordering a custom MCU. This information may be transmitted to Motorola in any of the following media:

PROM(s)
MDOS disk file

To initiate a ROM pattern for the MCU, it is necessary to first contact your local field service office, local sales person or your local Motorola representative.

PROMs — The MCM2708 or MCM2716 type PROMs, programmed with the customer program (positive logic sense for address and data), may be clearly marked to indicate which PROM corresponds to which address space (\$000-\$FFF HEX). See Figure 23 for recommended marking procedure.

After PROM(s) are marked, they should be placed in conductive IC carriers and securely packed. DO NOT USE STYROFOAM.

MDOS DISKFILE — The diskette delivered to Motorola should be single sided, single density with a minimum of the operating system on disk and the user's program on disk in the ".LX" format. All other information is extra. The user should indicate clearly the name of the program.

Option List

Select the options for your MCU from the following list. A manufacturing mask will be generated from this information.

ROM Mask

Timer Clock Source
Internal $\phi 2$ clock
TIMER input pin (8)

Timer Prescaler

2^0 (divide by 1)	2^4 (divide by 16)
2^1 (divide by 2)	2^5 (divide by 32)
2^2 (divide by 4)	2^6 (divide by 64)
2^3 (divide by 8)	2^7 (divide by 128)

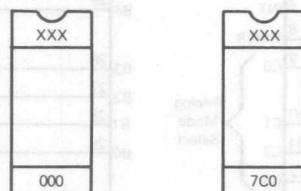
Internal Oscillator Input

Crystal
Resistor

Low Voltage Inhibit

Disable
Enable

FIGURE 23 — PROM MARKING



XXX = Customer ID

AD0244

M6805 Family System Configuration
And Programming Features

	THE GROWING M6805 FAMILY				FUTURE PRODUCTS	
	MC6805P2	MC146805E2	MC6805R2	MC6805U2	MC68705P3	MC146805G2
Technology	HMOS	CMOS	HMOS	HMOS	HMOS	CMOS
Number of Pins	28	40	40	40	28	40
On-Chip RAM (Bytes)	64	112	64	64	112	112
On-Chip User ROM (Bytes)	1.1 k	None	2 k	2 k	1.8 k EPROM	2.2 k
Expansion Bus	None	Yes	None	None	None	None
Bidirectional I/O Lines	20	16	32	32	20	32
I/O Options	None	None	A/D Converter	None	None	None
Software Compatibility	Similar to M6800					
True Bit Manipulation	Yes	Yes	Yes	Yes	Yes	Yes
Instructions	59	61	59	59	59	61
Ten Addressing Modes	Yes	Yes	Yes	Yes	Yes	Yes

Customer Name _____
 Address _____
 City _____ State _____ Zip _____
 Phone (_____) _____ Extension _____
 Contact Ms/Mr _____
 Customer Part Number _____

Pattern Media

2708 PROM

2716 PROM

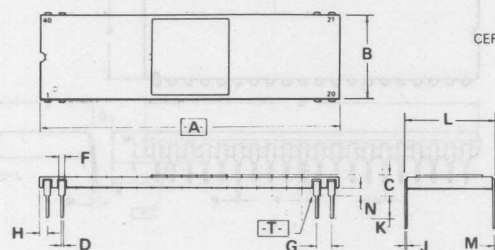
MDOS Disk File

(Note 2)

Notes: (2) Other media require prior factory approval.

Signature _____
 Title _____

PACKAGE DIMENSIONS



L SUFFIX
 CERAMIC PACKAGE
 CASE 715-05

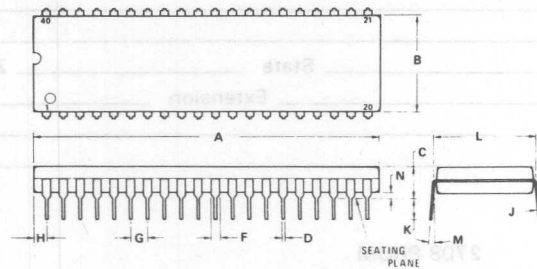
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	3.05	4.32	0.120	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	254 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	—	10°	—	10°
N	1.02	1.52	0.040	0.060

NOTES:

1. DIMENSION [A] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:

$$\oplus 0.25 (0.010) \text{ (M) } T A \text{ (M)}$$

3. [T] IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

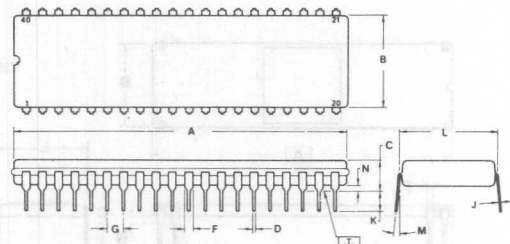


P SUFFIX
PLASTIC PACKAGE
CASE 711-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



S SUFFIX
CERDIP PACKAGE
CASE 734-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:

1. DIMENSION A-IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:

$$\pm 0.25 (0.010) \text{ (M)} \text{ T A (M)}$$

3. T IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSION A AND B INCLUDES MENISCUS.

Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others.

MC6805T2

Advance Information

8-BIT MICROCOMPUTER UNIT WITH PLL LOGIC

The MC6805T2 Microcomputer Unit (MCU) with PLL logic is a member of the M6805 Family of microcomputers. This 8-bit microcomputer contains a CPU, on-chip clock, ROM, RAM, I/O, timer and PLL logic. It is designed for the user who needs an economical microcomputer with the proven capabilities of the M6800-based instruction set, as well as the necessary logic required for frequency synthesis applications. The following are some of the hardware and software highlights of the MCU.

HARDWARE FEATURES:

- 8-Bit Architecture
- 64 Bytes of RAM
- Memory Mapped I/O
- 2500 Bytes of User ROM
- Internal 8-Bit Timer with 7-Bit prescaler
- Timer Start/Stop Select
- Timer Clock Source Select
- Vectored Interrupts—External and Timer
- 19 TTL/CMOS Compatible I/O Lines;
- 8 Lines LED Compatible
- On-Chip Clock Circuit
- Self-Check Mode
- Master Reset
- Complete Development System Support on EXORciser
- 5Vdc Single Supply
- 14-Bit Binary Variable Divider
- 10-Stage Mask-Programmable Reference Divider
- Three-State Phase and Frequency Comparator
- Suitable for TV Frequency Synthesizers

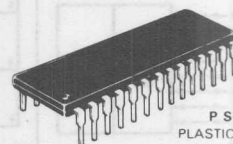
SOFTWARE FEATURES:

- Similar to M6800
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instructions
- Versatile Interrupt Handling
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Branches
- Memory Usable as Registers/Flags
- Single Instruction Memory Examine/Change
- 10 Powerful Addressing Modes
- All Addressing Modes Apply to ROM, RAM and I/O

HMOS

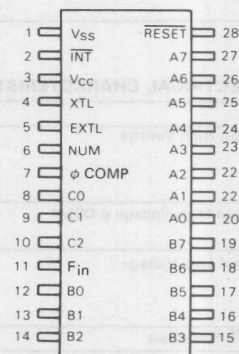
(HIGH DENSITY
N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

8-BIT MCU
WITH PLL LOGIC



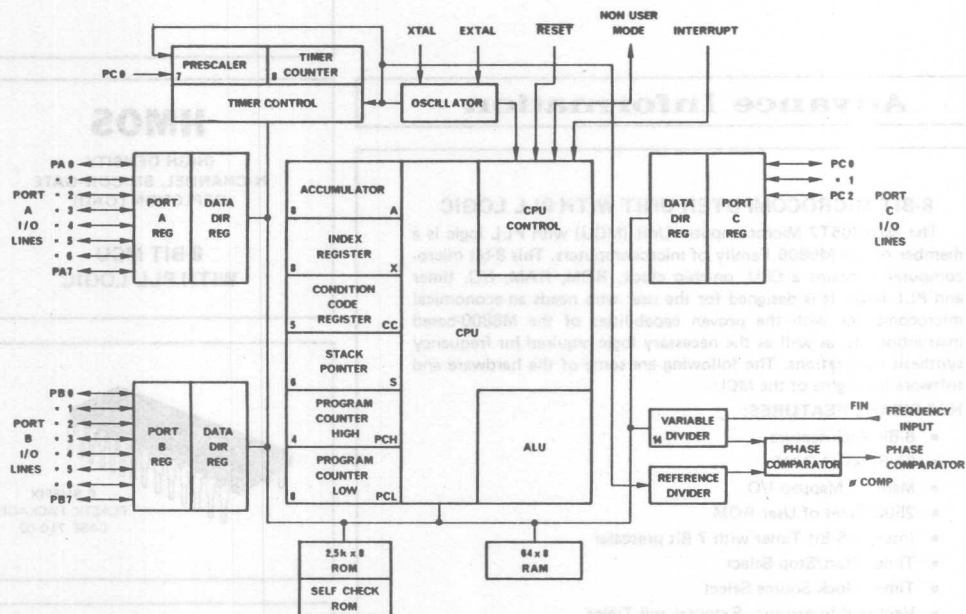
P SUFFIX
PLASTIC PACKAGE
CASE 710 02

FIGURE 1 — PIN ASSIGNMENTS



MC6805T2

FIGURE 2 — MC6805T2 HMOS MICROCOMPUTER BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	Vdc
Input Voltage	V _{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T _A	0 to 70	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Thermal Resistance Plastic Package	θ _{JA}	85	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} - (V_{in} or V_{out}) + V_{CC}.

ELECTRICAL CHARACTERISTICS (V_{CC} +5 Vdc ± 0.5 Vdc, V_{SS} GND, T_A = 0° - 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	RESET	V _{IH}	4.0	V _{CC}	Vdc
	INT	V _{IH}	2.2	—	Vdc
	All Other Except Fin	V _{IH}	V _{SS} + 2.0	V _{CC}	Vdc
Input High Voltage φ COMP	Normal Mode	V _{IH}	—	V _{CC}	Vdc
	Self-Check Mode	V _{IH}	9.0	15.0	Vdc
Input Low Voltage	RESET	V _{IL}	V _{SS} - 0.3	0.8	Vdc
	INT	V _{IL}	—	2.0	Vdc
	All Other Except Fin	V _{IL}	V _{SS} - 0.3	V _{SS} + 0.8	Vdc
INT Hysteresis	V _H	—	100	—	mVdc
Power Dissipation	P _D	—	350	—	mW

ELECTRICAL CHARACTERISTICS (Continued) ($V_{CC} = 5 \text{ Vdc} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0 - 70^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	10	—	pF
AC Coupled Input Voltage Swing	V_{FIP}	0.5	1.2	—	V _{ac} p-p
Input Current ($V_{IH} = V_{CC}$)	I_{FH}	—	—	40	μAdc
Output LO Current ($V_{OL} = 1.0 \text{ Vdc}$)	I_{CML}	—	300	—	μAdc
Output HI Current ($V_{OH} = V_{CC} - 1 \text{ Vdc}$)	I_{CMH}	—	200	—	μAdc
Leakage Current ($V_{IN} = V_{CC}$)	I_{OFF}	—	2	—	nAdc
Charging Current on Reset	$V_i = 0.8 \text{ V}$, $V_{CC} = 4.5 \text{ V}$	I_{IL}	4	—	μA
	$V_i = 0.8 \text{ V}$, $V_{CC} = 5.5 \text{ V}$	I_{IL}	—	50	μA
Reset Input Schmitt Trigger Switching Levels	V_{IH}	2.0	—	4.0	Vdc
	V_{IL}	—	—	0.8	Vdc
Sink Current on Interrupt Pin ($V_O = 4.5 \text{ V}$, $V_{CC} = 5.5 \text{ V}$)	I_{INT}	—	20	—	μA
Switching Points on Interrupt Pin	V_{IL}	—	—	1.5	V
	V_{IH}	4.0	—	—	V

SWITCHING CHARACTERISTICS ($V_{CC} = +5 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ - 70^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{cl}	0.4	—	4.0	MHz
Cycle Time	t_{CYC}	1.0	—	10	μs
INT Pulse Width	t_{IWL}	$t_{CYC} + 250$	—	—	ns
RESET Pulse Width	t_{RWL}	$t_{CYC} + 250$	—	—	ns
Delay Time Reset (External Cap = $0.47 \mu\text{F}$)	t_{RHL}	20	50	—	ms
Input Frequency	F_{in}	1	—	16	MHz
Input Frequency Rise Time at F_{in} max.	t_{INR}	—	—	20	ns
Input Frequency Fall Time at F_{in} max.	t_{INF}	—	—	20	ns
Duty Cycle	DF_{IN}	40	—	60	%
Injection Pulse Active Time	t_{err}	—	70	—	ns

PORT ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.00 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ$ to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A					
Output Low Voltage $I_{load} = 1.6 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output High Voltage $I_{load} = -100 \mu\text{Adc}$	V_{OH}	2.4	—	—	Vdc
Output High Voltage $I_{load} = -10 \mu\text{Adc}$	V_{OH}	3.5	—	—	Vdc
Input High Voltage $I_{load} = -300 \mu\text{Adc}$ (max)	V_{IH}	$V_{SS} + 2.0$	—	V_{CC}	Vdc
Input Low Voltage $I_{load} = -500 \mu\text{Adc}$ (max)	V_{IL}	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	Vdc
Port B					
Output Low Voltage $I_{load} = 3.2 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output Low Voltage $I_{load} = 10 \text{ mAdc}$ (sink)	V_{OL}	—	—	1.0	Vdc
Output High Voltage $I_{load} = -200 \mu\text{Adc}$	V_{OH}	2.4	—	—	Vdc
Darlington Current Drive (Source) $V_O = 1.5 \text{ Vdc}$	I_{OH}	-1.0	—	-10	mAdc
Input High Voltage	V_{IH}	$V_{SS} + 2.0$	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$V_{SS} + 0.8$	Vdc

PORT ELECTRICAL CHARACTERISTICS (continued)

Port C					
Output Low Voltage $I_{load} = 1.6 \text{ mA}$	VOL	—	—	0.4	Vdc
Output High Voltage $I_{load} = -100 \mu\text{A}$	VOH	2.4	—	—	Vdc
Input High Voltage	VIH	VSS + 2.0	—	VCC	Vdc
Input Low Voltage	VIL	VSS - 0.3	—	VSS + 0.8	Vdc
Off-State Input Current					
Three-State Ports B & C	ITSI	—	2	20	μA
Input Current					
Extl at $V_{in} = 0.1 \text{ V}$	Iin	—	40	—	μA

FIGURE 3 — TTL EQUIV. TEST LOAD (PORT B)

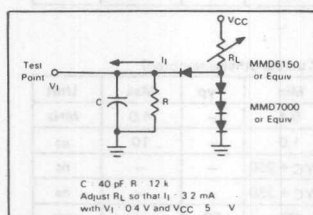


FIGURE 4 — CMOS EQUIV. TEST LOAD (PORT A)

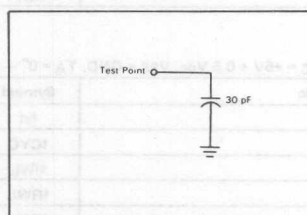
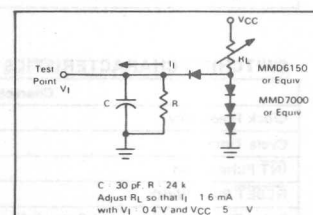


FIGURE 5 — TTL EQUIV. TEST LOAD (PORTS A AND C)



SIGNAL DESCRIPTION

The input and output signals for the MCU shown in Figure 1 are described in the following paragraphs.

VCC AND VSS — Power is supplied to the MCU using these two pins. VCC is +5.00 Vdc $\pm 0.5 \text{ V}$. VSS is the ground connection.

INT — This pin provides the capability for applying an external interrupt to the MCU. Refer to **INTERRUPTS** for additional information.

XTAL AND EXTAL — These pins provide control input for the on-chip clock circuit. A crystal (AT cut, 4 MHz maximum) can be connected to these pins to provide the internal oscillator. Refer to **INTERNAL OSCILLATOR** for recommendations about these pins.

ϕCOMP — This tristate output is the result of comparing the internal reference frequency to the variable divider signal. Refer to **PLL** for details. In Self Test it is raised to $>9 \text{ Vdc}$.

RESET — This pin allows resetting of the MCU at times other than the automatic resetting capability already in the MCU. Refer to **RESETS** for additional information.

NUM — This pin is not for user application and should be connected to VSS.

INPUT/OUTPUT LINES (A0-A7, B0-B7, C0-C2) — These 19 lines are arranged into two 8-bit ports (A and B) and one 3-bit port (C). All lines are programmable as either inputs or outputs under software control of the data direction registers. Refer to **INPUTS/OUTPUTS** for additional information.

MEMORY

The MCU memory is configured as shown in Figure 6. During the processing of an interrupt, the contents of the MCU registers are pushed onto the stack in the order shown in Figure 7. Since the stack pointer decrements during pushes, the low order byte (PCL) of the program counter is stacked first, then the high order three bits (PCH) are stacked. This ensures that the program counter is loaded correctly as the stack pointer increments when it pulls data from the stack. A subroutine call will cause only the program counter (PCH, PCL) contents to be pushed onto the stack.

Fin — This is a self biased clock input from the high speed variable divider, requiring min. 0.5 Vpp , AC coupled input signal, frequency range is 1 to 16 MHz.

REGISTERS

The MCU has five registers available to the programmer. They are shown in Figure 8 and are explained in the following paragraphs.

ACCUMULATOR (A) — The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

INDEX REGISTER (X) — The index register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit address that may be added to an offset value to create an effective address. The index register can also be used for limited calculations and data manipulations when using read/modify/write instructions. When not required by a code sequence being executed, the index register can be used as a temporary storage area.

PROGRAM COUNTER (PC) — The program counter is a 12-bit register that contains the address of the next instruction to be executed.

STACK POINTER (SP) — The stack pointer is a 12-bit register that contains the address of the next free location on the stack. Initially, the stack pointer is set to location \$07F and is decremented as data is being pushed onto the stack and incremented as data is being pulled from the stack. The seven most significant bits of the stack pointer are permanently set to 0000011. During a MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location \$07F. Subroutines and interrupts may be nested down to location \$061 which allows the programmer to use up to 15 levels of subroutine calls.

CONDITION CODE REGISTER (CC) — The condition code register is a 5-bit register in which each bit is used to indicate or flag the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each individual condition code register bit is explained in the following paragraphs.

Half Carry (H) — Used during arithmetic operations (ADD and ADC) to indicate that a carry occurred between bits 3 and 4.

Interrupt (I) — This bit is set to mask the timer and external interrupt (INT). If an interrupt occurs while this bit is set it is latched and will be processed as soon as the interrupt bit is reset.

Negative (N) — Used to indicate that the result of the last arithmetic, logical or data manipulation was negative (bit 7 in result equal to a logical one).

Zero (Z) — Used to indicate that the result of the last arithmetic, logical or data manipulation was zero.

Carry/Borrow (C) — Used to indicate that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

TIMER

The MCU timer circuitry is shown in Figure 9. The 8-bit counter is loaded under program control and counts down toward zero as soon as the clock input is applied. When the timer reaches zero the timer interrupt request bit (bit 7) in the timer control register is set. The MCU responds to this interrupt by saving the present MCU state in the stack, fetching the timer interrupt vector from locations \$FF8 and \$FF9 and executing the interrupt routine. The timer interrupt can be masked by setting the timer interrupt mask bit (bit 6) in the timer control register. The interrupt bit (I bit) in the condition code register will also prevent a timer interrupt from being processed.

The timer's clock input can be monitored via bit 5, (TCR5), in the timer control register. When this bit is set high, logical one, (external mode), the timer clock source is dependant on port C0 status. In this mode a mask option is used to select either a) the gated $\phi 2$ with port C0 status, or b) the positive transition on port C0 as the timer clock source. This allows easily performed pulse width or pulse count measurements.

When TCR5 is low, logical zero, the timer clock source is internal $\phi 2$. At power up reset this bit is reset to logical zero.

Bit 4 in the timer control register (TCR4) disables the timer clock source when set to logical one. This bit is cleared to logical zero at power up reset.

RESETS

The MCU can be reset two ways: by the external reset input (RESET) and during the power up time. See Figure 11.

Upon power up, a minimum of 20 milliseconds is needed before allowing the reset input to go high. This time allows the internal oscillator to stabilize. Connecting a capacitor to the RESET input as shown in Figure 12 will provide sufficient delay.

INTERNAL OSCILLATOR

The internal oscillator circuit has been designed to require a minimum of external components. The use of a crystal (AT cut, 4 MHz max) is sufficient to drive the internal oscillator. The different connection methods are shown in Figures 13 and 14 while the crystal specifications are given in Figure 15.

FIGURE 6 — MCU MEMORY CONFIGURATION

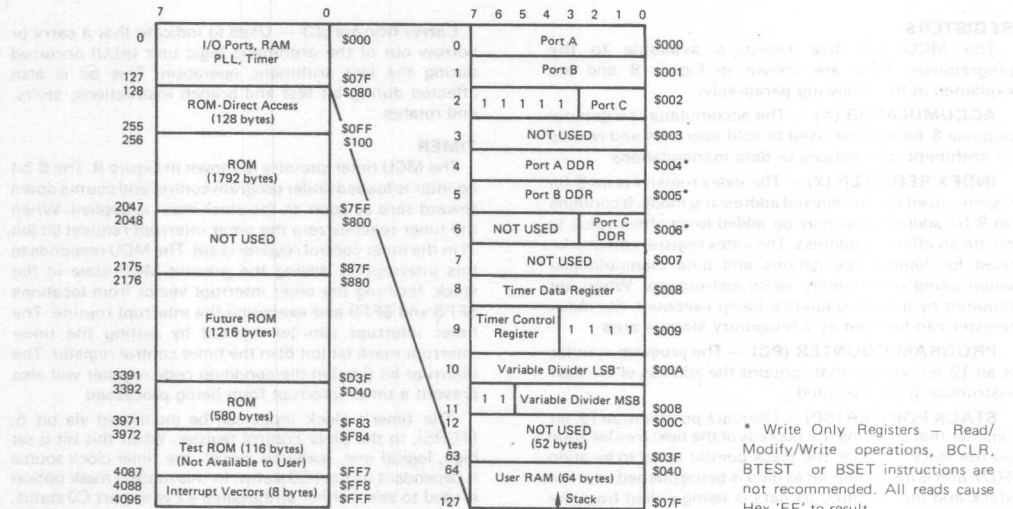
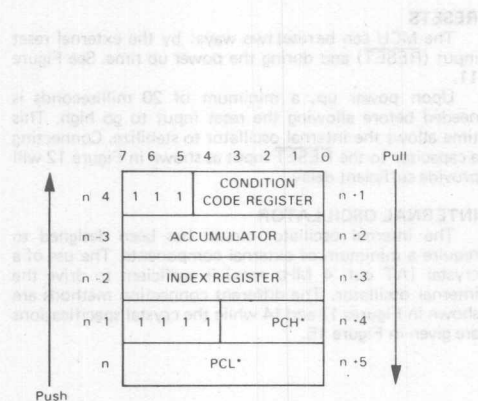


FIGURE 7 — INTERRUPT STACKING ORDER



* For subroutine calls, only PCH and PCL are stacked

FIGURE 8 — PROGRAMMING MODEL

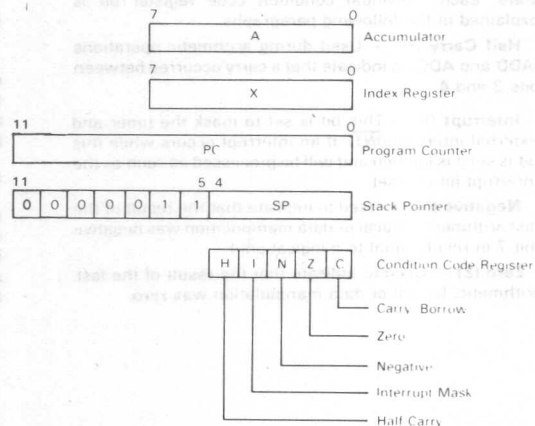


FIGURE 9 — TIMER BLOCK DIAGRAM

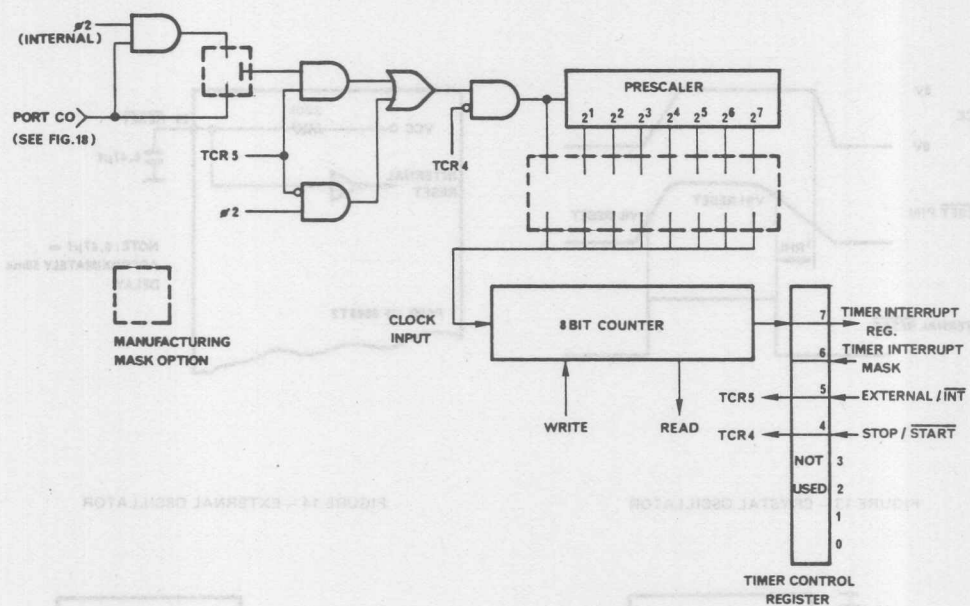


FIGURE 10 — SELF CHECK CONNECTIONS

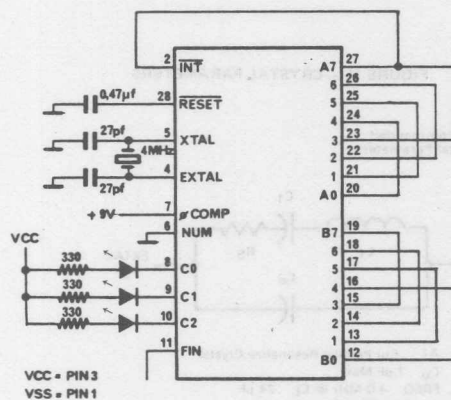


FIGURE 11 – POWER UP AND RESET TIMING

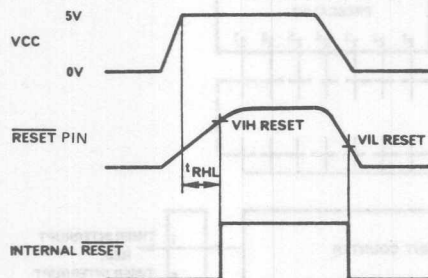


FIGURE 12 – POWER UP RESET DELAY CIRCUIT

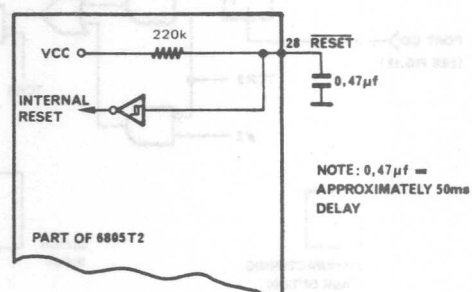


FIGURE 13 – CRYSTAL OSCILLATOR

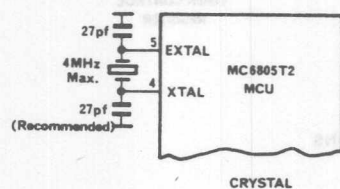


FIGURE 14 – EXTERNAL OSCILLATOR

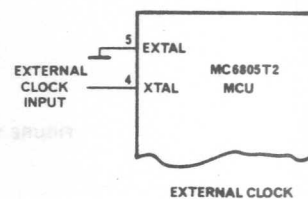
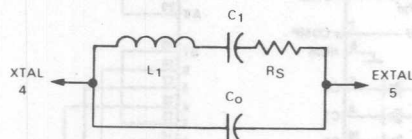


FIGURE 15 – CRYSTAL PARAMETERS

Recommended
Crystal Parameters



AT - Cut Parallel Resonance Crystal
 C_0 - 7 pF Max
 FREQ - 4.0 MHz @ C_L 24 pF
 R_S = 100Ω Max

INTERRUPTS

The MCU can be interrupted three different ways through the external interrupt ($\overline{\text{INT}}$) input pin, the internal timer interrupt request, and a software interrupt instruction (SWI). When any interrupt occurs, processing is suspended, the present MCU state is pushed onto the stack, the interrupt bit (I) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. The interrupt service routines normally end with a return from interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt. Table 1 provides a listing of the interrupts, their priority, and the vector address that contain the starting address of the appropriate interrupt routine.

A sinusoidal signal (1 kHz maximum) can be used to generate an external interrupt ($\overline{\text{INT}}$) as shown in Figure 16.

A flowchart of the interrupt processing sequence is given in Figure 17.

TABLE 1 - INTERRUPT PRIORITIES

Interrupt	Priority	Vector Address
RESET	1	\$FFE and \$FFF
SWI	2	\$FFC and \$FFD
INT	3	\$FFA and \$FFB
Timer	4	\$FF8 and \$FF9

INPUT/OUTPUT

There are 19 input/output pins. All pins are programmable as either inputs or outputs under software control of the data direction registers. When programmed as outputs, all I/O pins read latched output data regardless of the logic level at the output pin due to output loading (see Figure 18). When port B is programmed for outputs, it is capable of sinking 10 milliamperes on each pin (one volt maximum). All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs while port B and C lines are CMOS compatible as inputs. Figure 19 provides some examples of port connections.

FIGURE 16 - TYPICAL SINUSODIAL INTERRUPT CIRCUITS

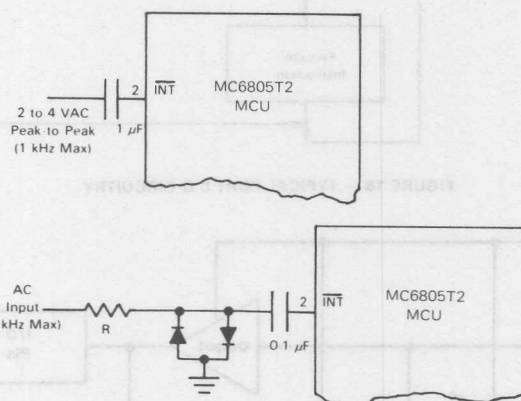
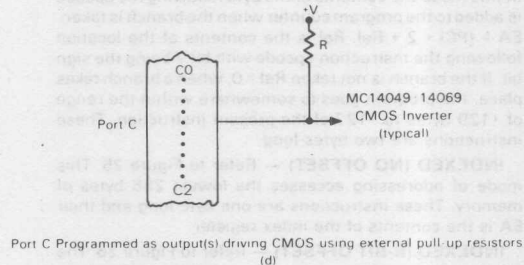
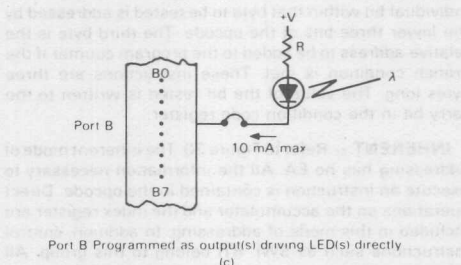
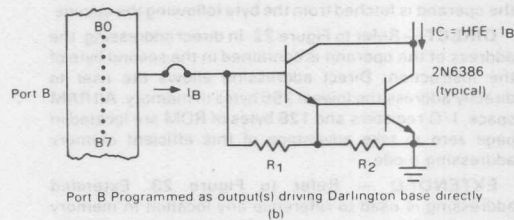
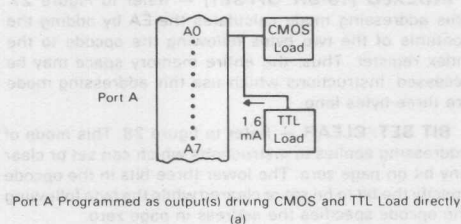


FIGURE 19 — TYPICAL PORT CONNECTIONS



BIT MANIPULATION

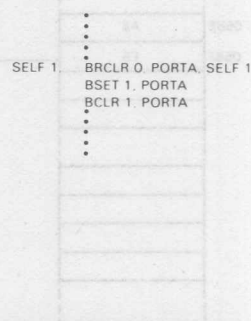
The MCU has the ability to set or clear any single random access memory or input/output bit (except the data direction registers) with a single instruction (BSET, BCLR). Any bit in the page zero read only memory can be tested, using the BRSET and BRCLR instructions, and the program branches as a result of its state. This capability to work with any bit in RAM, ROM or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines. The example in Figure 20 illustrates the usefulness of the bit manipulation and test instructions. Assume that bit 0 of port A is connected to a zero crossing detector circuit and that bit 1 of port A is connected to the trigger of a TRIAC which powers the controlled hardware.

This program, which uses only seven ROM locations, provides turn-on of the TRIAC within 14 microseconds of the zero crossing. The timer could also be incorporated to

provide turn-on at some later time which would permit pulse-width modulation of the controlled power.

ADDRESSING MODES The MCU has ten addressing modes available for use by the programmer. They are explained and illustrated briefly in the following paragraphs.

FIGURE 20 — BIT MANIPULATION EXAMPLE



IMMEDIATE — Refer to Figure 21. The immediate addressing mode accesses constants which do not change during program execution. Such instructions are two bytes long. The effective address (EA) is the PC and the operand is fetched from the byte following the opcode.

DIRECT — Refer to Figure 22. In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in memory. All RAM space, I/O registers and 128 bytes of ROM are located in page zero to take advantage of this efficient memory addressing mode.

EXTENDED — Refer to Figure 23. Extended addressing is used to reference any location in memory space. The EA is the contents of the two bytes following the opcode. Extended addressing instructions are three bytes long.

RELATIVE — Refer to Figure 24. The relative addressing mode applies only to the branch instructions. In this mode the contents of the byte following the opcode is added to the program counter when the branch is taken. $EA = (PC) + 2 + Rel$. Rel is the contents of the location following the instruction opcode with bit 7 being the sign bit. If the branch is not taken $Rel = 0$, when a branch takes place, the program goes to somewhere within the range of +129 bytes to -127 of the present instruction. These instructions are two bytes long.

INDEXED (NO OFFSET) — Refer to Figure 25. This mode of addressing accesses the lowest 256 bytes of memory. These instructions are one byte long and their EA is the contents of the index register.

INDEXED (8-BIT OFFSET) — Refer to Figure 26. The EA is calculated by adding the contents of the byte

following the opcode to the contents of the index register. In this mode, 511 low memory locations are accessible. These instructions occupy two bytes.

INDEXED (16-BIT OFFSET) — Refer to Figure 27. This addressing mode calculates the EA by adding the contents of the two bytes following the opcode to the index register. Thus, the entire memory space may be accessed. Instructions which use this addressing mode are three bytes long.

BIT SET/CLEAR — Refer to figure 28. This mode of addressing applies to instructions which can set or clear any bit on page zero. The lower three bits in the opcode specify the bit to be set or cleared while the byte following the opcode specifies the address in page zero.

BIT TEST AND BRANCH — Refer to Figure 29. This mode of addressing applies to instructions which can test any bit in the first 256 locations (\$00-\$FF) and branch to any location relative to the PC. The byte to be tested is addressed by the byte following the opcode. The individual bit within that byte to be tested is addressed by the lower three bits of the opcode. The third byte is the relative address to be added to the program counter if the branch condition is met. These instructions are three bytes long. The value of the bit tested is written to the carry bit in the condition code register.

INHERENT — Refer to Figure 30. The inherent mode of addressing has no EA. All the information necessary to execute an instruction is contained in the opcode. Direct operations on the accumulator and the index register are included in this mode of addressing. In addition, control instructions such as SWI RTI belong to this group. All inherent addressing instructions are one byte long.

FIGURE 21 — IMMEDIATE ADDRESSING EXAMPLE

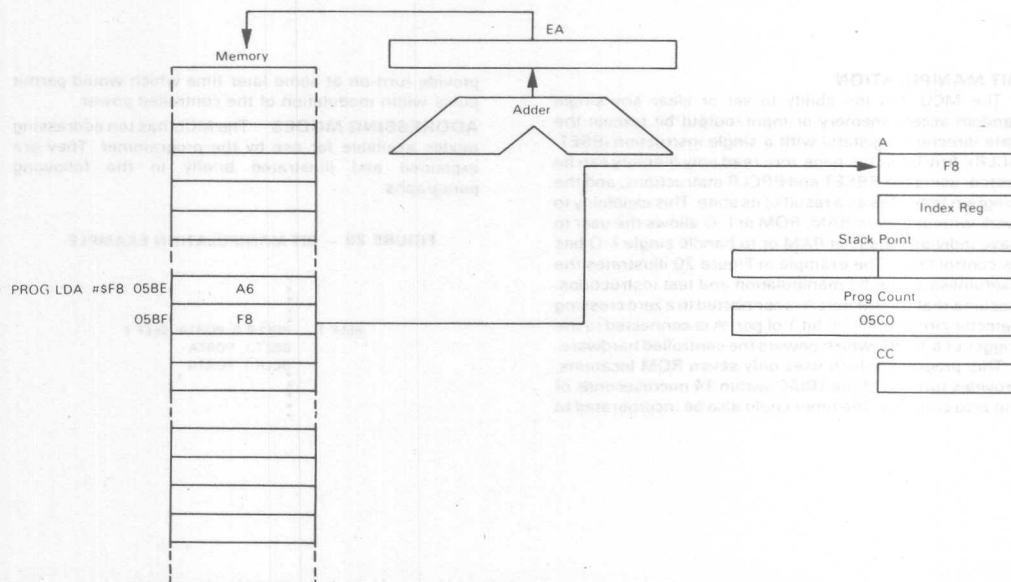


FIGURE 22 — DIRECT ADDRESSING EXAMPLE

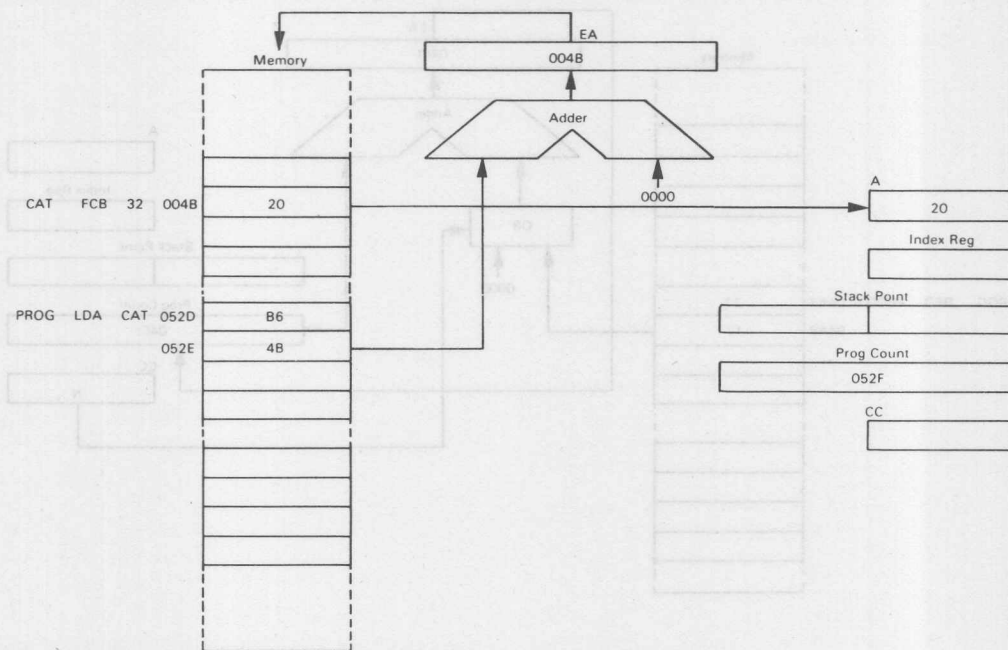


FIGURE 23 — EXTENDED ADDRESSING EXAMPLE

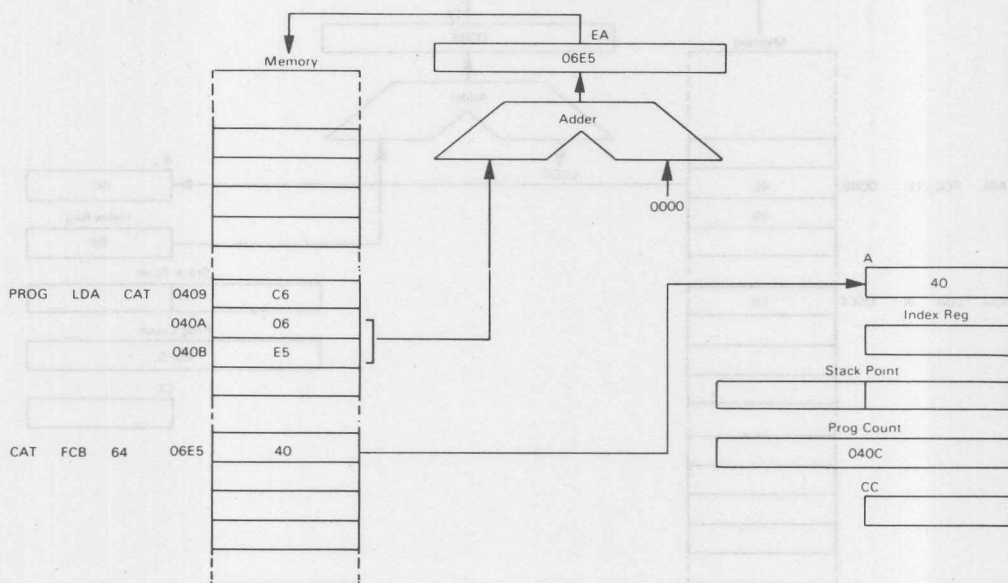


FIGURE 24 — RELATIVE ADDRESSING EXAMPLE

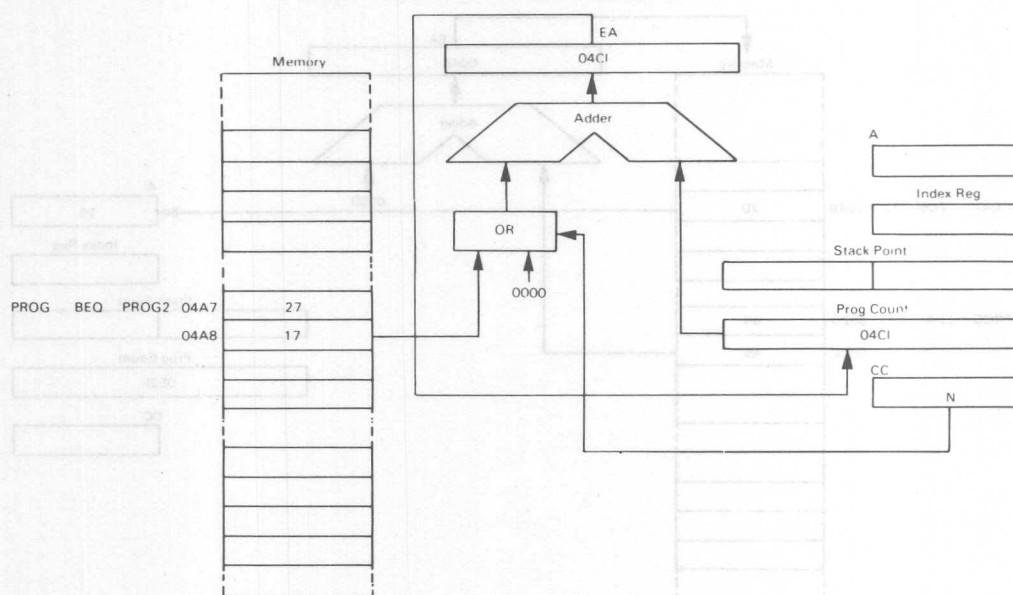


FIGURE 25 — INDEXED (NO OFFSET) ADDRESSING EXAMPLE

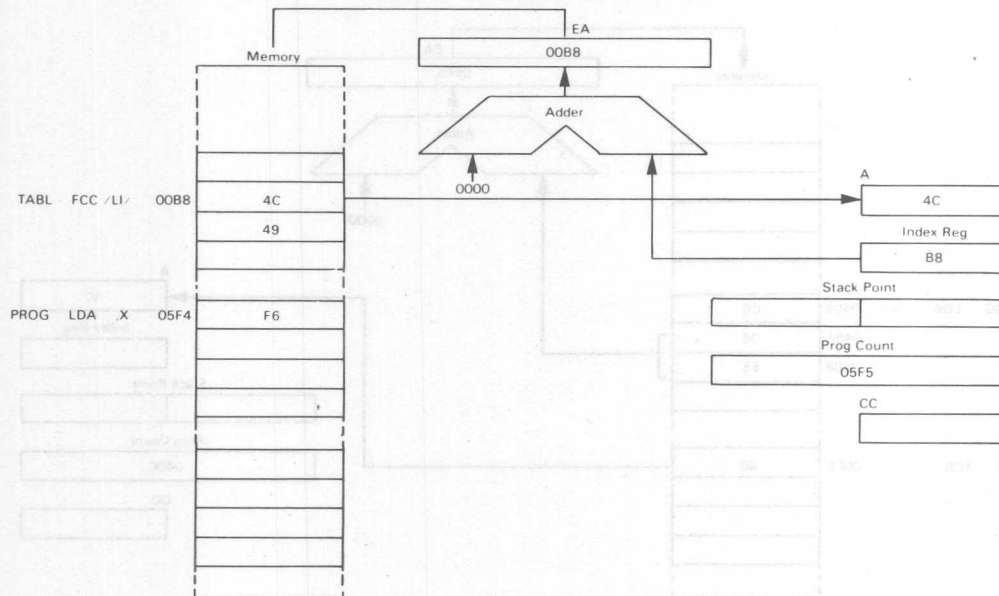


FIGURE 26 — INDEXED (8-BIT OFFSET) ADDRESSING EXAMPLE

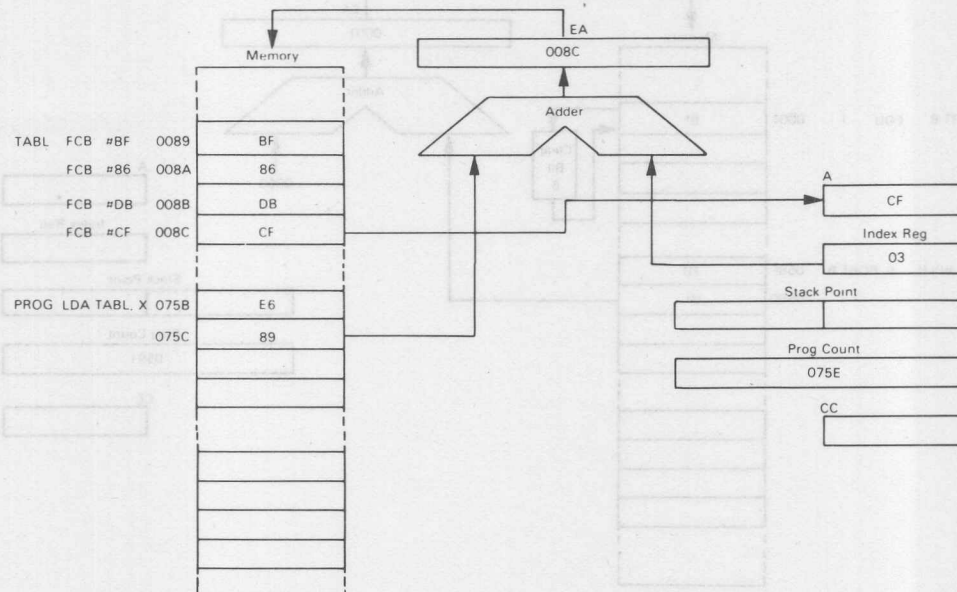


FIGURE 27 INDEXED (16-BIT OFFSET) ADDRESSING EXAMPLE

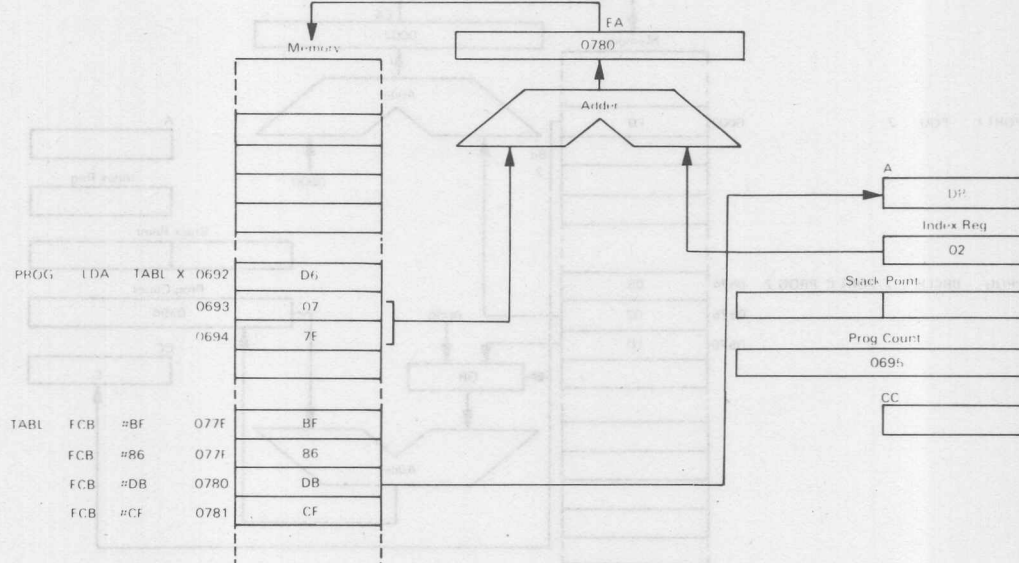


FIGURE 28 — BIT SET/CLEAR ADDRESSING EXAMPLE

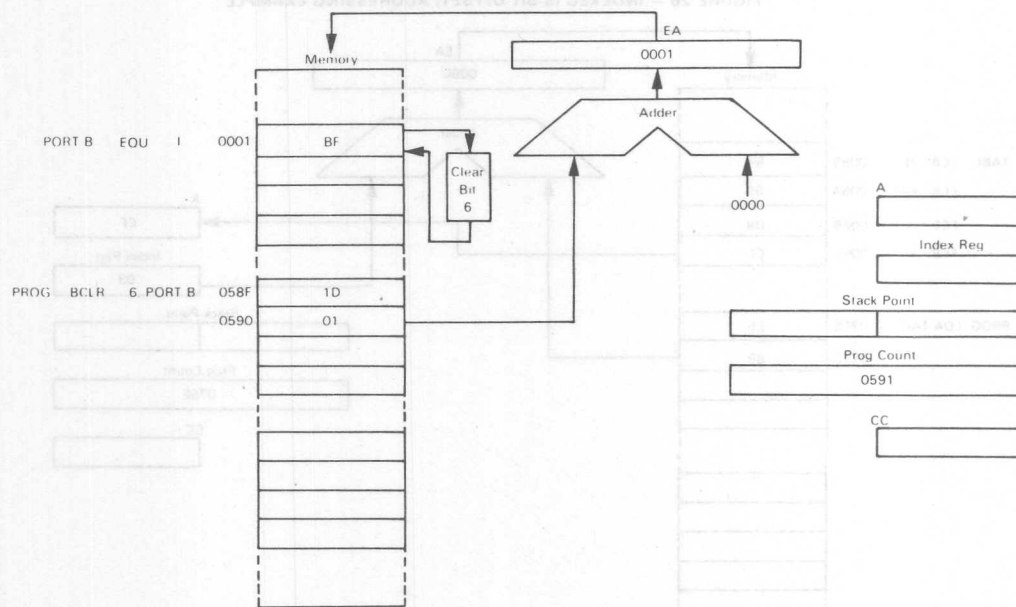


FIGURE 29 — BIT TEST AND BRANCH ADDRESSING EXAMPLE

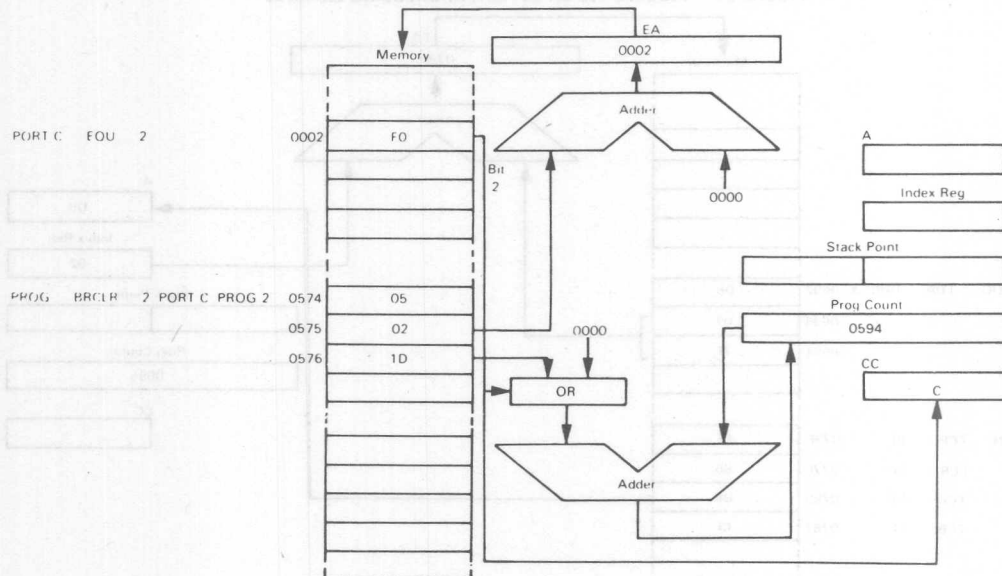
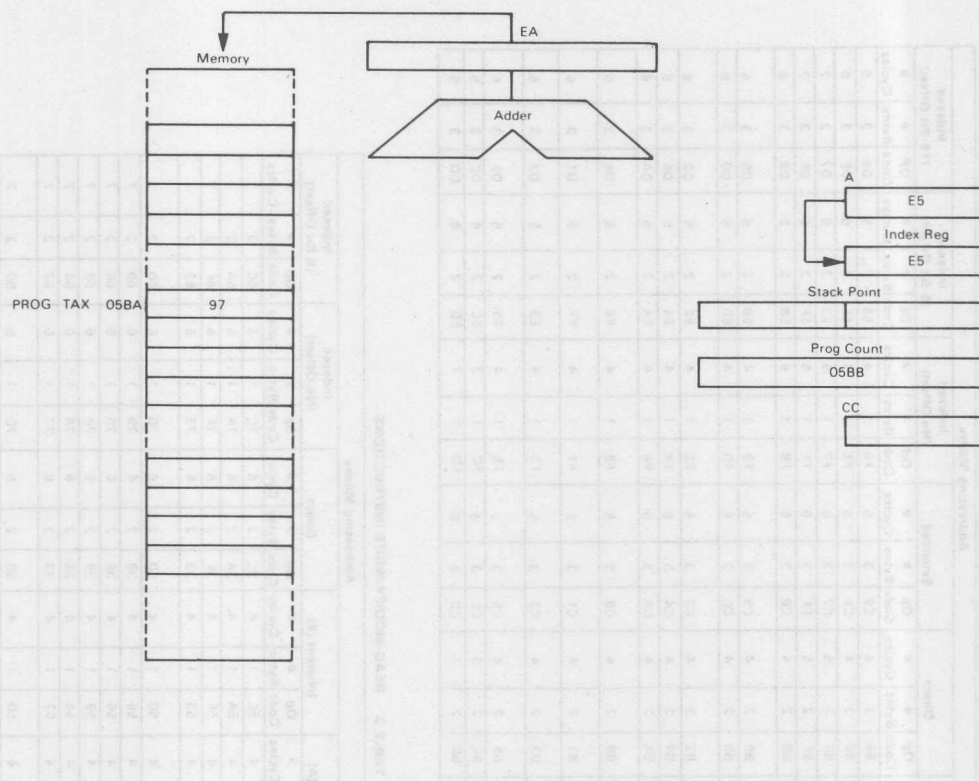


FIGURE 30 — INHERENT ADDRESSING EXAMPLE

**INSTRUCTION SET**

The MCU has a set of 59 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS — Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 2.

READ/MODIFY/WRITE INSTRUCTIONS — These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/

write instructions since it does not perform the write. Refer to Table 3.

BRANCH INSTRUCTIONS — The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 4.

BIT MANIPULATION INSTRUCTIONS — These instructions are used on any bit in the first 256 bytes of the memory. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 5.

CONTROL INSTRUCTIONS — The control instructions control the MCU operations during program execution. Refer to Table 6.

ALPHABETICAL LISTING — The complete instruction set is given in alphabetical order in Table 7.

OPCODE MAP — Table 8 is an opcode map for the instructions used on the MCU.

TABLE 2 — REGISTER/MEMORY INSTRUCTIONS

Function	Mnemonic	Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
Load X from Memory	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
Store A in Memory	STA	—	—	—	B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
Store X in Memory	STX	—	—	—	BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
Add Memory to A	ADD	AB	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
Add Memory and Carry to A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
Subtract Memory	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
AND Memory to A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
OR Memory with A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
Jump Unconditional	JMP	—	—	—	BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
Jump to Subroutine	JSR	—	—	—	BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9

TABLE 3 — READ-MODIFY-WRITE INSTRUCTIONS

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8 Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
Decrement	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
Clear	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
Complement	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
Negate (2's Complement)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
Rotate Left Thru Carry	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
Rotate Right Thru Carry	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
Logical Shift Left	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
Logical Shift Right	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
Arithmetic Shift Right	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
Test for Negative or Zero	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

TABLE 4 — BRANCH INSTRUCTIONS

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	4
Branch Never	BRN	21	2	4
Branch IFF Higher	BHI	22	2	4
Branch IFF Lower or Same	BLS	23	2	4
Branch IFF Carry Clear	BCC	24	2	4
(Branch IFF Higher or Same)	(BHS)	24	2	4
Branch IFF Carry Set	BCS	25	2	4
(Branch IFF Lower)	(BLO)	25	2	4
Branch IFF Not Equal	BNE	26	2	4
Branch IFF Equal	BEQ	27	2	4
Branch IFF Half Carry Clear	BHCC	28	2	4
Branch IFF Half Carry Set	BHCS	29	2	4
Branch IFF Plus	BPL	2A	2	4
Branch IFF Minus	BMI	2B	2	4
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	4
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	4
Branch IFF Interrupt Line is Low	BIL	2E	2	4
Branch IFF Interrupt Line is High	BIH	2F	2	4
Branch to Subroutine	BSR	AD	2	8

TABLE 5 — BIT MANIPULATION INSTRUCTIONS

Function	Mnemonic	Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is set	BRSET n (n = 0...7)	—	—	—	2 · n	3	10
Branch IFF Bit n is clear	BRCLR n (n = 0...7)	—	—	—	01 + 2 · n	3	10
Set Bit n	BSET n (n = 0...7)	10 + 2 · n	2	7	—	—	—
Clear bit n	BCLR n (n = 0...7)	11 + 2 · n	2	7	—	—	—

TABLE 6 — CONTROL INSTRUCTIONS

Function	Mnemonic	Inherent		
		Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	11
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No Operation	NOP	9D	1	2

TABLE 7 — INSTRUCTION SET

Mnemonic	Addressing Modes									Bit Set/ Clear	Bit Test & Branch	Condition Code				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)				H	I	N	Z	C
ADC		X	X	X		X	X	X				△	●	△	△	△
ADD		X	X	X		X	X	X				△	●	△	△	△
AND		X	X	X		X	X	X				●	●	△	△	●
ASL	X		X			X	X					●	●	△	△	△
ASR	X		X			X	X					●	●	△	△	△
BCC					X							●	●	●	●	●
BCLR										X		●	●	●	●	●
BCS					X							●	●	●	●	●
BEQ					X							●	●	●	●	●
BHCC					X							●	●	●	●	●
BHCS					X							●	●	●	●	●
BHI					X							●	●	●	●	●
BHS					X							●	●	●	●	●
BIH					X							●	●	●	●	●
BIL					X							●	●	●	●	●
BIT		X	X	X		X	X	X				●	●	△	△	●
BLO					X							●	●	●	●	●
BLS					X							●	●	●	●	●
BMC					X							●	●	●	●	●
BMI												●	●	●	●	●
BMS												●	●	●	●	●
BNE												●	●	●	●	●
BPL												●	●	●	●	●
BRA												●	●	●	●	●
BRN												●	●	●	●	●
BRCLR											X	●	●	●	△	
BRSET											X	●	●	●	△	
BSET										X		●	●	●	●	●
BSR					X							●	●	●	●	●
CLC	X											●	●	●	●	0
CLI	X											●	0	●	●	●
CLR	X		X			X	X					●	●	0	1	●
CMP		X	X	X		X	X	X				●	●	△	△	△
COM	X		X			X	X					●	●	△	△	1
CPX		X	X	X		X	X	X				●	●	△	△	△
DEC	X		X			X	X					●	●	△	△	●
EOR		X	X	X		X	X	X				●	●	△	△	●
INC	X		X			X	X					●	●	△	△	△
JMP			X	X		X	X	X				●	●	●	●	●
JSR			X	X		X	X	X				●	●	●	●	●
LDA		X	X	X		X	X	X				●	●	△	△	●
LDX		X	X	X		X	X	X				●	●	△	△	●
LSL	X		X			X	X					●	●	△	△	△
LSR	X		X			X	X					●	●	0	△	△
NEQ	X		X			X	X					●	●	△	△	△
NOP	X											●	●	●	●	●
ORA		X	X	X		X	X	X				●	●	△	△	●
ROL	X		X			X	X					●	●	△	△	△
RSP	X											●	●	●	●	●

Condition Code Symbols

H Half Carry (From Bit 3)
 I Interrupt Mask
 N Negative (Sign Bit)
 Z Zero

C Carry Borrow
 △ Test and Set if True, Cleared Otherwise
 ● Not Affected

TABLE 7 INSTRUCTION SET
(CONT.)

Mnemonic	Addressing Modes										Condition Code				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	△	△	△
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	△	△	●
STX			X	X		X	X	X			●	●	△	△	●
SUB		X	X	X		X	X	X			●	●	△	△	△
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	△	△	●
TXA	X										●	●	●	●	●

Condition Code Symbols

H Half Carry (From Bit 3)

I Interrupt Mask

N Negative (Sign Bit)

Z Zero

C Carry Borrow

△ Test and Set if True, Cleared Otherwise

● Not Affected

? Load CC Register From Stack

TABLE 8 — OPCODE MAP

Bit Manipulation		Brnch	Read/Modify/Write					Control		Register/Memory						
Test & Branch	Set/ Clear		Rel	DIR	A	X	.X1	.X0	INH	INH	IMM	DIR	EXT	.X2	.X1	.X0
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
	BRSET0	BSET0	BRA					NEO	RTI*	—				SUB		0
1	BRCLR0	BCLR0	BRN					—	RTS*	—				CMP		1
2	BRSET1	BSET1	BHI					—	—	—				SBC		2
3	BRCLR1	BCLR1	BLS					COM	SWI*	—				CMPX/CPX		3
4	BRSET2	BSET2	BCC					LSR	—	—				AND		4
5	BRCLR2	BCLR2	BCS					—	—	—				BIT		5
6	BRSET3	BSET3	BNE					ROR	—	—				LDA		6
7	BRCLR3	BCLR3	BEQ					ASR	—	TAX	—			STA (+1)		7
8	BRSET4	BSET4	BHCC					LSL/ASL	—	CLC				EOR		8
9	BRCLR4	BCLR4	BHCS					ROL	—	SEC				ADC		9
A	BRSET5	BSET5	BPL					DEC	—	CLI				ORA		A
B	BRCLR5	BCLR5	BMI					—	—	SEI				ADD		B
C	BRSET6	BSET6	BMC					INC	—	RSP	—			JMP (-1)		C
D	BRCLR6	BCLR6	BMS					TST	—	NOP	BSR*			JSR (+3)		D
E	BRSET7	BSET7	BIL					—	—	—				LDX		E
F	BRCLR7	BCLR7	BIH					CLR	—	TXA	—			STX (+1)		F
	3/10	2/7	2/4	2/6	1/4	1/4	2/7	1/6	1/*	1/2	2/2	2/4	3/5	3/6	2/5	1/4

Notes

Undefined opcodes are marked with "—".

The numbers at the bottom of each column denote the number of bytes and the number of cycles required (Bytes: Cycles)

Mnemonics followed by a "*" require a different number of cycles as follows:

RTI 9

RTS 6

SWI 11

BSR 8

() indicate that the number in parenthesis must be added to the cycle count for that instruction

FIGURE 32 — PRINCIPAL PLL EQUATIONS

For a system in lock:

$$FVAR = FREF$$

$$\text{since } FIN = FVAR \cdot N$$

$$FVCO = FIN \cdot P$$

where P = prescaler division ratio

$$\Rightarrow FVCO = FREF \cdot P \cdot N$$

Minimum frequency step =

$$\frac{\Delta FVCO}{\Delta N} = FREF \cdot P$$

$$\text{e.g.: } FCL = 4.00 \text{ MHz}$$

$$R = 2^{10}$$

where R = the reference divider ratio

$$P = 64$$

$$\rightarrow \frac{\Delta FVCO}{\Delta N} = 62.5 \text{ kHz}$$

$$FREF = 976.5 \text{ Hz}$$

FIGURE 33 — MC6805T2 PLL HARDWARE BLOCK DIAGRAM

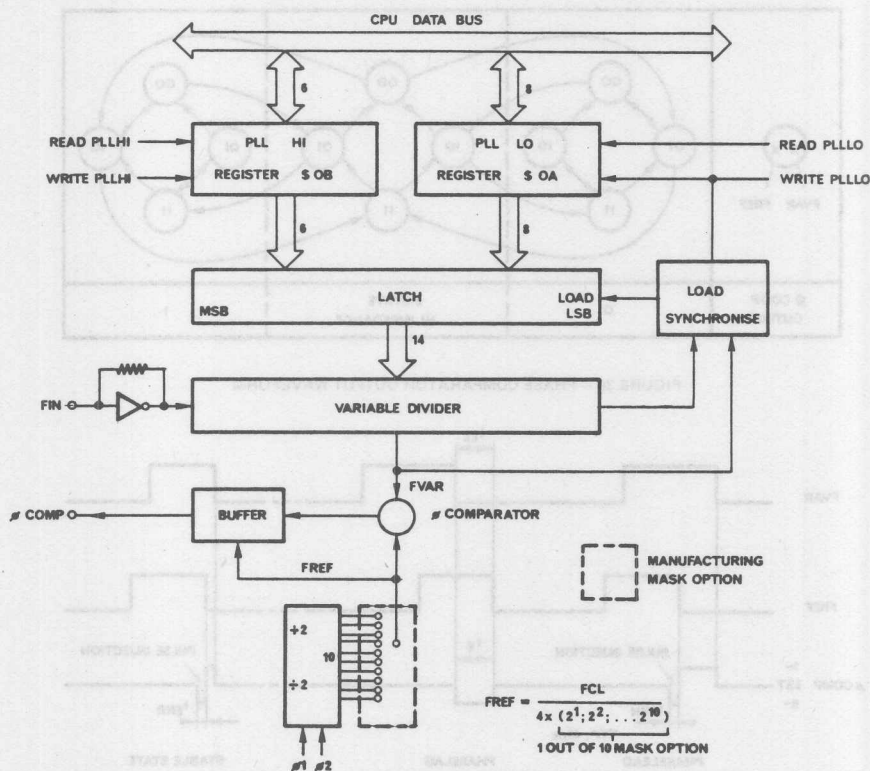


FIGURE 34 – TYPICAL FINE TUNE EXAMPLE

FTUP	LDA	PLLLOW	
	INCA		check if LS byte = FF (Reg \$0A)
	BNE	TT1	if not increment only LS byte
	INC	PLLLOW	increment MSB (Reg \$0B) before LSB
TT1	INC	PLLLOW	
	•		
	•		
	•		
FTDWN	TST	PLLLOW	check if LS byte = 00
	BNE	TT2	if not decrement only LS byte
	DEC	PLLHI	decrement MSB before LSB
TT2	DEC	PLLLOW	
	•		
	•		
	•		

FIGURE 35 – PHASE COMPARATOR STATE DIAGRAM

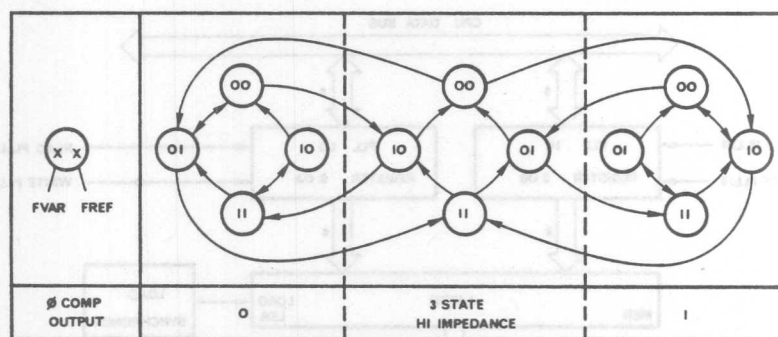


FIGURE 36 – PHASE COMPARATOR OUTPUT WAVEFORM

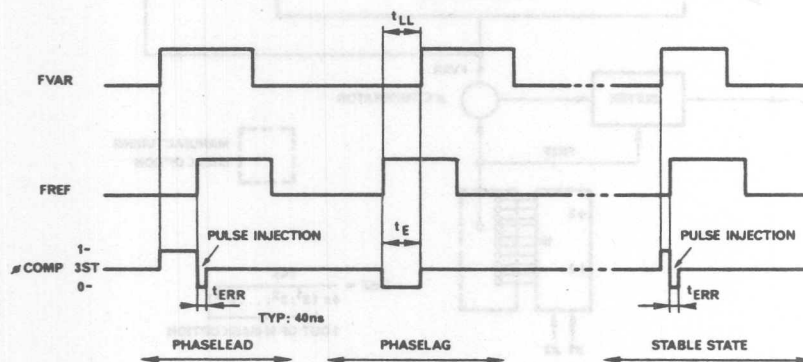


FIGURE 37 — PHASE COMPARATOR CHARACTERISTICS

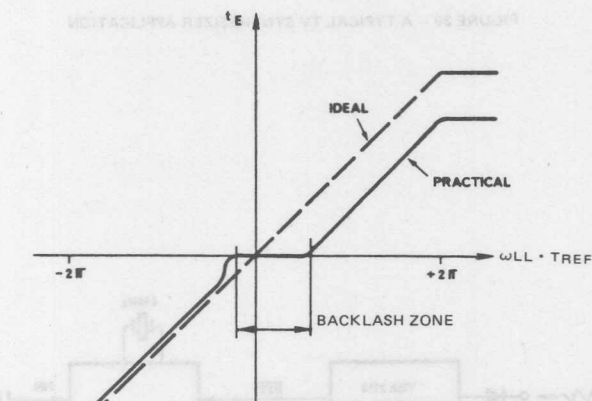


FIGURE 38 — PHASE COMPARATOR WITH PULSE INJECTION

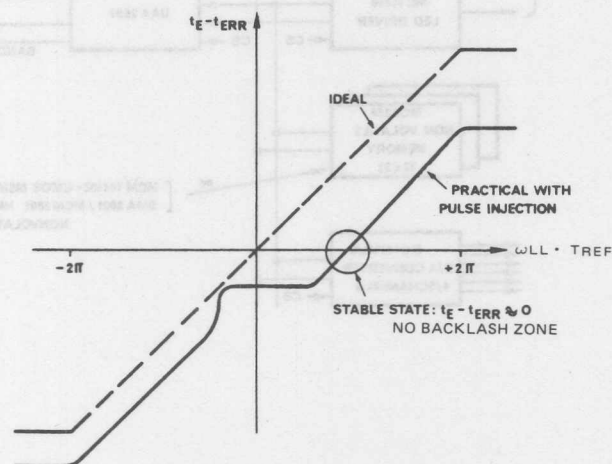
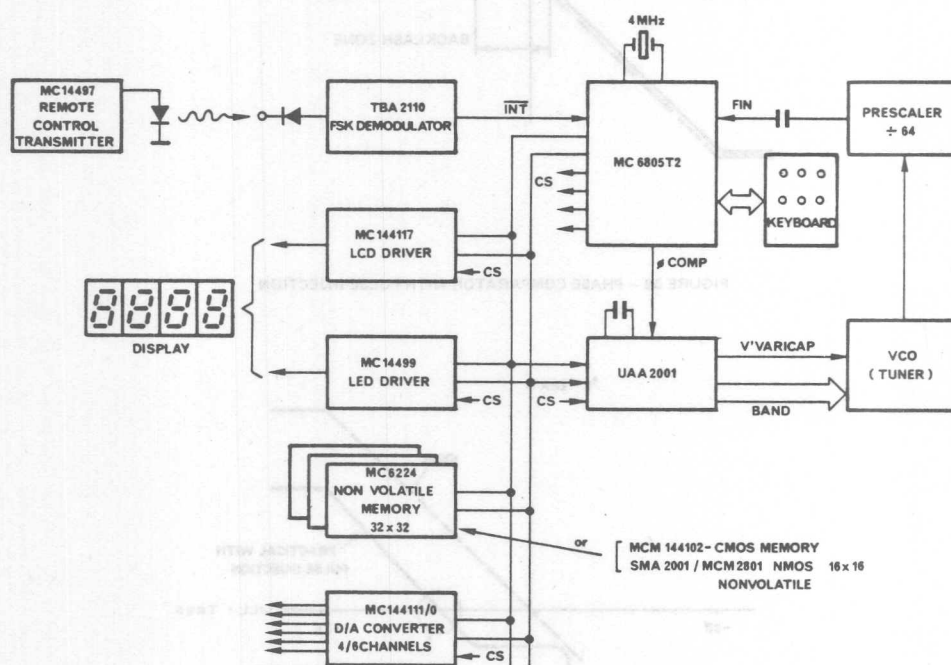


FIGURE 39 - A TYPICAL TV SYNTHESIZER APPLICATION



ORDERING INFORMATION

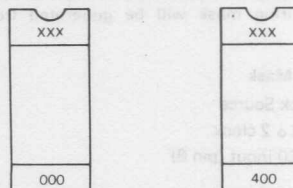
The following information is required when ordering a custom MCU. This information may be transmitted to Motorola in any of the following media:

PROM(s)
Assembler formatted object tape
Punched card deck
Paper tape of card deck format
MDOS disk file

To initiate a ROM pattern for the MCU it is necessary to first contact your local field service office, local sales person or your local Motorola representative.

PROMS — The MCM2708 or MCM2716 type PROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. The PROMs must be clearly marked to indicate which PROM corresponds to which address space (000 3FF HEX). See Figure 40 for recommended marking procedure.

After the PROM(s) are marked they should be placed in conductive IC carriers and securely packed. Do not use styrofoam.

FIGURE 40 — PROM MARKING

XXX = Customer ID

ASSEMBLER FORMATTED OBJECT TAPE —
Cassette tapes produced on a Silent 700 terminal and EXORciser are acceptable.

Customer Name _____
Address _____
City _____
State _____
Phone (____) _____
Contact Mr./Ms. _____
Customer Ref. Number _____
Pattern Media _____
2708 PROM _____
2716 PROM _____
Paper Object Tape _____
Silent 700 Cassette _____
Card Deck _____
Tape to Card Deck _____
MDOS Disk File _____
(None?) _____
Notes: (2) Other media require prior factory approval.
Signature _____
Title _____

OPTION LIST

Select the options for your MCU from the following list.
A manufacturing mask will be generated from this information.

- ☐ ROM Mask
- External Clock Source
- ☐ Gated ϕ 2 clock
- ☐ Port C0 input (pin 8)

Timer Prescaler

- | | |
|---|---|
| <input type="checkbox"/> 2 ⁰ (divide by 1) | <input type="checkbox"/> 2 ⁴ (divide by 16) |
| <input type="checkbox"/> 2 ¹ (divide by 2) | <input type="checkbox"/> 2 ⁵ (divide by 32) |
| <input type="checkbox"/> 2 ² (divide by 4) | <input type="checkbox"/> 2 ⁶ (divide by 64) |
| <input type="checkbox"/> 2 ³ (divide by 8) | <input type="checkbox"/> 2 ⁷ (divide by 128) |
| | <input type="checkbox"/> 2 ¹⁰ (divide by 1024) |

Customer Name _____

Address _____

City _____ State _____ Zip _____

Phone (_____) _____ Extension _____

Contact Ms/Mr _____

Customer Part Number _____

Pattern Media

2708 PROM

2716 PROM

Paper Object Tape

Silent 700 Cassette

Card Deck

Tape of Card Deck

MDOS Disk File

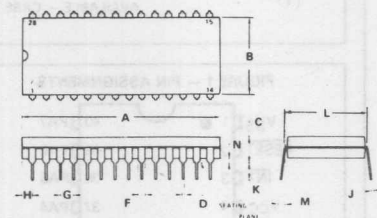
(Note 2) _____

Notes: (2) Other media require prior factory approval.

Signature _____

Title _____

PACKAGE DIMENSIONS



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.38	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24	BSC	0.600	BSC
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

MC6805U2

Advance Information

8-BIT MICROCOMPUTER UNIT

The MC6805U2 Microcomputer Unit (MCU) is a member of the M6805 Family of Microcomputers. This 8-bit microcomputer contains a CPU, on-chip clock, ROM, RAM, I/O, and timer. It is designed for the user who needs an economical microcomputer with the proven capabilities of the M6800-based instruction set. A comparison of the key features of the M6805 Family of Microcomputers is shown in the table on the last page of this data sheet. The following are some of the hardware and software highlights of the MCU. Some of the hardware options are mask programmable.

Hardware Features:

- 8-Bit Architecture
- 64 Bytes of RAM
- Memory Mapped I/O
- 2048 Bytes of User ROM
- Internal 8-Bit Timer with 7-Bit Prescaler
- 4 Vectored Interrupts; Timer, Software and Two External
- 24 TTL/CMOS Compatible I/O Lines with 8 of these LED Compatible
- 8 Input Lines
- Zero-Crossing Detection
- On-Chip Clock Generator
- Self-Check Mode
- Master Reset
- Low Voltage Inhibit
- Complete Development System Support on EXORciser.
- 5 Vdc Single Supply

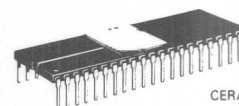
Software Features:

- Similar to M6800
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instructions
- Versatile Interrupt Handling
- Versatile Index Register
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Branches
- Memory Usable as Registers/Flags
- Single Instruction Memory Examine/Change
- 10 Powerful Addressing Modes
- All Addressing Modes Apply to ROM, RAM, and I/O
- User Callable Self-Check Subroutines

HMOS

(HIGH DENSITY
N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

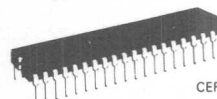
8-BIT MICROCOMPUTER



L SUFFIX
CERAMIC PACKAGE
CASE 715

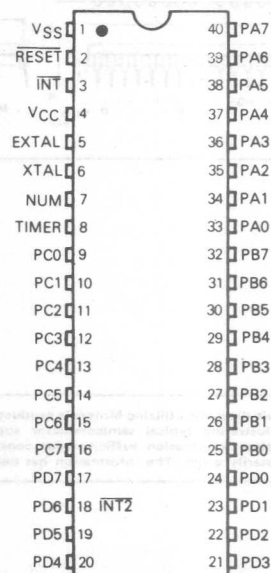


P SUFFIX
PLASTIC PACKAGE
CASE 711



S SUFFIX
CERDIP PACKAGE ALSO
AVAILABLE - CASE 734

FIGURE 1 - PIN ASSIGNMENTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage (Except Pin 6)	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	150	°C
Plastic Package		175	
Ceramic Package		175	
Thermal Resistance	ϕJA	100	°C/W
Plastic Package		50	
Ceramic Package		60	
Cerdip		60	

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.25 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ - 70^\circ\text{C}$ Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	4.0	—	V_{CC}	Vdc
RESET		4.0	2.2*		
INT		+2.0	—		
Input High Voltage Timer	V_{IH}	+2.0	—	V_{CC}	Vdc
Timer Mode		—	9.0	15.0	
Self-Check Mode					
Input Low Voltage	V_{IL}	-0.3	—	0.8	Vdc
RESET		-0.3	2.0*	+1.5	
INT		-0.3	—	+0.8	
All Other					
Reset Voltage	V_{IRES+}	2.0	—	4.0	Vdc
"Out Of"		0.8	—	—	Vdc
"Into"	V_{IRES-}	—	—	—	Vdc
INT Zero — Cross Input Voltage — Through Capacitor	V_{INT}	2	—	4	VacPP
Power Dissipation — No Port Loading $V_{CC} = 5.25 \text{ V}$, $T_J = 0^\circ\text{C}$	P_D	—	600	—	mW
Input Capacitance	C_{in}	—	25	—	pF
EXTAL		—	10	—	
All Other					
Low Voltage Recover	L_{VR}	—	—	4.75	Vdc
Low Voltage Inhibit	L_{VI}	—	3.5	—	Vdc

*Due to internal biasing only.

SWITCHING CHARACTERISTICS ($V_{CC} = +5.25 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ - 70^\circ\text{C}$ Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	f_{osc}	0.4	—	4.2	MHz
Cycle Time ($4/f_{osc}$)	t_{cyc}	0.95	—	10	μs
INT Pulse Width	t_{IWL}, t_{IWH}	$t_{cyc} + 250$	—	—	ns
RESET Pulse Width	t_{RWL}	$t_{cyc} + 250$	—	—	ns
Delay Time Reset (External Cap = $1 \mu\text{F}$ (for $\pm 5^\circ$ Accuracy)	t_{RHL}	—	100	—	ms
INT Zero Cross Detect Input Frequency	f_{INT}	0.03	—	1	kHz
External Clock Input Duty Cycle (Pin 5)	—	40	50	60	%

PORT ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.25 \text{ V} \pm 0.5 \text{ Vdc}$, $V_{SS} = \text{GND}$, $T_A = 0^\circ \text{ to } 70^\circ \text{C}$ Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A					
Output Low Voltage $I_{load} = 1.6 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output High Voltage $I_{load} = -100 \text{ } \mu\text{Adc}$	V_{OH}	2.4	—	—	Vdc
Output High Voltage $I_{load} = -10 \text{ } \mu\text{Adc}$	V_{OH}	$V_{CC} - 1$	—	—	Vdc
Input High Voltage $I_{load} = -300 \text{ } \mu\text{Adc}$ (max)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage $I_{load} = -500 \text{ } \mu\text{Adc}$ (max)	V_{IL}	-0.3	—	+0.8	Vdc
Off-State Input Current, Input 0.8 V	I_{IH}	—	—	-300	μAdc
Off-State Input Current, Input 0.2 V	I_{IL}	—	—	-500	μAdc
Port B					
Output Low Voltage $I_{load} = 3.2 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output Low Voltage $I_{load} = 10 \text{ mAdc}$ (sink)	V_{OL}	—	—	1.0	Vdc
Output High Voltage $I_{load} = -200 \text{ } \mu\text{Adc}$	V_{OH}	2.4	—	—	Vdc
Darlington Current Drive (Source) $V_O = 1.5 \text{ Vdc}$	I_{OH}	-1.0	—	-10	mAdc
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Off-State Input Current	I_{TSI}	—	2	50	μAdc
Port C					
Output Low Voltage $I_{load} = 1.6 \text{ mAdc}$	V_{OL}	—	—	0.4	Vdc
Output High Voltage $I_{load} = -100 \text{ } \mu\text{Adc}$	V_{OH}	2.4	—	—	Vdc
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Off-State Input Current	I_{TSI}	—	2	50	μAdc
Port D (Input Only)					
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	V_{RL}	—	+0.8	Vdc
Input Current					
Timer at $V_{in} = (0.4 \text{ to } 2.4 \text{ Vdc})$	I_{in}	—	—	20	μAdc

POWER CONSIDERATIONS

The average chip junction temperature, T_J , in $^\circ\text{C}$ can be obtained from

$$T_J = T_A + [(P_D + P_{IO}) \cdot \theta_{JA}] \quad (1)$$

Where

T_A = ambient temperature, $^\circ\text{C}$,

θ_{JA} = package thermal resistance, $^\circ\text{C}/\text{watt}$,

P_{IO} = output port power dissipation, watts,

$$= \Sigma(V_{CC} - V_{OH})(|I_{OH}|) + \Sigma(V_{OL})(|I_{OL}|) + \Sigma(V_{CC} - V_{IL})(|I_{IL}|) + \Sigma(V_{CC} - V_{IH})(|I_{IH}|)$$

P_D = chip internal power dissipation, watts.

An approximate relationship between P_D and T_J is

$$P_D = K(T_J + 273) - 0.96 \quad (2)$$

where K is a constant pertaining to the particular part, which may be determined from measurement of P_D immediately after turn-on (i.e., $T_J = T_A$). Using this value of K , then, for any T_A , P_{IO} , and θ_{JA} , the values of P_D and T_J may be obtained for a particular part by an iterative procedure using these two equations. For example, assume that $\theta_{JA} = 50^\circ\text{C}/\text{W}$, maximum $P_{IO} = 150 \text{ mW}$, and P_D is measured for the part to be 400 mW at turn-on at room temperature (25°C). To determine the T_J at a $T_A = 40^\circ\text{C}$, the following iterative procedure is used. First,

Calculate K from equation (2):	$K = (0.400)/(25 + 273) - 0.96 = 94.9$
Estimate T_J from equation (1):	$T_J = 40 + [(0.400 + 0.150) \cdot 50] = 67.5^\circ\text{C}$
Substitute this T_J into eq. (2):	$P_D = 94.9(67.5 + 273) - 0.96 = 0.352 \text{ W}$
Substitute this P_D into eq. (1):	$T_J = 40 + [(0.352 + 0.150) \cdot 50] = 65.1^\circ\text{C}$
Substitute this T_J into eq. (2):	$P_D = 94.9(65.1 + 273) - 0.96 = 0.345 \text{ W}$
Substitute this P_D into eq. (1):	$T_J = 40 + [(0.345 + 0.150) \cdot 50] = 65.2^\circ\text{C}$

Since the last two values obtained for T_J are essentially the same, the iterative process is complete, with the solution $T_J = 65.2^\circ\text{C}$.

FIGURE 2 — MC6805U2 HMOS MICROCOMPUTER BLOCK DIAGRAM

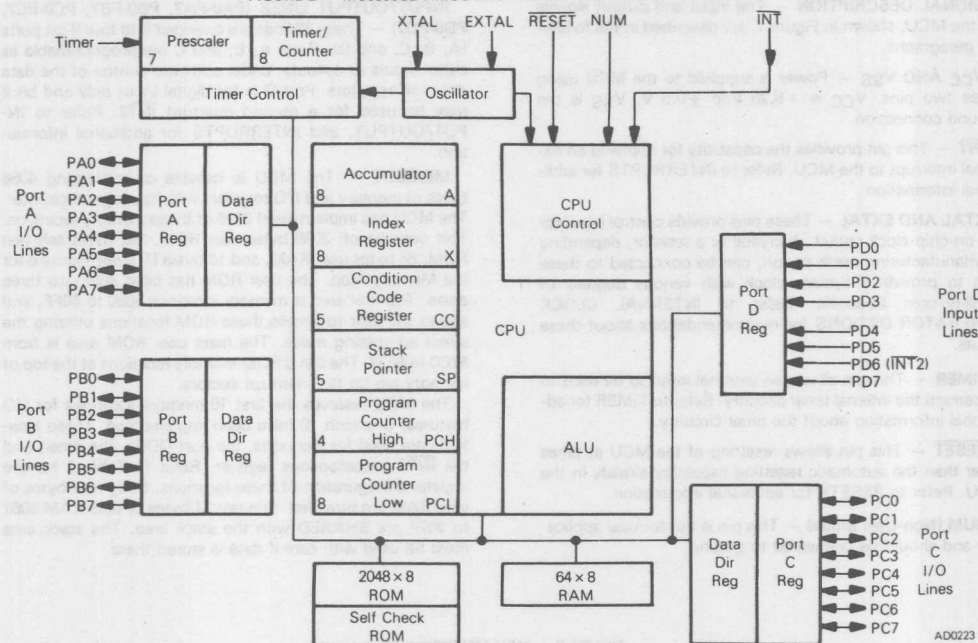


FIGURE 3 — TTL EQUIV. TEST LOAD (PORT B)

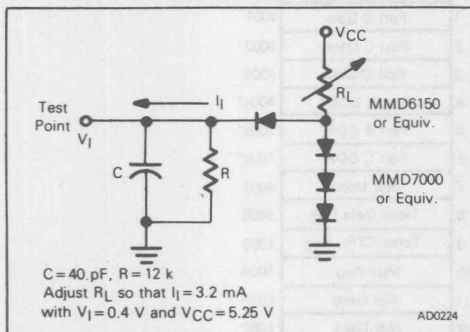


FIGURE 4 — CMOS EQUIV. TEST LOAD (PORT A)

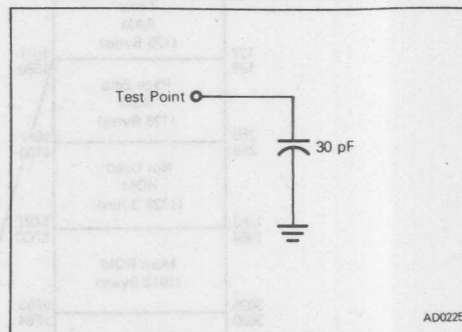
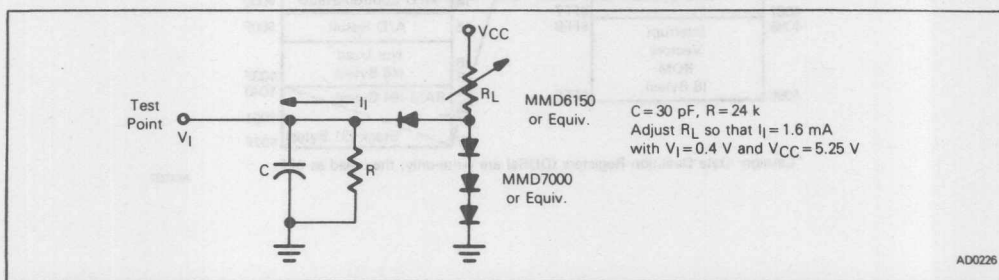


FIGURE 5 — TTL EQUIV. TEST LOAD (PORTS A AND C)



SIGNAL DESCRIPTION — The input and output signals for the MCU, shown in Figure 1, are described in the following paragraphs.

VCC AND VSS — Power is supplied to the MCU using these two pins. VCC is +5.25 Vdc ± 0.5 V. VSS is the ground connection.

INT — This pin provides the capability for applying an external interrupt to the MCU. Refer to INTERRUPTS for additional information.

XTAL AND EXTAL — These pins provide control input for the on-chip clock circuit. A crystal or a resistor, depending on manufacturing mask option, can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Refer to INTERNAL CLOCK GENERATOR OPTIONS for recommendations about these inputs.

TIMER — This pin allows an external input to be used to decrement the internal timer circuitry. Refer to TIMER for additional information about the timer circuitry.

RESET — This pin allows resetting of the MCU at times other than the automatic resetting capability already in the MCU. Refer to RESETS for additional information.

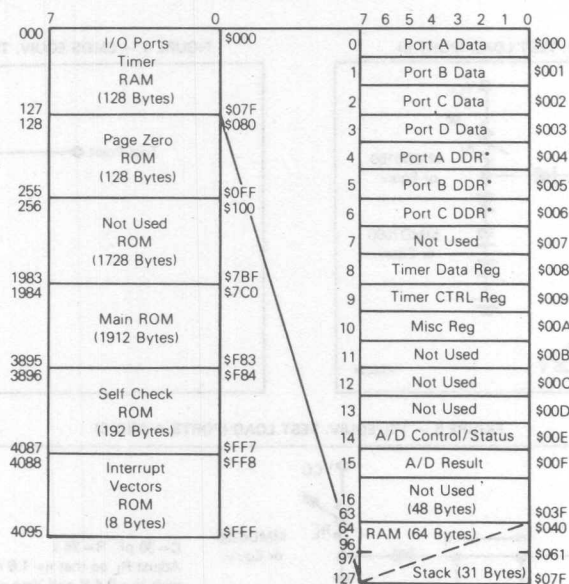
NUM (Non-User Mode) — This pin is not for user application and should be connected to ground.

INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7) — These 32 lines are arranged into four 8-bit ports (A, B, C, and D). Ports A, B, and C are programmable as either inputs or outputs, under software control of the data direction registers. Port D is for digital input only and bit 6 may be used for a second interrupt INT2. Refer to INPUT/OUTPUT, and INTERRUPTS for additional information.

MEMORY — The MCU is capable of addressing 4096 bytes of memory and I/O registers with its program counter. The MCU has implemented 2316 of these memory locations. This consists of: 2048 bytes user ROM, 192 bytes self test ROM, 64 bytes user RAM, and 10 bytes I/O; see Figure 6 for the Memory Map. The user ROM has been split into three areas. The first area is memory locations \$080 to \$0FF, and allows the user to access these ROM locations utilizing the direct addressing mode. The main user ROM area is from \$7C0 to \$F37. The last 8 ROM memory locations at the top of memory are for the interrupt vectors.

The MCU reserves the first 16 memory locations for I/O features, of which 10 have been implemented. These locations are used for the ports, the port DDRs, the timer, and the INT2 miscellaneous register. Refer to Table 2 for the register configuration of these locations. Sixty-four bytes of user RAM are provided. The last 31 bytes of user RAM \$061 to \$07F are SHARED with the stack area. The stack area must be used with care if data is stored there.

FIGURE 6 — MCU MEMORY MAP

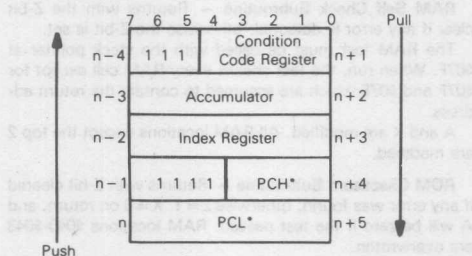


* Caution: Data Direction Registers (DDRs) are write-only; they read as \$FF.

AD0227

The shared stack area is used during the processing of an interrupt. The contents of the MCU registers are pushed on to the stack in the order shown in Figure 7. Since the Stack Pointer decrements during pushes, the low order byte (PCL) of the Program Counter is stacked first; then the high order four bits (PCH) are stacked. This ensures that the program counter is loaded correctly as the stack pointer increments when it pulls data from the stack. A subroutine call will cause only the Program Counter (PCL, PCH) contents to be pushed onto the stack.

FIGURE 7 — INTERRUPT STACKING ORDER



*For subroutine calls, only PCH and PCL are stacked AD0228

REGISTERS — The MCU has five registers available to the programmer. They are shown in Figure 8 and are explained in the following paragraphs.

ACCUMULATOR (A) — The Accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

INDEX REGISTER (X) — The Index Register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit address that may be added to an offset value to create an effective address. The index register can also be used for limited calculations and data manipulations when using

read/modify/write instructions. When not required for Index Addressing, the Index Register can be used as a temporary storage area.

PROGRAM COUNTER (PC) — The Program Counter is a 12-bit register that contains the address of the next instruction to be executed.

STACK POINTER (SP) — The Stack Pointer is a 12-bit register that contains the address of the next free location on the stack. During an MCU reset, or the Reset Stack Pointer (RSP) instruction, the Stack Pointer is set to location \$07F. The Stack Pointer is then decremented as data is pushed on to the stack and incremented as data is then pulled from the stack. The seven most significant bits of the Stack Pointer are permanently set to 000011. Subroutines and interrupts may be nested down to location \$061 which allows the programmer to use up to 15 levels of subroutine calls (less if interrupts are allowed).

CONDITION CODE REGISTER (CC) — The Condition Code Register is a 5-bit register in which each bit is used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each bit is explained in the following paragraphs.

Half Carry (H) — Set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

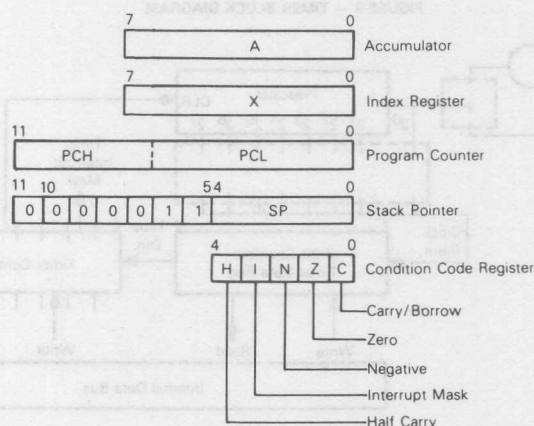
Interrupt (I) — When this bit is set, the timer and external interrupts (INT and INT2) are masked. If an interrupt occurs while this bit is set, the interrupt is latched and will be processed as soon as the interrupt bit is cleared.

Negative (N) — Indicates that the result of the last arithmetic, logical or data manipulation was negative (bit 7 in the result is a logical one).

Zero (Z) — Indicates that the result of the last arithmetic, logical or data manipulation was zero.

Carry/Borrow (C) — Indicates that a carry or borrow out of the Arithmetic Logic Unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

FIGURE 8 — PROGRAMMING MODEL



AD0229

TIMER — The MCU timer circuitry is shown in Figure 9. The 8-bit counter is loaded under program control and is decremented toward zero by the clock input. When the timer reaches zero, the timer interrupt request bit (bit 7) in the Timer Control/Status Register (TCSR) is set. The timer interrupt can be masked by setting the timer interrupt mask bit (bit 6) in the TCSR. The interrupt bit (I-bit) in the Condition Code Register will also prevent a timer interrupt from being processed. The MCU responds to this interrupt by saving the present MCU state in the stack, fetching the timer interrupt vector from locations \$FF8 and \$FF9 and executing the interrupt routine; see Figure 16. THE TIMER INTERRUPT REQUEST BIT MUST BE CLEARED BY SOFTWARE. The timer and INT2 share the same interrupt vector. THE INTERRUPT ROUTINE MUST CHECK THE REQUEST BITS TO DETERMINE THE SOURCE OF THE INTERRUPT.

The clock input to the timer can be from an external source (decrementing of Timer Counter occurs on a positive transition of the external source) applied to the TIMER input pin or it can be the internal $\phi 2$ signal. When the $\phi 2$ signal is used as the source, it can be gated by an input applied to the TIMER input pin allowing the user to easily perform pulse-width measurements. (Note: For ungated $\phi 2$ clock input to the timer prescaler, the timer pin should be tied to V_{CC} .) The source of the clock input is one of the options that has to be specified before manufacture of the MCU. A prescaler option can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before decrementing the counter. This prescaling option must also be specified before manufacturing begins. To avoid truncation errors, the prescaler is cleared when bit 3 of timer control register is written to a logic 1 (this bit always reads as a logic 0). The timer continues to count past zero, falling through to FF16 and then continuing the count. The count can be read at any time by monitoring the Timer Data Register (TDR). This allows a program to determine the length of time since a timer interrupt has occurred, and not disturb the counting process.

At Power-up or Reset, the prescaler and counter are initialized with all logical ones; the timer interrupt request bit

(bit 7) is cleared and the timer interrupt request mask bit (bit 6) is set. Refer to Table 2 for MCU Register Configuration.

SELF CHECK — The self check capability of the MCU provides an internal check to determine if the part is functional. Connect the MCU as shown in Figure 10 and monitor the output of Port C, bit 3 for an oscillation of approximately 7 Hz. A 9 volt level on the timer input, Pin 8, energizes the ROM based self check feature.

Two of the self check subroutines can be called by a user program. They are the RAM and ROM tests. The timer routine may also be called if the timer input is the internal clock.

RAM Self Check Subroutine — Returns with the Z-bit clear if any error is detected; otherwise the Z-bit is set.

The RAM test must be called with the stack pointer at \$07F. When run, the test checks every RAM cell except for \$07F and \$07E which are assumed to contain the return address.

A and X are modified. All RAM locations except the top 2 are modified.

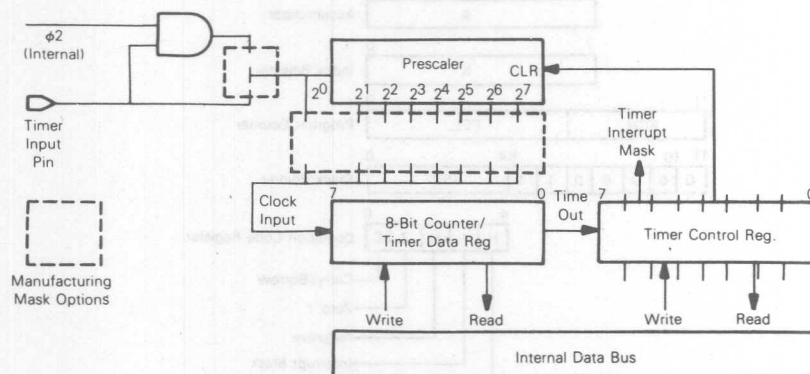
ROM Checksum Subroutine — Returns with Z-bit cleared if any error was found; otherwise Z = 1. X = 0 on return, and A will be zero if the test passed. RAM locations \$040-\$043 are overwritten.

Timer Test — Return with Z-bit cleared if any error was found; otherwise Z = 1.

This runs a simple test on the timer. In order to work correctly as a user subroutine, the internal clock must be the clocking source and interrupts must be disabled. Also, on exit, the clock will be running and the interrupt mask not set so the caller must protect himself from interrupts if necessary.

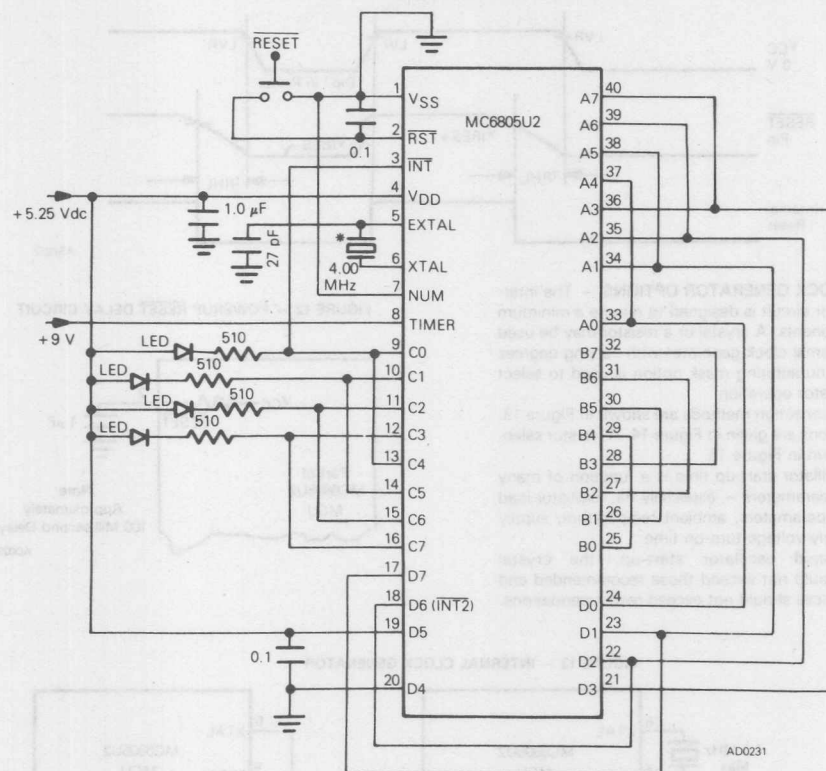
A and X register contents are lost, this routine counts how many times the clock counts in 128 cycles. The number of counts should be a power of two since the prescaler is a power of two. If not, the timer probably is not counting correctly. The routine will also detect if the timer is running at all.

FIGURE 9 — TIMER BLOCK DIAGRAM



AD0230

FIGURE 10 — SELF CHECK CONNECTIONS



*Use jumper if RC mask option is selected. This connection depends on clock oscillator mask option.

LED Meanings

C0	C1	C2	C3	Remarks (1:LED ON; 0:LED OFF)
1	0	1	0	Bad I/O
0	0	1	0	Bad Timer
1	1	0	0	Bad RAM
0	1	0	0	Bad ROM
0	0	0	0	Bad Interrupts or Request Flag
All Flashing				Good Part

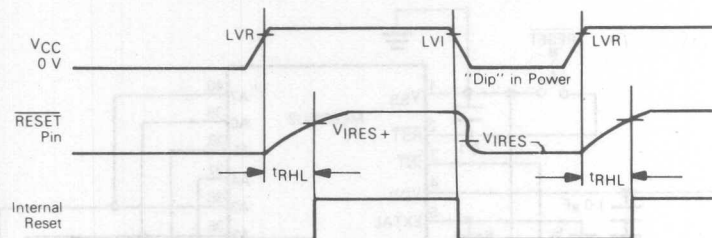
Anything else bad Part, Bad Port 3, Bad ISP, etc.

RESETS — The MCU can be reset three ways: by initial powerup, by the external reset input (RESET) and by an internal low voltage detect circuit, (mask option) see Figure 11. The internal circuit connected to the RESET pin consists of a Schmitt trigger which senses the RESET line logic level. The Schmitt trigger provides an internal reset voltage if it senses a logical 0 on the RESET pin. During powerup, the Schmitt trigger switches on (removes reset) when the RESET pin voltage rises to $V_{IRES} +$. When the RESET pin voltage falls

to a logical 0 for a period longer than one E cycle, the Schmitt trigger switches off to provide an internal reset voltage. The "switch off" voltage occurs at $V_{IRES} +$.

Upon powerup, a delay of t_{RHL} is needed before allowing the RESET input to go high. This time allows the internal clock generator to stabilize. Connecting a capacitor to the RESET input as shown in Figure 12 will typically provide sufficient delay.

FIGURE 11 — POWER AND RESET TIMING



AS0232

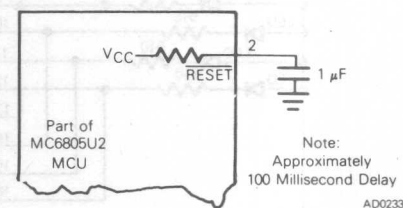
INTERNAL CLOCK GENERATOR OPTIONS — The internal clock generator circuit is designed to require a minimum of external components. A crystal or a resistor may be used to control the internal clock generator with varying degrees of stability. A manufacturing mask option is used to select the crystal or resistor operation.

The different connection methods are shown in Figure 13. Crystal specifications are given in Figure 14. A resistor selection graph is shown in Figure 15.

The crystal oscillator start-up time is a function of many variables: crystal parameters — especially R_s , oscillator load capacitances, IC parameters, ambient temperature, supply voltage, and supply voltage turn-on time.

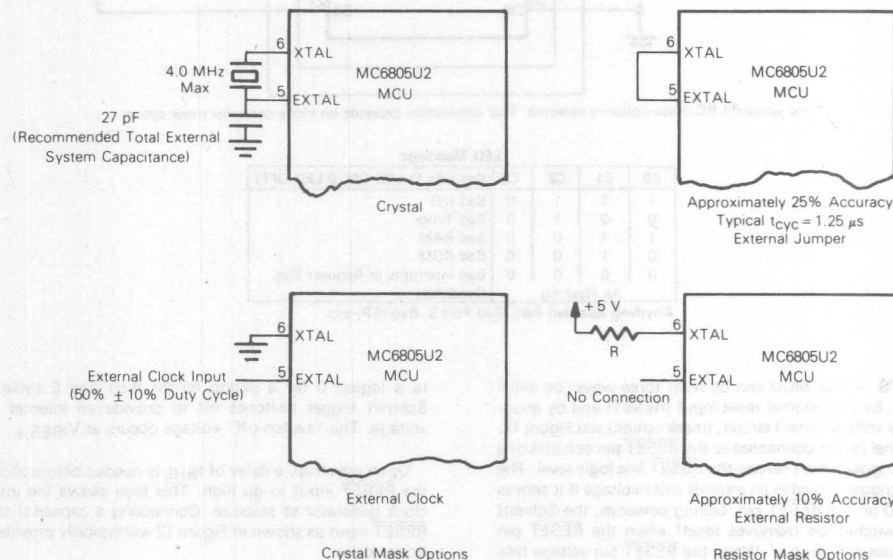
To ensure rapid oscillator start-up, the crystal characteristics should not exceed those recommended and the load capacitances should not exceed recommendations.

FIGURE 12 — POWERUP RESET DELAY CIRCUIT



AD0233

FIGURE 13 — INTERNAL CLOCK GENERATOR



AD0234

Note: All connections to pins 5 and 6 should have leads as short as possible.

FIGURE 14 — CRYSTAL PARAMETERS

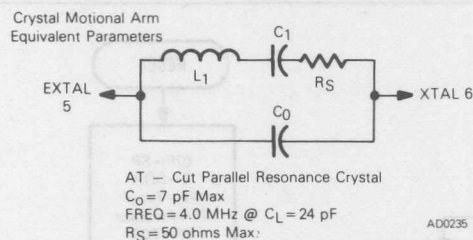
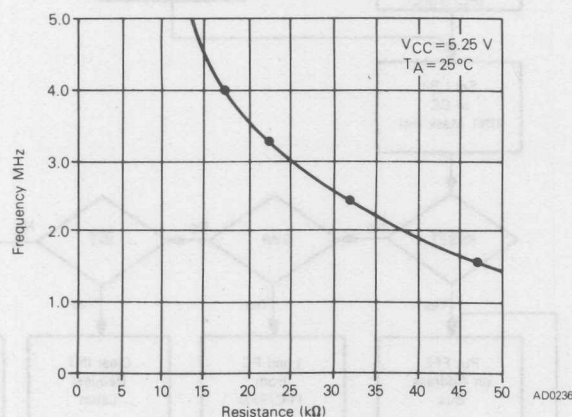


FIGURE 15 — TYPICAL RESISTOR SELECTION GRAPH



INTERRUPTS — The MCU can be interrupted four different ways: through the external interrupt ($\overline{\text{INT}}$) input pin, the internal timer interrupt request, the external port D bit 6 (INT2) input pin, and a software interrupt instruction (SWI). When any interrupt occurs, processing is suspended, the present MCU state is pushed onto the stack, the interrupt bit (I-bit) in the Condition Code Register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. Refer to Figure 16 for Flowchart. The interrupt service routines must end with a Return from Interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt. Table 1 provides a listing of the interrupts, their priority, and the address of the vector which contains the starting address of the appropriate interrupt service routine. RESET is listed in Table 1 because it is processed similar to an interrupt. However, it is not normally used as an interrupt. Note: The timer and INT2 share the same vector address. The interrupt routine must determine the source by examining the interrupt request bits (TCR bit 7 and MR bit 7). Both TCR bit 7 and MR bit 7 can only be written to 0 by software.

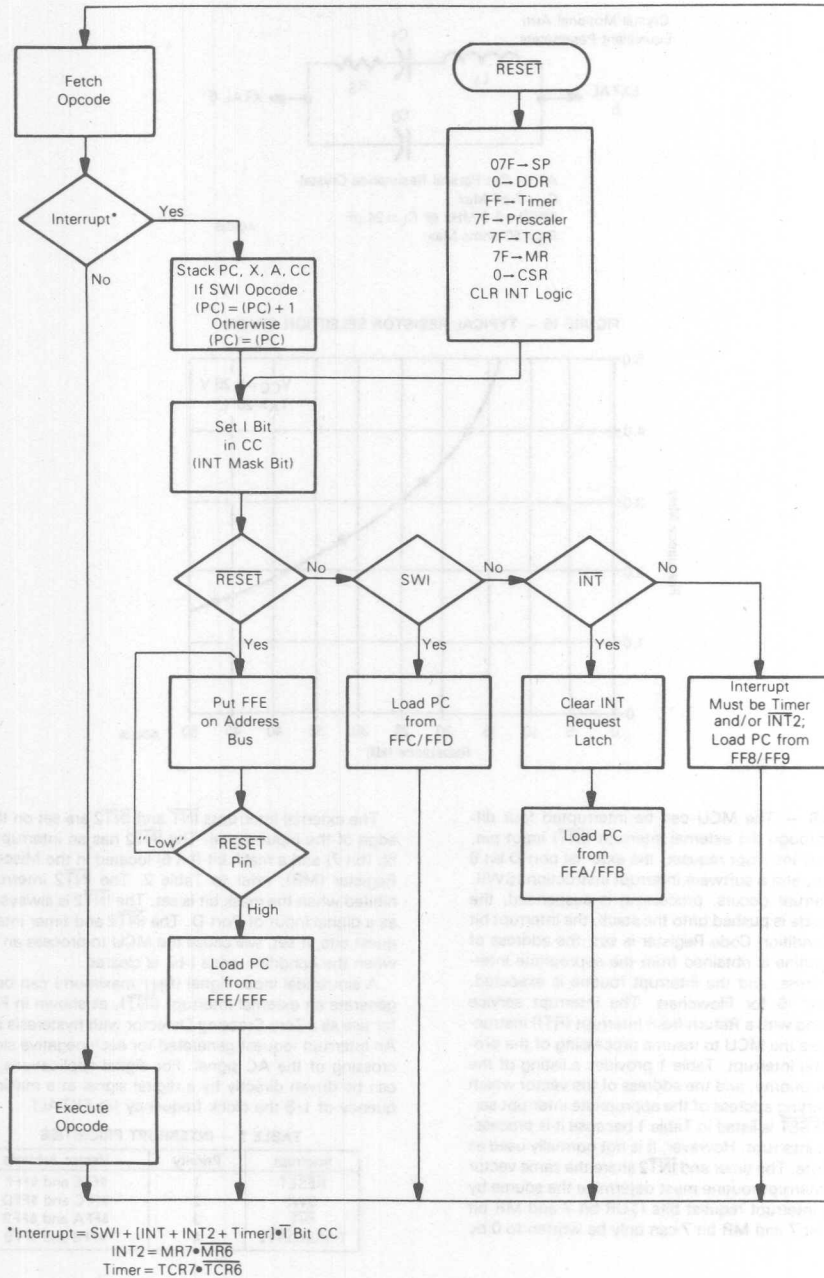
The external interrupts $\overline{\text{INT}}$ and INT2 are set on the falling edge of the input signal. The INT2 has an interrupt request bit (bit 7) and a mask bit (bit 6) located in the Miscellaneous Register (MR), refer to Table 2. The INT2 interrupt is inhibited when the mask bit is set. The INT2 is always readable as a digital input of Port D. The $\overline{\text{INT}}$ and timer interrupt request bits, if set, will cause the MCU to process an interrupt when the condition code I-bit is cleared.

A sinusoidal input signal (f_{INT} maximum) can be used to generate an external interrupt ($\overline{\text{INT}}$), as shown in Figure 17, for use as a Zero Crossing Detector with hysteresis included. An interrupt request generated for each negative slope, zero crossing of the AC signal. For digital applications, the $\overline{\text{INT}}$ can be driven directly by a digital signal at a maximum frequency of $1/8$ the clock frequency (at EXTAL).

TABLE 1 — INTERRUPT PRIORITIES

Interrupt	Priority	Vector Address
RESET	1	\$FFE and \$FFF
SWI	2	\$FFC and \$FFD
$\overline{\text{INT}}$	3	\$FFA and \$FFB
TIMER/ INT2	4	\$FF8 and \$FF9

FIGURE 16 — INTERRUPT PROCESSING FLOW CHART



INPUT/OUTPUT — There are 32 input or input/output pins. All pins on ports A, B and C are programmable as either inputs or outputs under software control of corresponding Data Direction Registers (DDRs). The port I/O programming is accomplished by setting the corresponding bit in the ports DDR to a logic "1" for output or a logic "0" for input. On reset all the DDRs are initialized to a logic "0" state, placing the ports in the input mode. The port output registers are not initialized on reset and should be initialized by software before changing the DDRs from input to output. When programmed as outputs, all I/O pins read latched output data, regardless of the logic levels at the output pin due to output loading; refer to Figure 18.

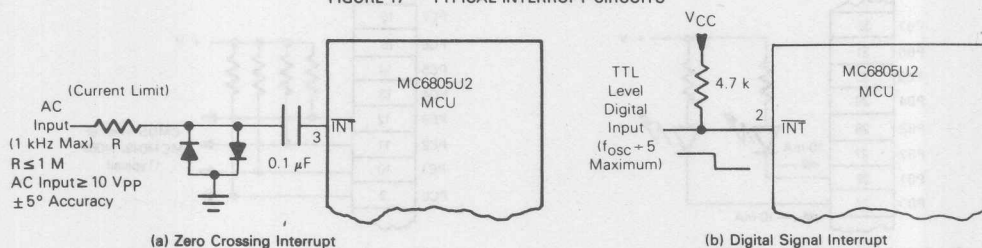
All input/output lines are TTL compatible as both inputs

and outputs. Port A lines are CMOS compatible as outputs. Port B, C and D lines are CMOS compatible as inputs. Port D lines are input only; thus, there is no corresponding DDR. When programmed as outputs, Port B is capable of sinking 10 milliamperes on each pin and sourcing 1.0 milliamperes on each pin.

Figure 19 provides some examples of port connections. The Memory Map, in Figure 6, gives the addresses of data registers and DDRs. The Register Configuration is provided in Table 2.

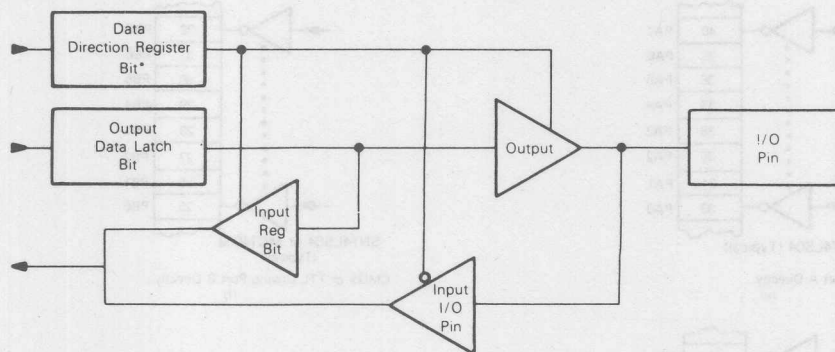
Caution: The corresponding DDRs of Port A, B and C are write-only registers. These registers will read (via any Register/Memory, Read/Modify/Write, BSET/BCLR, or BRSET/BRCLR instruction) as all 1's (FF₁₆).

FIGURE 17 — TYPICAL INTERRUPT CIRCUITS



AD0238

FIGURE 18 — TYPICAL PORT I/O CIRCUITRY



AD0239

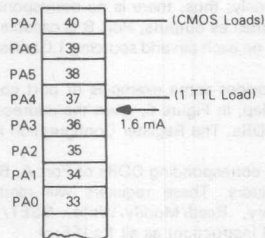
*Write Only Registers

Data Direction Register Bit	Output Data Bit	Output State	Input To MCU
1	0	0	0
1	1	1	1
0	X	3-State**	Pin

**Ports B and C Only

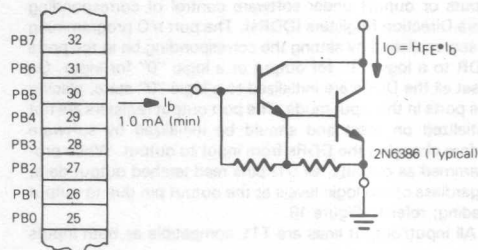
FIGURE 19 — TYPICAL PORT CONNECTIONS

Output Modes



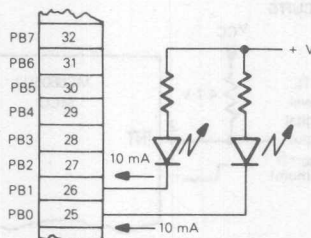
Port A, Bit 7 Programmed as Output, Driving CMOS Loads and Bit 4 Driving one TTL Load Directly

(a)



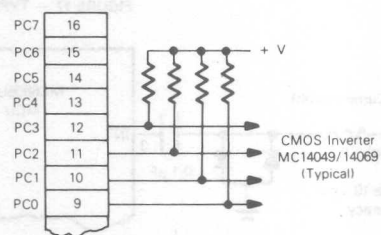
Port B, Bit 5 Programmed as Output, Driving Darlington-Base Directly

(b)



Port B, Bit 0 and Bit 1 Programmed as Output, Driving LEDs Directly

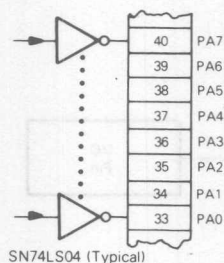
(c)



Port C, Bits 0-3 Programmed as Output, Driving CMOS Loads, Using External Pullup Resistors

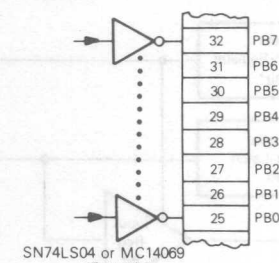
(d)

Input Modes



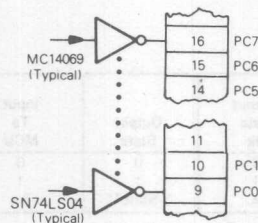
TTL Driving Port A Directly

(e)



CMOS or TTL Driving Port B Directly

(f)



CMOS and TTL Driving Port C Directly

(g)

BIT MANIPULATION — The MCU has the ability to set or clear any single RAM or input/output bit (except the data direction registers, see Caution on page 12) with a single instruction (BSET, BCLR). Any bit in the page zero including ROM, except the DDRs, can be tested using the BRSET and BRCLR instructions and the program branches as a result of its state. The Carry bit (C) will equal the value of the bit referenced by BRSET or BRCLR. The capability to work with any bit in RAM, ROM or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines. The coding example in Figure 20 illustrates the usefulness of the bit manipulation and test instructions. Assume that the MCU is to communicate with an external serial device. The external device has a data ready signal, a data output line, and a clock line to clock data one bit at a time, LSB first, out of the device. The MCU waits until the data is ready, clocks the external device, picks up the data in the Carry Flag (C-bit), clears the clock line and finally accumulates the data bits in a RAM location.

ADDRESSING MODES

The M6805 Family has ten addressing modes available for use by the programmer. They are explained briefly in the following paragraphs. For additional details and graphical illustrations, refer to the M6805, M146805 Family Users Manual.

The term "effective address" (EA) is sometimes used in describing the addressing modes and it is defined as the address from which the argument for an instruction is fetched or stored.

IMMEDIATE — In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

DIRECT — In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes all on-chip RAM and I/O registers and up to 128 bytes of ROM. Direct addressing is an effective use of both memory and speed.

EXTENDED — In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing

mode are capable of referencing arguments anywhere in memory with a single three byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler will automatically select the shortest form of the instruction.

RELATIVE — The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if, and only if, the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is limited to +129, -126 from the opcode address. The programmer need not worry about calculating the correct offset if he uses the Motorola assembler, since it calculates the proper offset and checks to see if it is within the span of the branch.

INDEXED, NO OFFSET — In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long and are therefore fast. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

INDEXED, 8-BIT OFFSET — In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. This addressing mode is useful in selecting the kth element in an n element table.

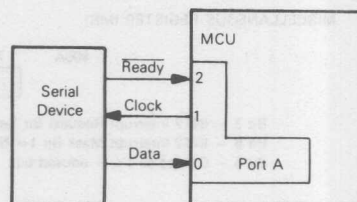
INDEXED, 16-BIT OFFSET — In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed, 8-bit offset; except that this three byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). As with direct and extended, the Motorola assembler will determine the shortest form of indexed addressing.

BIT SET/CLEAR — In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode and the byte following the opcode specifies the address of the byte in which the specified bit is to be set or cleared. Thus, any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two byte instruction. See Caution on page 12.

FIGURE 20 — BIT MANIPULATION EXAMPLE

```

*      BRSET  2,PORTA,* WAIT FOR READY
      BSET   1,PORTA  CLOCK NEXT BIT IN
      BRCLR  0,PORTA,NEXT PICKUP BIT IN C-BIT
NEXT   BCLR  1,PORTA  RETURN CLOCK LINE HIGH
      ASR    RAMLOC  MOVE C-BIT INTO RAM
  
```



AD0242

BIT TEST AND BRANCH — Bit test and branch is a combination of direct addressing and relative addressing. The bit and condition (set or clear) to be tested is part of the opcode and the address of the byte to be tested is in the single byte immediately following the opcode byte. The signed relative 8-bit offset is in the third byte and is added to the PC if the specified bit is set or clear in the specified memory location. This single three byte instruction allows the program to

branch based on the condition of any readable bit in the first 256 location of memory. The span of branching is +130, -125 from the opcode address. See Caution on page 12.

INHERENT — In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are also included in this mode.

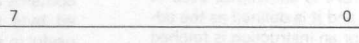
TABLE 2 — MCU REGISTER CONFIGURATION

PORT DATA DIRECTION REGISTER (DDR)



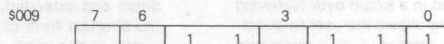
- (1) Write Only; reads as all 1's
- (2) 1 = Output, 0 = Input
- (3) Port A ADDR = \$004
- Port B ADDR = \$005
- Port C ADDR = \$006
- Port D ADDR = None; Port D is Input only

PORT DATA REGISTER



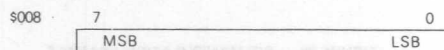
- Port A ADDR = \$000
- Port B ADDR = \$001
- Port C ADDR = \$002
- Port D ADDR = \$003

TIMER CONTROL/STATUS REGISTER (TCSR)

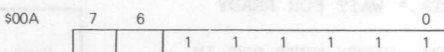


- Bit 7 — Timer Interrupt Request Status Bit Set when TDR goes to zero; must be cleared by software
- Bit 6 — Timer Interrupt Mask Bit; 1 = timer masked (disabled)
- Bit 3 — Always reads as a 0; clears prescaler when written to a logic 1
- Bits 5, 4, 2, 1, 0 read 1's — unused bits

TIMER DATA REGISTER (TDR)



MISCELLANEOUS REGISTER (MRI)



- Bit 7 — INT2 Interrupt Request Bit Set when falling edge detected on INT2 pin must be cleared by software
- Bit 6 — INT2 Interrupt Mask Bit 1 = INT2 Interrupt masked (disabled)
- Bit 5 — 0 Read as 1's — unused bits

INSTRUCTION SET

The MCU has a set of 59 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

BRANCH INSTRUCTIONS — The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 3.

BIT MANIPULATION INSTRUCTIONS — These instructions are used on any bit in the first 256 bytes of the memory, see Caution on page 12. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 4.

REGISTER/MEMORY INSTRUCTIONS — Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is ob-

tained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 5.

READ/MODIFY/WRITE INSTRUCTIONS — These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register, see Caution on page 12. The test for negative or zero (TST) instruction is included in the read/modify/write instruction even though it does not perform the write. Refer to Table 6.

CONTROL INSTRUCTIONS — The control instructions control the MCU operations during program execution. Refer to Table 7.

ALPHABETICAL LISTING — The complete instruction set is given in alphabetical order in Table 8.

OPCODE MAP — Table 9 is an opcode map for the instructions used on the MCU.

TABLE 3 — BRANCH INSTRUCTIONS

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	HMOS/CMOS # Of Cycles
Branch Always	BRA	20	2	4/3
Branch Never	BRN	21	2	4/3
Branch IFF Higher	BHI	22	2	4/3
Branch IFF Lower or Same	BLS	23	2	4/3
Branch IFF Carry Clear	BCC	24	2	4/3
(Branch IFF Higher or Same)	(BHS)	24	2	4/3
Branch IFF Carry Set	BCS	25	2	4/3
(Branch IFF Lower)	(BLO)	25	2	4/3
Branch IFF Not Equal	BNE	26	2	4/3
Branch IFF Equal	BEQ	27	2	4/3
Branch IFF Half Carry Clear	BHCC	28	2	4/3
Branch IFF Half Carry Set	BHCS	29	2	4/3
Branch IFF Plus	BPL	2A	2	4/3
Branch IFF Minus	BMI	2B	2	4/3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	4/3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	4/3
Branch IFF Interrupt Line is Low	BIL	2E	2	4/3
Branch IFF Interrupt Line is High	BIH	2F	2	4/3
Branch to Subroutine	BSR	AD	2	8/6

TABLE 4 — BIT MANIPULATION INSTRUCTIONS

Function	Mnemonic	Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	HMOS/CMOS # of Cycles
Branch IFF Bit n is set	BRSET n (n = 0...7)	—	—	—	2 • n	3	10/5
Branch IFF Bit n is clear	BRCLR n (n = 0...7)	—	—	—	01 + 2 • n	3	10/5
Set Bit n	BSET n (n = 0...7)	10 + 2 • n	2	7/5	—	—	—
Clear bit n	BCLR n (n = 0...7)	11 + 2 • n	2	7/5	—	—	—

TABLE 5 — REGISTER/MEMORY INSTRUCTIONS

Function	Mnem.	Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
		Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)
Load A from Memory	LDA	A6	2	2/2	B6	2	4/3	C6	3	5/4	F6	1	4/3	E6	2	5/4	D6	3	6/5
Load X from Memory	LDX	AE	2	2/2	BE	2	4/3	CE	3	5/4	FE	1	4/3	EE	2	5/4	DE	3	6/5
Store A in Memory	STA	—	—	—	B7	2	5/4	C7	3	6/5	F7	1	5/4	E7	2	6/5	D7	3	7/6
Store X in Memory	STX	—	—	—	BF	2	5/4	CF	3	6/5	FF	1	5/4	EF	2	6/5	DF	3	7/6
Add Memory to A	ADD	A8	2	2/2	BB	2	4/3	CB	3	5/4	FB	1	4/3	EB	2	5/4	DB	3	6/5
Add Memory and Carry to A	ADC	A9	2	2/2	B9	2	4/3	C9	3	5/4	F9	1	4/3	E9	2	5/4	D9	3	6/5
Subtract Memory	SUB	A0	2	2/2	B0	2	4/3	C0	3	5/4	F0	1	4/3	E0	2	5/4	D0	3	6/5
Subtract Memory from A with Borrow	SBC	A2	2	2/2	B2	2	4/3	C2	3	5/4	F2	1	4/3	E2	2	5/4	D2	3	6/5
AND Memory to A	AND	A4	2	2/2	B4	2	4/3	C4	3	5/4	F4	1	4/3	E4	2	5/4	D4	3	6/5
OR Memory with A	ORA	AA	2	2/2	BA	2	4/3	CA	3	5/4	FA	1	4/3	EA	2	5/4	DA	3	6/5
Exclusive OR Memory with A	EOR	A8	2	2/2	B8	2	4/3	C8	3	5/4	F8	1	4/3	E8	2	5/4	D8	3	6/5
Arithmetic Compare A with Memory	CMP	A1	2	2/2	B1	2	4/3	C1	3	5/4	F1	1	4/3	E1	2	5/4	D1	3	6/5
Arithmetic Compare X with Memory	CPX	A3	2	2/2	B3	2	4/3	C3	3	5/4	F3	1	4/3	E3	2	5/4	D3	3	6/5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2/2	B5	2	4/3	C5	3	5/4	F5	1	4/3	E5	2	5/4	D5	3	6/5
Jump Unconditional	JMP	—	—	—	BC	2	3/2	CC	3	4/3	FC	1	3/2	EC	2	4/3	DC	3	5/4
Jump to Subroutine	JSR	—	—	—	BD	2	7/6	CD	3	8/6	FD	1	7/5	ED	2	8/7	DD	3	9/7

NOTE: The cycles column actually shows the number of HMOS/CMOS cycles (e.g., 4/3 indicates 4 HMOS cycles or 3 CMOS cycles).

TABLE 6 — READ/MODIFY/WRITE INSTRUCTIONS

Function	Mnem.	Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
		Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)	Op Code	# Bytes	Cycles (see note)
Increment	INC	4C	1	4/3	5C	1	4/3	3C	2	6/5	7C	1	6/5	6C	2	7/6
Decrement	DEC	4A	1	4/3	5A	1	4/3	3A	2	6/5	7A	1	6/5	6A	2	7/6
Clear	CLR	4F	1	4/3	5F	1	4/3	3F	2	6/5	7F	1	6/5	6F	2	7/6
Complement	COM	43	1	4/3	53	1	4/3	33	2	6/5	73	1	6/5	63	2	7/6
Negate (2's complement)	NEG	40	1	4/3	50	1	4/3	30	2	6/5	70	1	6/5	60	2	7/6
Rotate Left Thru Carry	ROL	49	1	4/3	59	1	4/3	39	2	6/5	79	1	6/5	69	2	7/6
Rotate Right Thru Carry	ROR	46	1	4/3	56	1	4/3	36	2	6/5	76	1	6/5	66	2	7/6
Logical Shift Left	LSL	48	1	4/3	58	1	4/3	38	2	6/5	78	1	6/5	68	2	7/6
Logical Shift Right	LSR	44	1	4/3	54	1	4/3	34	2	6/5	74	1	6/5	64	2	7/6
Arithmetic Shift Right	ASR	47	1	4/3	57	1	4/3	37	2	6/5	77	1	6/5	67	2	7/6
Test for Negative or Zero	TST	4D	1	4/3	5D	1	4/3	3D	2	6/4	7D	1	6/4	6D	2	7/5

NOTE: The cycles column actually shows the number of HMOS/CMOS cycles (e.g., 4/3 indicates 4 HMOS cycles or 3 CMOS cycles).

TABLE 7 — CONTROL INSTRUCTIONS

Function	Mnemonic	Inherent		
		Op Code	# Bytes	HMOS/CMOS # of Cycles
Transfer A to X	TAX	97	1	2/2
Transfer X to A	TXA	9F	1	2/2
Set Carry Bit	SEC	99	1	2/2
Clear Carry Bit	CLC	98	1	2/2
Set Interrupt Mask Bit	SEI	9B	1	2/2
Clear Interrupt Mask Bit	CLI	9A	1	2/2
Software Interrupt	SWI	83	1	11/10
Return from Subroutine	RTS	81	1	6/6
Return from Interrupt	RTI	80	1	9/9
Reset Stack Pointer	RSP	9C	1	2/2
No-Operation	NOP	9D	1	2/2
Enable IRQ, Stop Oscillator*	STOP	8E	1	-/2
Enable Interrupt, Stop Processor*	WAIT	8F	1	-/2

*CMOS Instructions

TABLE 8 — INSTRUCTION SET

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	*	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	*	Λ	Λ	Λ
AND		X	X	X		X	X	X			*	*	Λ	Λ	*
ASL	X		X			X	X				*	*	Λ	Λ	Λ
ASR	X		X			X	X				*	*	Λ	Λ	Λ
BCC					X						*	*	*	*	*
BCLR									X		*	*	*	*	*
BCS					X						*	*	*	*	*
BEQ					X						*	*	*	*	*
BHCC					X						*	*	*	*	*
BHCS					X						*	*	*	*	*
BHI					X						*	*	*	*	*
BHS					X						*	*	*	*	*
BIH					X						*	*	*	*	*
BIL					X						*	*	*	*	*
BIT		X	X	X		X	X	X			*	*	Λ	Λ	*
BLO					X						*	*	*	*	*
BLS					X						*	*	*	*	*
BMC					X						*	*	*	*	*
BMI					X						*	*	*	*	*
BMS					X						*	*	*	*	*
BNE					X						*	*	*	*	*
BPL					X						*	*	*	*	*
BRA					X						*	*	*	*	*
BRN					X						*	*	*	*	*
BRCLR										X	*	*	*	*	Λ
BRSET										X	*	*	*	*	Λ
BSET									X		*	*	*	*	*
BSR					X						*	*	*	*	*
CLC	X										*	*	*	*	0
CLI	X										*	0	*	*	*
CLR	X		X			X	X				*	*	0	1	*
CMP		X	X	X		X	X	X			*	*	Λ	Λ	Λ
COM	X		X			X	X				*	*	Λ	Λ	1
CPX		X	X	X		X	X	X			*	*	Λ	Λ	Λ

TABLE 8 — INSTRUCTION SET (CONTINUED)

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/Clear	Bit Test & Branch	H	I	N	Z	C
DEC	X		X			X	X				•	•	Δ	Δ	•
EOR		X	X	X		X	X	X			•	•	Δ	Δ	•
INC	X		X			X	X				•	•	Δ	Δ	•
JMP			X	X		X	X	X			•	•	•	•	•
JSR			X	X		X	X	X			•	•	•	•	•
LDA		X	X	X		X	X	X			•	•	Δ	Δ	•
LDX		X	X	X		X	X	X			•	•	Δ	Δ	•
LSL	X		X			X	X				•	•	Δ	Δ	Δ
LSR	X		X			X	X				•	•	0	Δ	Δ
NEQ	X		X			X	X				•	•	Δ	Δ	Δ
NOP	X										•	•	•	•	•
ORA		X	X	X		X	X	X			•	•	Δ	Δ	•
ROL	X		X			X	X				•	•	Δ	Δ	Δ
RSP	X										•	•	•	•	•
RTI	X										?	?	?	?	?
RTS	X										•	•	•	•	•
SBC		X	X	X		X	X	X			•	•	Δ	Δ	Δ
SEC	X										•	•	•	•	1
SEI	X										•	1	•	•	•
STA			X	X		X	X	X			•	•	Δ	Δ	•
STX			X	X		X	X	X			•	•	Δ	Δ	•
STOP*	X										•	1	•	•	•
SUB		X	X	X		X	X	X			•	•	Δ	Δ	Δ
SWI	X										•	0	•	•	•
TAX	X										•	•	•	•	•
TST	X		X			X	X				•	•	Δ	Δ	•
TXA	X										•	•	•	•	•
WAIT*	X										•	0	•	•	•

*CMOS Instructions Only

Condition Code Symbols

H Half Carry (From Bit 3)
 I Interrupt Mask
 N Negative (Sign Bit)
 Z Zero

C Carry/Borrow
 Δ Test and Set if True, Cleared Otherwise
 • Not Affected
 ? Load CC Register From Stack

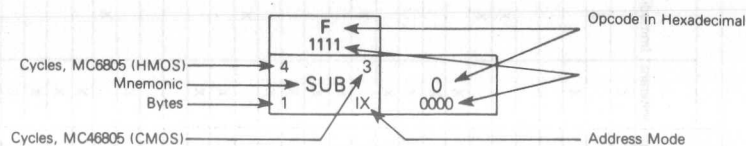
TABLE 9 — MC6805/MC1467805 INSTRUCTION SET OP CODE MAP

	Bit Manipulation		Branch		Read/Modify/Write				Control		Register/Memory						
	BTB	BSC	REL	DIR	INH(A)	INH(X)	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
Low	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Hi
0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	0
0	BRSET0	BSET0	BRA	NEG	NEGA	NEGX	NEG	RTI			SUB	SUB	SUB	SUB	SUB	SUB	0
1	BRCLR0	BCLR0	BRN					RTS			CMP	CMP	CMP	CMP	CMP	CMP	1
2	BRSET1	BSET1	BHI								SBC	SBC	SBC	SBC	SBC	SBC	2
3	BRCLR1	BCLR1	BLS	COM	COMA	COMX	COM	COM	SWI		CPX	CPX	CPX	CPX	CPX	CPX	3
4	BRSET2	BSET2	BCC	LSR	LSRA	LSRX	LSR	LSR			AND	AND	AND	AND	AND	AND	4
5	BRCLR2	BCLR2	BCS								BIT	BIT	BIT	BIT	BIT	BIT	5
6	BRSET3	BSET3	BNE	ROR	RORA	RORX	ROR	ROR			LDA	LDA	LDA	LDA	LDA	LDA	6
7	BRCLR3	BCLR3	BEQ	ASR	ASRA	ASRX	ASR	ASR	TAX		STA	STA	STA	STA	STA	STA	7
8	BRSET4	BSET4	BHCC	LSL	LSLA	LSLX	LSL	LSL	CLC		EOR	EOR	EOR	EOR	EOR	EOR	8
9	BRCLR4	BCLR4	BHCS	ROL	ROLA	ROLX	ROL	ROL	SEC		ADC	ADC	ADC	ADC	ADC	ADC	9
A	BRSET5	BSET5	BPL	DEC	DECA	DECX	DEC	DEC	CLI		ORA	ORA	ORA	ORA	ORA	ORA	A
B	BRCLR5	BCLR5	BMI						SEI		ADD	ADD	ADD	ADD	ADD	ADD	B
C	BRSET6	BSET6	BMC	INC	INCA	INCX	INC	INC	RSP		JMP	JMP	JMP	JMP	JMP	JMP	C
D	BRCLR6	BCLR6	BMS	TST	TSTA	TSTX	TST	TST	NOP		BSR	BSR	BSR	BSR	BSR	BSR	D
E	BRSET7	BSET7	BIL						STOP		LDX	LDX	LDX	LDX	LDX	LDX	E
F	BRCLR7	BCLR7	BIH	CLR	CLRA	CLRX	CLR	CLR	WAIT	TXA	STX	STX	STX	STX	STX	STX	F

Abbreviations for Address Modes

INH	Inherent
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset

LEGEND



*CMOS only

AD0052

STANDALONE EVALUATION PROGRAMS

The MC6805U2L1/P1 is a device containing two separate ROM programs which can be used to evaluate the performance of the MC6805U2. The two programs allow the user to operate the part in a monitor mode or as an ASCII keyboard encoder. The monitor mode allows the user to examine, change and execute programs in the memory through a series of commands. There are 43 bytes in RAM, locations 4C to 76 where the user can write and execute his own evaluation program. Note: The upper RAM memory limit will vary depending on stack usage. The following is a list of commands available to the user.

R — Print registers. Format is CCCC AA XX PP.

A — Print/change A accumulator. Prints the register value, then waits for new value. Type any non-hex character to exit.

X — Print/change X accumulator. Works the same as "A", except modifies X instead.

M — Memory examine/change. Type M AAA to begin, then type

- to re-examine current
- A** — to examine previous
- CR** — to examine next
- DD** — new data

Anything else exists memory command.

C — Continue program. Execution starts at the location specified in the program counter, and continues until an SWI is executed or until reset.

E — Execute from address. Format is E AAA. AAA is any valid memory address.

S — Display Machine State. All important registers are displayed, as well as all 64 bytes of RAM.

Figure 21 shows the connection diagram for the Monitor/Keyboard Evaluation Circuit. For the monitor mode of operation only the port C connections are required. By proper connection to bits C0 and C1 the baud rate is selected. The monitor mode is selected by grounding bits C2 and C3. The serial input is the C4 bit and serial output is the C5 bit. The remaining ports may be connected as desired to evaluate the part.

The keyboard encoder routine translates a key-matrix configuration to ASCII characters. The key-matrix configuration is shown in Figure 22 and is related to the proper port I/O connections. The output mode may be selected to have both a serial format with output on the C5 bit and a parallel format using port B as output, or a parallel output format using port B only.

The encoder program features two-key-lockout for the control keys while simultaneously having 4-key rollover (minimum) for alphanumeric keys.

The port B parallel output functions as follows. The character is output to bits 0-6, then a negative strobe is transmitted to the host device via bit 7, followed by a 24 cycle pause, then a positive strobe is transmitted. The character will remain on the B port for at least five milliseconds following the positive strobe.

Note that part of the 8 × 16 matrix capability is shared (port C, bits 0-5) on this Demonstration ROM by the monitor program.

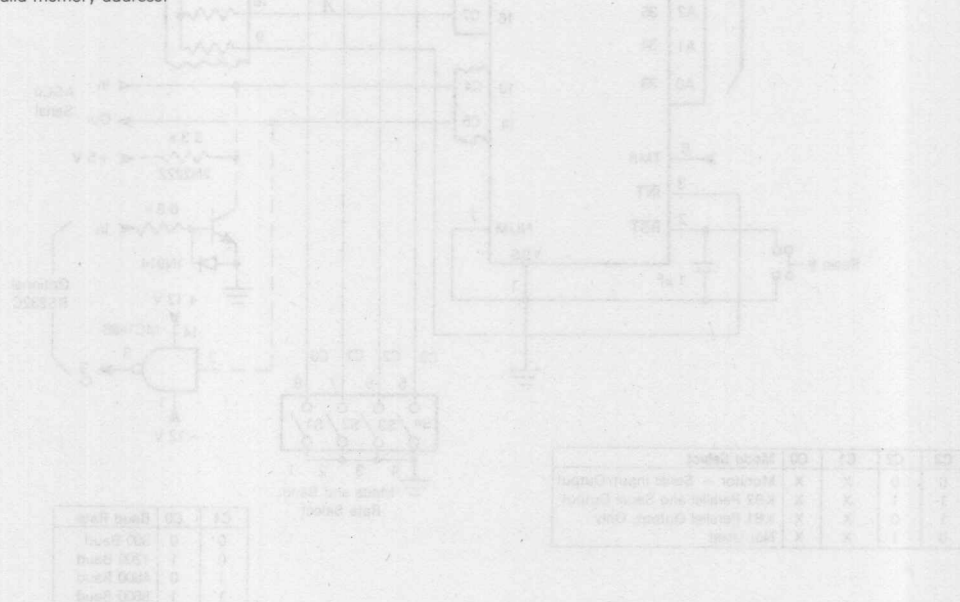


FIGURE 21 — MONITOR/KEYBOARD EVALUATION CIRCUIT

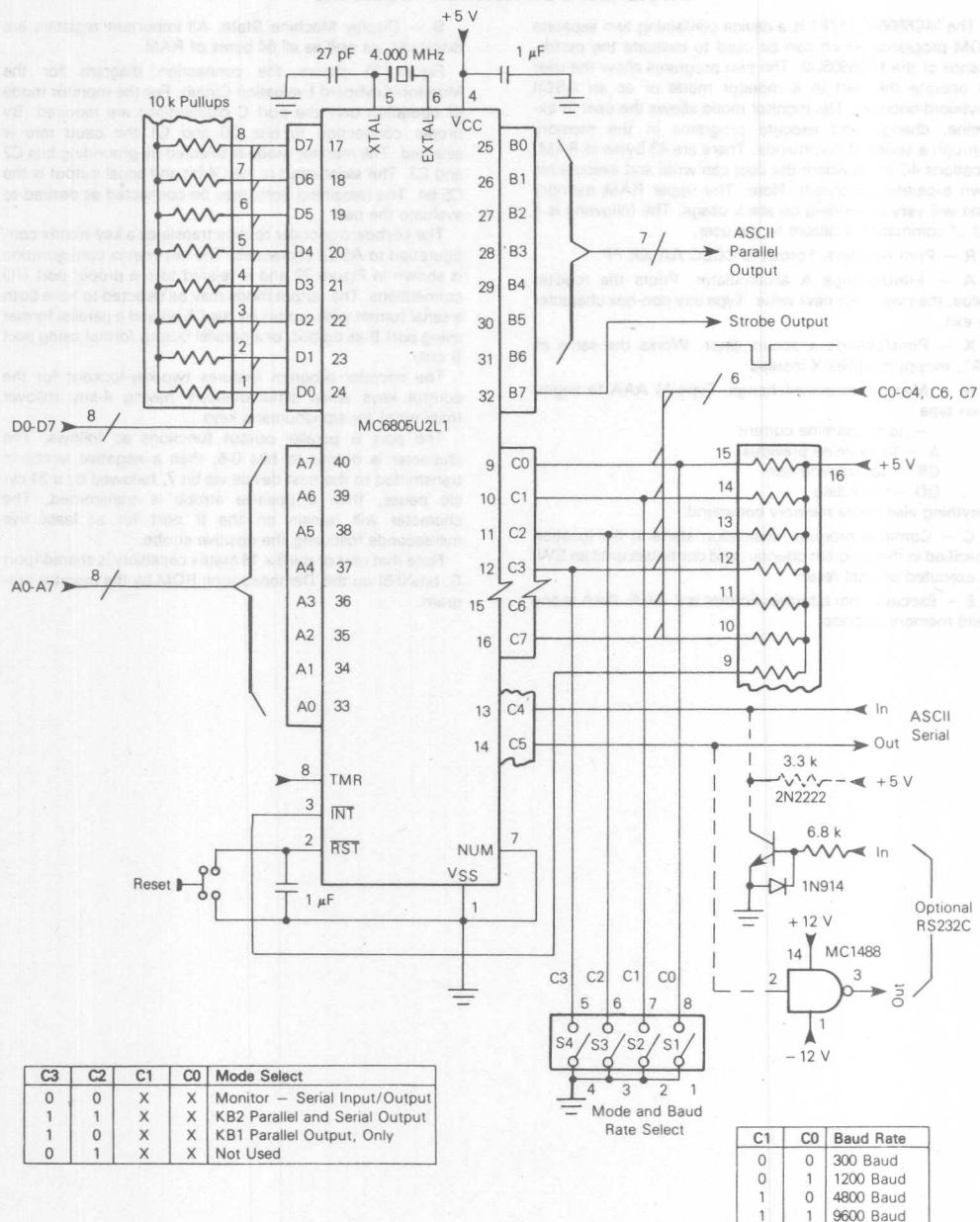
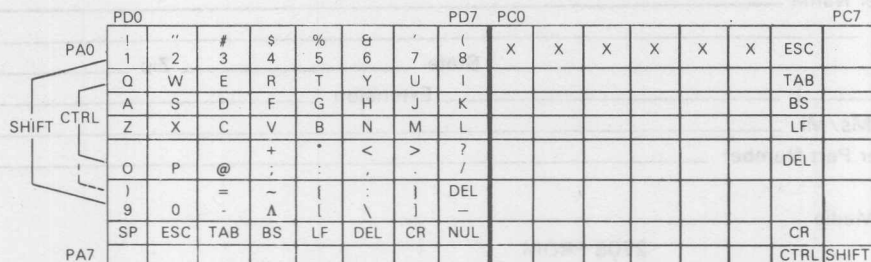


FIGURE 22 — TYPICAL IMPLEMENTATION ASCII PARALLEL OUTPUT, WITH STROBE, AND SERIAL OUTPUT
SELECTRONICS KEYBOARD (8x16 MATRIX, PARTIALLY-FILLED)



X: Specifically assigned for demonstration purposes.

ORDERING INFORMATION

The following information is required when ordering a custom MCU. This information may be transmitted to Motorola in any of the following media:

PROM(s)

MDOS disk file

To initiate a ROM pattern for the MCU, it is necessary to first contact your local field service office, local sales person or your local Motorola representative.

PROMs — The MCM2708 or MCM2716 type PROMs, programmed with the customer program (positive logic sense for address and data), may be clearly marked to indicate which PROM corresponds to which address space (\$000-\$FFF HEX). See Figure 23 for recommended marking procedure.

After PROM(s) are marked, they should be placed in conductive IC carriers and securely packed. DO NOT USE STYROFOAM.

MDOS DISKFILE — The diskette delivered to Motorola should be single sided, single density with a minimum of the operating system on disk and the users program on disk in the ".LX" format. All other information is extra. The user should indicate clearly the name of the program.

Option List

Select the options for your MCU from the following list. A manufacturing mask will be generated from this information.

ROM Mask

Timer Clock Source

Internal $\phi 2$ clock

TIMER input pin (8)

Timer Prescaler

 2^0 (divide by 1) 2^1 (divide by 2) 2^2 (divide by 4) 2^3 (divide by 8) 2^4 (divide by 16) 2^5 (divide by 32) 2^6 (divide by 64) 2^7 (divide by 12)

Internal Oscillator Input

Crystal

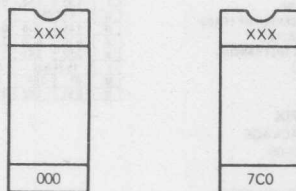
Resistor

Low Voltage Inhibit

Disable

Enable

FIGURE 23 — PROM MARKING



XXX = Customer ID

AD0244

Customer Name _____
 Address _____
 City _____ State _____ Zip _____
 Phone (____) _____ Extension _____
 Contact Ms/Mr _____
 Customer Part Number _____

Pattern Media

2708 PROM

2716 PROM

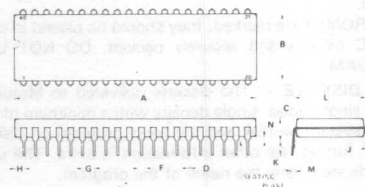
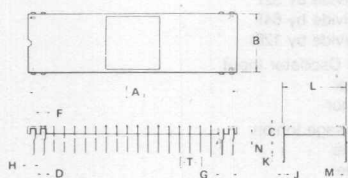
MDOS Disk File

(Note 2) _____

Notes: (2) Other media require prior factory approval.

Signature _____
 Title _____

OUTLINE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	3.05	4.32	0.120	0.170
D	0.38	0.53	0.015	0.021
E	0.76	1.40	0.030	0.055
F	254 BSC		0.100 BSC	
G	0.20	0.33	0.008	0.013
H	2.54	4.19	0.100	0.165
J	14.99	15.65	0.590	0.616
K	109		109	
L	1.02	1.52	0.040	0.060

NOTES

1. DIMENSION [A] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS

[B] 0.25 (0.010) [T] A [W]

3. [T] IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

L SUFFIX
 CERAMIC PACKAGE
 CASE 715-05

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.09	52.45	2.035	2.065
B	13.12	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	150°	0°	150°
N	0.51	1.02	0.020	0.040

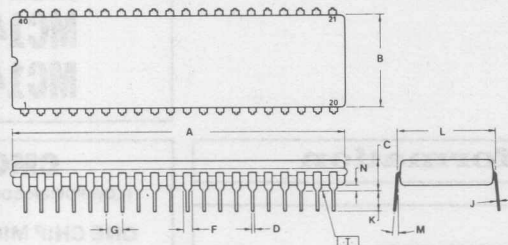
NOTES

1. POSITIONAL TOLERANCE OF LEADS (D) SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

P SUFFIX
 PLASTIC PACKAGE
 CASE 711-01

Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others.

MC6805U2



S SUFFIX
CERDIP PACKAGE
CASE 734-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:

1. DIMENSION A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
 $\pm 0.25 (0.010) \text{ (M)} \quad T \quad A \text{ (M)}$
3. [T] IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSION A AND B INCLUDES MENISCUS.

THE GROWING M6805 FAMILY

M6805 Family System Configuration And Programming Features

	MC6805P2	MC146805E2	MC6805R2	MC6805U2	MC146805G2	MC68705P3
Technology	HMOS	CMOS	HMOS	HMOS	CMOS	HMOS
Number of Pins	28	40	40	40	40	28
On-Chip RAM (Bytes)	64	112	64	64	112	112
On-Chip User ROM (Bytes)	1.1 k	None	2 k	2 k	2.2 k	1.8 k EPROM
Expansion Bus	None	Yes	None	None	None	None
Bidirectional I/O Lines	20	16	32	32	32	20
I/O Options	None	None	A/D Converter	None	None	None
Software Compatibility	Similar to M6800				Similar to M6800	
True Bit Manipulation	Yes	Yes	Yes	Yes	Yes	Yes
Instructions	59	61	59	59	61	59
Ten Addressing Modes	Yes	Yes	Yes	Yes	Yes	Yes

Advance Information

ONE CHIP MICROCOMPUTERS

The MC141000 family is a series of 4-bit CMOS Microcomputers designed for dedicated applications. The CMOS technology of the MC141000 family provides the flexibility of microcomputers, for battery-powered and battery-backed-up applications. The MC141000 and MC141200 include ROM, RAM, and I/O for self-contained configurations in 28 and 40-pin packages. The 48-pin MC141099 has RAM and I/O with provision for external program memory. The MC141099 serves lower-volume applications such as prototyping or pilot production of MC141000 and MC141200 systems.

FEATURES	MC141000	MC141200	MC141099
Package Pin Count	28 Pins	40 Pins	48 Pins
Instruction Read Only Memory	1024 x 8 (8,192 Bits)	None	None
Data Random Access Memory	64 x 4 (256 Bits)		
"R" Individually Addressed Outputs	11	16	16
"O" Parallel Latched Data Outputs	8 Bits	5 Bits	
"R" and "O" Output Drive	Source 20 mA		
Maximum-Rated Voltage	6.5 V		
Working Registers	Static 2-4 Bits Each		
Instruction Set	See Table 2		
External Address Lines	None		10
On-Chip Oscillator	Yes		
Maximum Power Dissipation	5 V, 600 kHz	11.5 mW	
	5 V, 100 kHz	2.8 mW	
	3 V, 200 kHz	1.5 mW	
	3 V, 30 kHz	0.36 mW	

APPLICATIONS

- Appliance Controllers
- Calculators
- Toys
- Radio Controllers
- Communications Controllers
- Data Terminals
- Cash Registers
- Heating/Air-Conditioning Controllers
- Remote Sensing System
- Printing Controllers
- Security Systems
- Power Systems Control
- Automotive Control

The above applications of the MC141000 family demonstrate its wide potential. Motorola accepts customer programs or will contract complete program development given the specifications for the application. Customer hardware and software support is available for developing programs and debugging systems. This consists of one board and a software package using the M6800 EXORciser. Contact your local sales office for details.

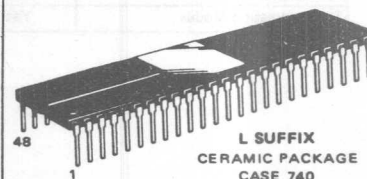
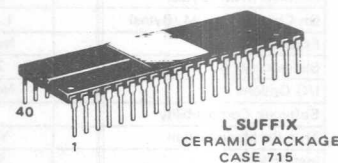
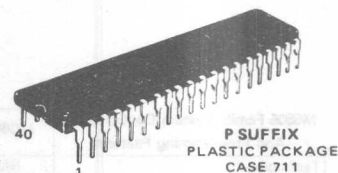
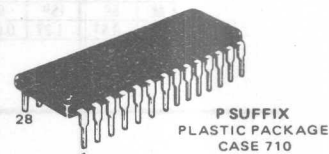
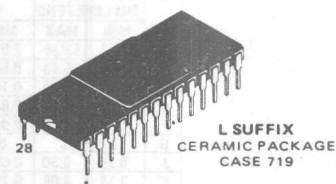
This is advance information and specifications are subject to change without notice.

MC14 1000
MC14 1200
MC14 1099

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

ONE CHIP MICROCOMPUTERS



ORDERING INFORMATION

MC14XXXX Suffix Denotes

└─ L Ceramic Package

└─ P Plastic Package

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.5	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
DC Current Drain per Pin, All Inputs	I	10	mA
DC Current Drain, V_{DD} Pin	I	250	mA
DC Current Drain, V_{SS} Pin	I	20	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Total Power Dissipation	P_D	See Figure 1	mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0$)

Parameter	Symbol	Value	Unit
DC Supply Voltage — High Speed Clock Full Range Operation	V_{DD}	+4.75 to +6.0 +3.0 to +6.0	Vdc
Clock Frequency — $V_{DD} = 5.0 \text{ Vdc} \pm 5\%$ $V_{DD} = 3.0 \text{ Vdc Min.}$	f_{Clk}	DC to 600 DC to 200	kHz

ELECTRICAL CHARACTERISTICS ($V_{DD} = +5.0 \text{ V}$, $V_{SS} \text{ Gnd}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — K Inputs and INIT ($V_{in} = 5.0 \text{ V}$) ($V_{in} = 0.0 \text{ V}$)	I_{in}	75 —	100 -0.00001	135 -0.3	μA
Input Current — I Inputs (MC141099 Only) ($V_{in} = 5.0 \text{ V}$) ($V_{in} = 0.0 \text{ V}$)	I_{in}	— —	0.00001 -0.00001	0.3 -0.3	μA
Input Voltage — I Inputs (MC141099 Only)	V_{IL} V_{IH}	— 2.0	— —	0.8 —	Vdc
Input Voltage — Other Inputs	V_{IL} V_{IH}	— 3.5	— —	1.5 —	Vdc
Output Drive — R and O Outputs ($V_{OH} = 2.4 \text{ V}$) — See Figure 2 ($V_{OL} = 0.4 \text{ V}$, $T_A = 85^\circ\text{C}$, $V_{DD} = 4.75 \text{ V}$)	I_{OH} I_{OL}	-20 1.6	— —	— —	mA
Output Drive — PA and PC Outputs (MC141099 Only) ($V_{OH} = 4.6 \text{ V}$) ($T_A = 85^\circ\text{C}$, $V_{DD} = 4.75 \text{ V}$) ($V_{OL} = 0.4 \text{ V}$)	I_{OH} I_{OL}	-100 100	— —	— —	μA
Average Supply Current	I_{DD}	—	—	See Figure 3	μA
Static Supply Current ($V_{DD} = 6.0 \text{ V}$)	I_{DD}	—	60	300	μA
Oscillator Frequency ($V_{DD} = 4.75 \text{ V}$)	f_{Clk}	No Limit	—	600	kHz
Internal Oscillator Frequency for $R_{ext} = 30 \text{ k}\Omega$	f_{Clk}	400	500	600	kHz
Input Capacitance — K Inputs and INIT	C_{in}	—	—	7.5	pF
Input Capacitance — Clock Input	C_{io}	—	—	30	pF

MC141000, MC141200, MC141099

FIGURE 1 – TOTAL POWER DISSIPATION

Care must be taken to ensure that the maximum power dissipation of the package is not exceeded.

$$T_{stg} = T_A + (P_D)(\theta_{JA})$$

where T_{stg} is maximum storage temperature (150°C)

T_A is ambient operating temperature

P_D is total power dissipation:

$$P_D = (I_{DD})(V_{DD}) + (I_{OH})(V_{DD} - V_{OH}) + (I_{OL})(V_{OL} - V_{SS})$$

(I_{OH} and I_{OL} are the sum of all output pins)

	θ_{JA} Value	
	Ceramic	Plastic
28-Pin Package	58	98
40-Pin Package	50	95
48-Pin Package	50	—

FIGURE 2 – MINIMUM OUTPUT SOURCE CURRENT
versus OUTPUT VOLTAGE (R and O Outputs)

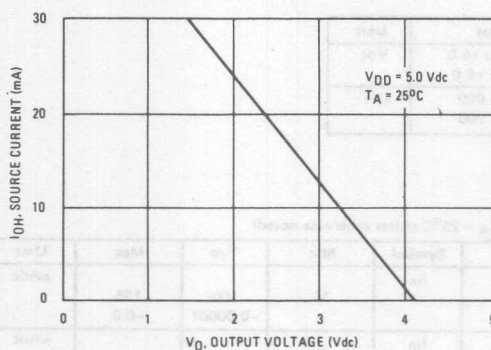
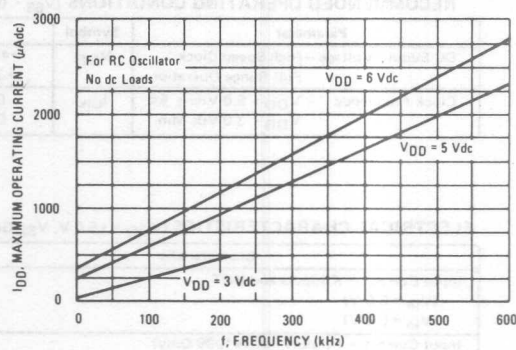


FIGURE 3 – MAXIMUM OPERATING CURRENT
versus OSCILLATOR FREQUENCY



PIN ASSIGNMENTS

MC141000

R8	1	28	R7
R9	2	27	R6
R10	3	26	R5
Neg Supply, V_{SS}	4	25	R4
K1	5	24	R3
K2	6	23	R2
K4	7	22	R1
K8	8	21	R0
INIT	9	20	Pos Supply, V_{DD}
O7	10	19	OSC2
O6	11	18	OSC1
O5	12	17	O0
O4	13	16	O1
O3	14	15	O2

MC14 1200

R8	1	40	R7
R9	2	39	R6
R10	3	38	R5
R11	4	37	R4
R12	5	36	R3
Neg Supply, V_{SS}	6	35	R15
K1	7	34	R14
K2	8	33	R13
K4	9	32	NC
K8	10	31	R2
INIT	11	30	R1
O7	12	29	R0
NC	13	28	Pos Supply, V_{DD}
NC	14	27	OSC2
NC	15	26	OSC1
O6	16	25	O0
O5	17	24	O1
O4	18	23	O2
O3	19	22	NC
NC	20	21	NC

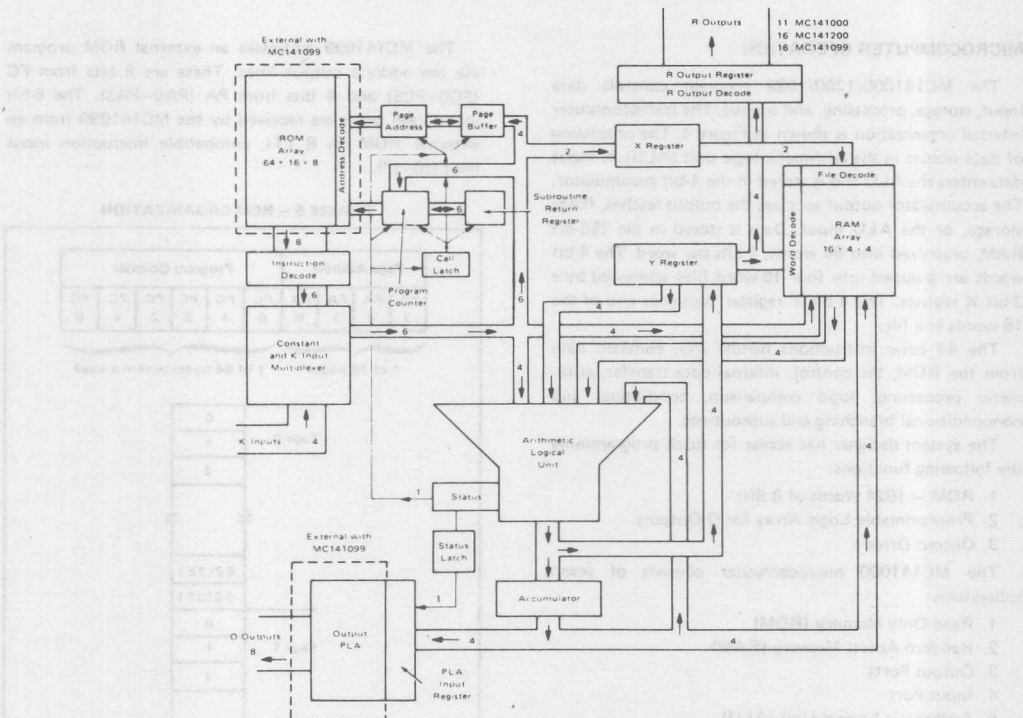
MC141099

R8	1	48	R7
R9	2	47	R6
R10	3	46	R5
R11	4	45	R4
R12	5	44	R3
Neg Supply, V_{SS}	6	43	R15
K1	7	42	R14
K2	8	41	R13
K4	9	40	R2
K8	10	39	R1
INIT	11	38	R0
(LSB) PC0	12	37	Pos Supply, V_{DD}
PC1	13	36	OSC2
PC2	14	35	OSC1
PC3	15	34	OSL
PC4	16	33	O8
PC5	17	32	O4
PA0	18	31	O2
PA1	19	30	O1
PA2	20	29	O0
(MSB) PA3	21	28	I1
Instruction Input	17	22	I2
	16	23	I3
	23	26	I4
	15	24	I5

ROM Address Out

Instruction Input

FIGURE 4 – FUNCTIONAL BLOCK DIAGRAM – MC141000/MC141200/MC141099



The block diagram above shows the resources available to the MC141000/1200/1099 programmer. They are:

A	The accumulator is used to store the result of an ALU operation for subsequent operations.
ALU	The arithmetic logical unit performs calculation and decision-making tasks.
K Inputs	The K lines are the data input port. Since there are only four input lines, they are usually multiplexed under control of the R lines. The inputs are diode protected and have a pull-down resistor of approximately 50 k Ω ; therefore, open inputs are read as a logic low.
O Outputs	The eight outputs of the PLA are connected to output drivers which comprise the O outputs. These output drivers may be manufactured as open emitter, active sink, or push-pull at the user's option.
PLA	The output programmable logic array is user-defined to specify the state of each of the eight O outputs for each of the 32 possible PLAIR outputs.
PLAIR	The programmable logic array input register is a 5-bit latch which latches the four accumulator bits and the output of the status latch.
RAM	Variable data is stored in the 64-word, 4-bit per word Random Access Memory. Data is accessed by decoding a 2-bit file address (X register) and 4-bit word address (Y register).

ROM Array	The user's instructions are mask programmed into the Read Only Memory (ROM). Instructions are addressed by a page address register (PA) and program counter (PC). A single subroutine return register (SRR) and page buffer register (PB) permit a subroutine call to any location within the ROM.
R Outputs	The output of the Y register is decoded to select one of the R-output lines which can then be set or reset under program control. The R lines are used as control lines to scan keyboards and displays, perform handshakes, and interface external logic. The R outputs may be manufactured as open emitter, active sink, or push-pull at the user's option.
S	All branches and subroutine calls are dependent on the state of status logic. It may be set or reset on logical or arithmetic operations and is set by the remainder of the instructions.
SL	The status latch stores the state of the status logic in order to preserve it for subsequent O output operations. NOTE: S and SL are NOT identical.
Y Register	The Y register is a multipurpose register used to address a word in a RAM file, to select an R output for manipulation by subsequent instructions, or as a general-purpose counting and storage register.

MICROCOMPUTER OPERATION

The MC141000/1200/1099 program controls data input, storage, processing, and output. The microcomputer internal organization is shown in Figure 4. The processing of data occurs in the arithmetic logic unit (ALU). K-input data enters the ALU and is stored in the 4-bit accumulator. The accumulator output accesses the output latches, RAM storage, or the ALU input. Data is stored in the 256-bit RAM, organized into 64 words, 4 bits per word. The 4-bit words are grouped into four 16-word files addressed by a 2-bit X register. The 4-bit Y register addresses one of the 16 words in a file.

The 43 basic instructions handle I/O, constant data from the ROM, bit control, internal data transfer, arithmetic processing, logic comparison, conditional and unconditional branching and subroutines.

The system designer has access for mask programming the following functions:

1. ROM — 1024 Words of 8 Bits
2. Programmable Logic Array for O Outputs
3. Output Drivers

The MC141000 microcomputer consists of seven subsystems:

1. Read Only Memory (ROM)
2. Random Access Memory (RAM)
3. Output Ports
4. Input Port
5. Arithmetic Logical Unit (ALU)
6. The Instruction Decoder
7. Clock

The following paragraphs describe how each of these subsystems is controlled by the instruction set. Every instruction occupies a single memory byte and is executed in one instruction cycle (six clock cycles).

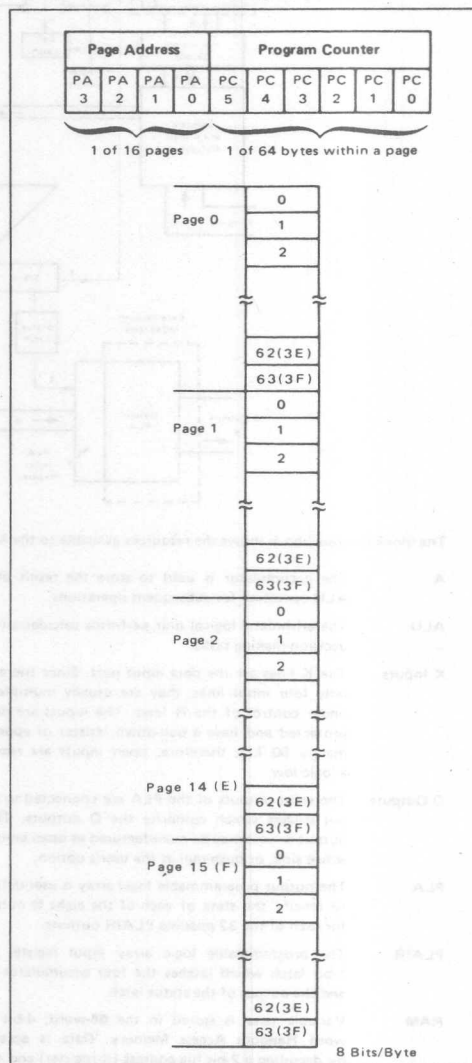
ROM ARRAY

The ROM in the MC141000/1200 consists of 8192 bits of mask-programmed memory organized as 1024 8-bit instructions. It is divided into 16 pages of 64 instructions per page. See Figure 5.

Instructions within ROM are addressed by the page address register (PA) which contains the page number, and the program counter (PC) which contains the location of the instruction relative to the beginning of the page. The PC is incremented prior to fetching the next instruction (unless diverted by a BRANCH or CALL) so each instruction is accessed in the numerical order of its address. A carry from the PC is not added to the PA so the program "wraps around" within the page rather than executing the first instruction of the following page. Upon power up, the PC is set to zero and the PA and PB are set to 15.

The MC141099 addresses an external ROM program via ten address output lines. These are 6 bits from PC (PC0-PC5) and 4 bits from PA (PA0-PA3). The 8-bit instruction bytes are received by the MC141099 from an external ROM on 8 TTL compatible instruction input lines (I0-I7).

FIGURE 5 — ROM ORGANIZATION

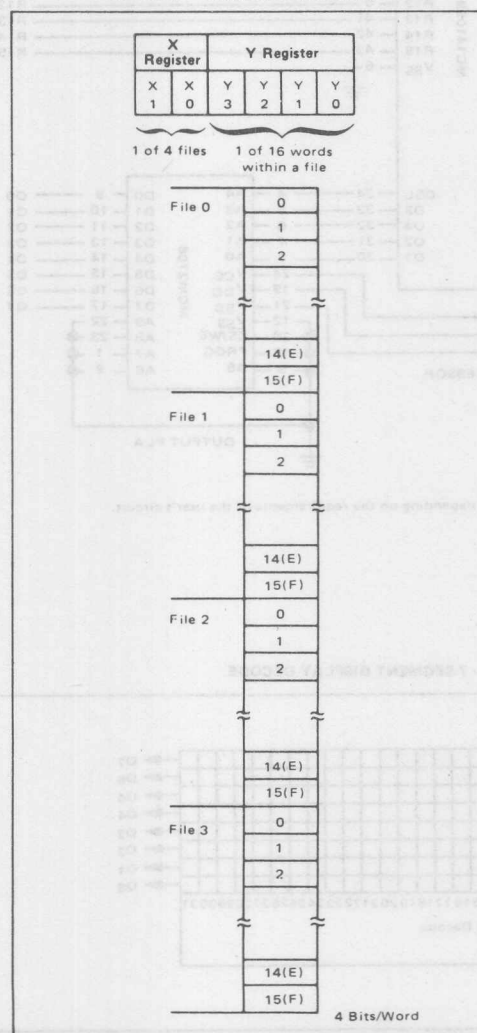


RANDOM ACCESS MEMORY – RAM

RAM consists of 256 bits organized into 64 4-bit words. For purposes of addressing, the 4-bit words are organized into four files of 16 4-bit words per file, Figure 6.

The X register is decoded to select 1 of the 4 RAM files; and the Y register is decoded to address 1 of the 16 words in the selected file.

Individual bits within the RAM can be set, reset and tested under program control.

FIGURE 6 – RAM ORGANIZATION**OUTPUT PORTS**

Two output ports (R and O) are included in the micro-computer. The MC141000 has eleven R outputs and the MC141200 and MC141099 each have sixteen R outputs. The MC141000 and MC141200 each have eight O outputs, while the MC141099 has five. The number of R outputs is the only difference between the MC141000 and the MC141200.

R-output lines are used primarily as control or "handshake" lines, and to multiplex external hardware. The R output which is to be operated on is selected by a binary decode of the contents of the Y register. Set R and reset R instructions change the state of one R output at a time.

The eight O-output lines on the MC141000 and MC141200 are the decoded outputs of the contents of the 5-bit PLAIR. Since the PLAIR is loaded from the A and the SL, these registers must be "set up" prior to an output operation. The status latch can only be loaded by the YNEA (Y register not equal to accumulator) instruction while the contents of the accumulator may be modified by numerous other instructions. The MC141099 brings out the 5-bit PLAIR to allow external decoding. An external PROM/EPROM could be used to simulate the PLA. Figure 7 shows how EPROMs may be used with MC141099 to emulate an MC14100 or an MC141200.

In a typical application, the first four R lines might be used as digit selects for outputting a four-digit decimal number using the PLA programmed as a seven-segment decode as shown in Figure 8.

The MC141000/1200 outputs may be mask programmed in any of three configurations. Figure 9 shows the open emitter circuit capable of sourcing 20 mA at $V_O = 2.4$ V and $V_{DD} = 5.0$ V, which will drive an LED. Figure 10 is the open drain circuit capable of sinking 1.6 mA over temperature, which will drive one TTL load or four LSTTL loads. The source and sink devices are combined in the active push-pull circuit of Figure 11. The MC141099 also has outputs as in Figure 11.

INPUTS

The input lines consist of the four K-input lines and the initialize (INIT) line. All inputs are static-protected CMOS inputs with pulldown of about 50 k Ω . Thus, an open input is equivalent to logic 0. The circuit is shown in Figure 12.

When power is applied, the registers shown in Table 1 are loaded as shown for power up. All other internal registers and RAM come up in an arbitrary state.

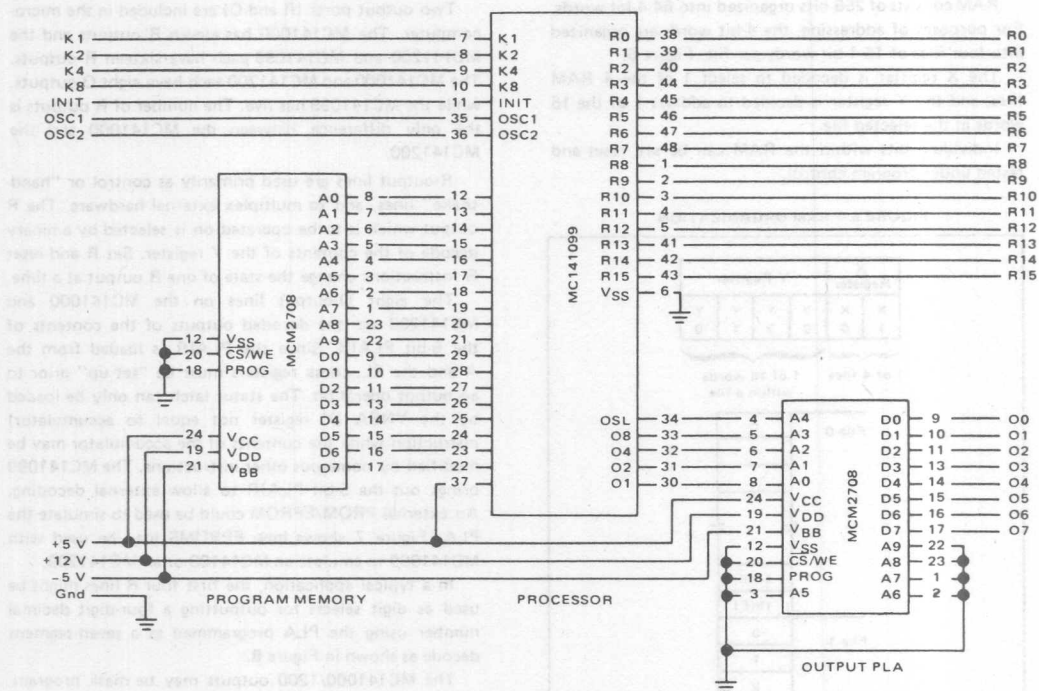
After power is applied, the initialize (INIT) input may be used to reinitialize the processor. Internally, INIT has

TABLE 1 – POWER UP AND INITIALIZE CONDITIONS

	PC	PA	PB	CL	PLAIR	R Outputs
Power Up	0	F16	F16	0	0	0
Initialize	0	\bar{K}	\bar{K}	0	0	0

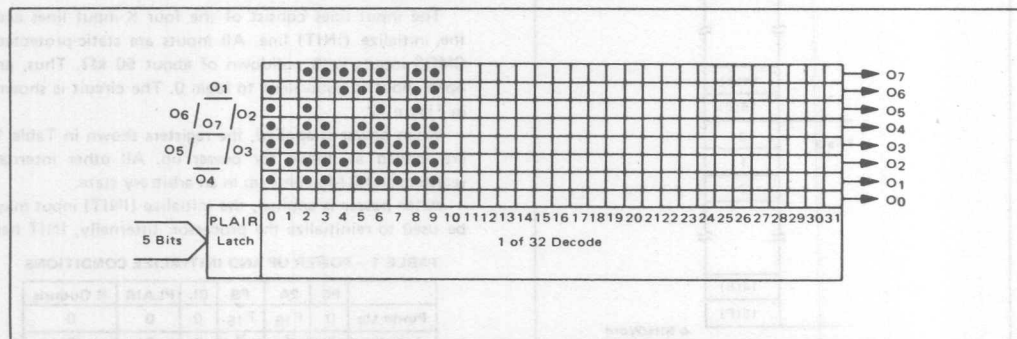
MC141000, MC141200, MC141099

FIGURE 7 – USING THE MC141099 TO EMULATE MC141000/MC141200 IN REAL-TIME



NOTE: The OPLA EPROM outputs may require buffers depending on the requirements of the user's circuit. The EPROM outputs are TTL compatible.

FIGURE 8 – OUTPUT PLA EXAMPLE – 7-SEGMENT DISPLAY DECODE



a 50 k Ω pull-down resistor which holds the INIT line low. It must be held high for a minimum of 6 full clock cycles and then returned to the low state. If a mechanical switch or other mechanical device is used to control INIT, it may be necessary to include a method of contact debounce to ensure a valid INIT pulse.

A valid INIT pulse causes the registers to be initialized as shown in the table. The contents of registers other than those shown remain unchanged during initialize. Note that the PA and PB are loaded with the 1's complement of the K-input lines (K8 = MSB). This feature allows the MC141000 to be initialized to the first instruction on any page by controlling the K inputs. This is useful where the same circuit may be used for several applications. Since the K inputs have 50 k Ω pull-down resistors, open inputs are a 0 (unless driven from another device) and the 1's complement (F16) is loaded into PA and PB.

ARITHMETIC LOGICAL UNIT (ALU)

The ALU is the calculating and decision-making portion of the MC141000/1200/1099 hardware and

consists of a 4-bit adder/comparator and the status logic.

The adder/comparator can add, subtract, compare two numbers, add +1, -1, 6, 8, and 10.

The status logic is selectively set or reset by add, subtract, increment, decrement, compare and bit-test operations. Other instructions always set the status logic to a 1.

INSTRUCTION DECODE

The instruction decode logic latches every instruction fetched from ROM and configures the internal logic to execute the current instruction. The instruction set is listed in Table 2.

CLOCK

The internal oscillator circuit operates with quartz crystals, ceramic resonators, an external resistor and from an external clock source. These oscillator circuit connections are shown in Figures 13, 14, and 15. Figure 16 shows the typical oscillation frequency with an external resistor. The discrete component values used with the quartz crystal and ceramic resonator oscillators may vary depending upon crystal/resonator manufacturer.

FIGURE 9 – OPEN EMITTER OUTPUT CIRCUIT

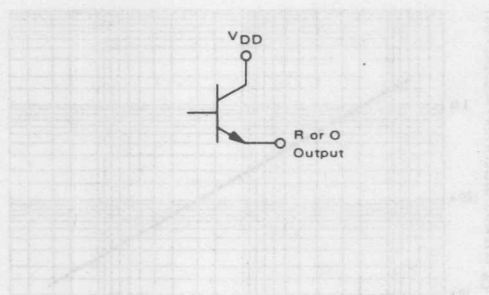


FIGURE 11 – ACTIVE PUSH-PULL OUTPUT CIRCUIT

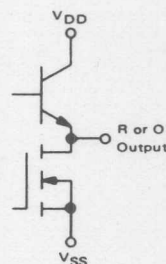


FIGURE 10 – OPEN DRAIN OUTPUT CIRCUIT

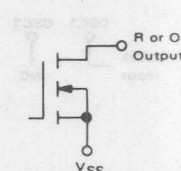


FIGURE 12 – INPUT CIRCUIT WITH PULLDOWN AND STATIC PROTECTION

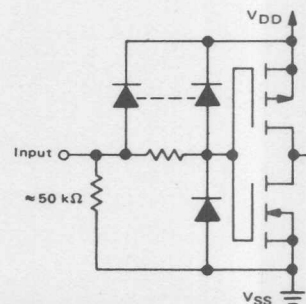
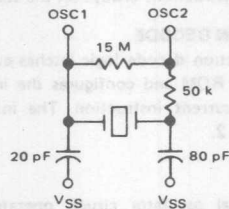


FIGURE 13 – EXTERNAL COMPONENTS FOR QUARTZ CRYSTAL OR CERAMIC RESONATOR OSCILLATOR



Component values typical for 500 kHz crystal.

FIGURE 15 – EXTERNAL CLOCK SOURCE INPUT

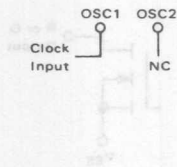


FIGURE 14 – OSCILLATOR CIRCUIT WITH ONE EXTERNAL RESISTOR

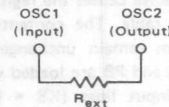
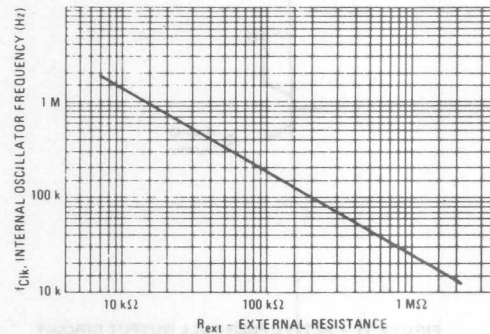


FIGURE 16 – TYPICAL OSCILLATOR FREQUENCY versus EXTERNAL RESISTANCE



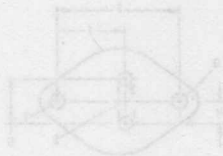
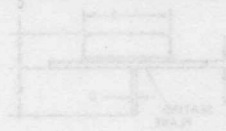
MC141000, MC141200, MC141099

TABLE 2 - MC141000/1200/1099 INSTRUCTION SET

Opcode	Mnemonic	Description
0111 (C)	ALEC	If accumulator is less than or equal to I(C) field, status = 1.
00101001	ALEM	If accumulator is less than or equal to M(X,Y), status = 1.
00100101	AMAAAC	Add memory to accumulator. Accumulator = result, status = carry.
00000110	A6AAC	Add 6 to accumulator. Accumulator = result, status = carry.
00000001	A8AAC	Add 8 to accumulator. Accumulator = result, status = carry.
00000101	A10AAC	Add 10 to accumulator. Accumulator = result, status = carry.
10 (W)	BR	Branch to label if status = 1.
11 (W)	CALL	Call subroutine if status = 1.
00101111	CLA	Clear contents of accumulator.
00001011	CLO	Clear PLA Input Register.
00000000	COMX	Complement X-Register.
00101101	CPAIZ	Complement accumulator, then add 1. If accumulator = 0, status = 1.
00000111	DAN	Decrement accumulator. If no borrow, status = 1.
00101010	DMAN	Load M(X, Y) into accumulator and decrement. If no borrow, status = 1.
00101100	DYN	Decrement Y-register. If no borrow, status = 1.
00001110	IA	Increment accumulator.
00101000	IMAC	Load M(X, Y) into accumulator and increment. Status = carry.
00101011	IYC	Increment Y-Register. Status = carry.
00001001	KNEZ	If K-inputs not equal to zero, status = 1.
0001 (C)	LDP	Load page buffer with I(C) field.
001111 (B)	LDX	Load X-register with I(B) field.
00100110	MNEZ	If M(X, Y) not equal to zero, status = 1.
001101 (B)	RBIT	Reset bit I(B) of M(X,Y).
00001111	RETN	Return from subroutine.
00001100	RSTR	Reset R-line specified by Y-register.
00100111	SAMAN	Subtract accumulator from memory. Accumulator = result. If no borrow, status = 1.
001100 (B)	SBIT	Set Bit I(B) of M(X,Y).
00001101	SETR	Set R-line specified by Y-register.
00000011	TAM	Transfer accumulator contents to M(X,Y).
00100000	TAMİY	Transfer accumulator contents to M(X,Y), increment Y-register.
00000100	TAMZA	Transfer accumulator contents to M(X,Y), zero accumulator.
00100100	TAY	Transfer accumulator contents to Y-register.
001110 (B)	TBIT1	If bit I(B) of M(X,Y) is one, status = 1.
0100 (C)	TCY	Transfer I(C) field to Y-register.
0110 (C)	TCMIY	Transfer I(C) field to M(X,Y), increment Y-register.
00001010	TDO	Transfer status latch and accumulator to PLA input register.
00001000	TKA	Transfer K-inputs to accumulator.
00100001	TMA	Transfer M(X,Y) to accumulator.
00100010	TMY	Transfer M(X,Y) to Y-register.
00100011	TYA	Transfer Y-register contents to accumulator.
00101110	XMA	Exchange contents of M(X,Y) and accumulator.
00000010	YNEA	If Y-register is not equal to accumulator, status and status latch = 1.
0101 (C)	YNEC	If Y-register is not equal to I(C) field, status = 1.

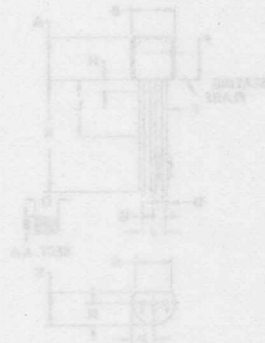
SECTION 7 PACKAGE INFORMATION

ITEM	QTY	DESCRIPTION	UNIT
1	1	TRANSISTOR	EA
2	1	TRANSISTOR	EA
3	1	TRANSISTOR	EA
4	1	TRANSISTOR	EA
5	1	TRANSISTOR	EA
6	1	TRANSISTOR	EA
7	1	TRANSISTOR	EA
8	1	TRANSISTOR	EA
9	1	TRANSISTOR	EA
10	1	TRANSISTOR	EA
11	1	TRANSISTOR	EA
12	1	TRANSISTOR	EA
13	1	TRANSISTOR	EA
14	1	TRANSISTOR	EA
15	1	TRANSISTOR	EA
16	1	TRANSISTOR	EA
17	1	TRANSISTOR	EA
18	1	TRANSISTOR	EA
19	1	TRANSISTOR	EA
20	1	TRANSISTOR	EA



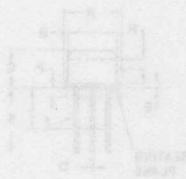
CASE 18 (TO-18)
Plastic Transistor
PDA = 180°C CW

ITEM	QTY	DESCRIPTION	UNIT
1	1	TRANSISTOR	EA
2	1	TRANSISTOR	EA
3	1	TRANSISTOR	EA
4	1	TRANSISTOR	EA
5	1	TRANSISTOR	EA
6	1	TRANSISTOR	EA
7	1	TRANSISTOR	EA
8	1	TRANSISTOR	EA
9	1	TRANSISTOR	EA
10	1	TRANSISTOR	EA
11	1	TRANSISTOR	EA
12	1	TRANSISTOR	EA
13	1	TRANSISTOR	EA
14	1	TRANSISTOR	EA
15	1	TRANSISTOR	EA
16	1	TRANSISTOR	EA
17	1	TRANSISTOR	EA
18	1	TRANSISTOR	EA
19	1	TRANSISTOR	EA
20	1	TRANSISTOR	EA



CASE 18 (TO-18)
Plastic Transistor
PDA = 180°C CW

ITEM	QTY	DESCRIPTION	UNIT
1	1	TRANSISTOR	EA
2	1	TRANSISTOR	EA
3	1	TRANSISTOR	EA
4	1	TRANSISTOR	EA
5	1	TRANSISTOR	EA
6	1	TRANSISTOR	EA
7	1	TRANSISTOR	EA
8	1	TRANSISTOR	EA
9	1	TRANSISTOR	EA
10	1	TRANSISTOR	EA
11	1	TRANSISTOR	EA
12	1	TRANSISTOR	EA
13	1	TRANSISTOR	EA
14	1	TRANSISTOR	EA
15	1	TRANSISTOR	EA
16	1	TRANSISTOR	EA
17	1	TRANSISTOR	EA
18	1	TRANSISTOR	EA
19	1	TRANSISTOR	EA
20	1	TRANSISTOR	EA



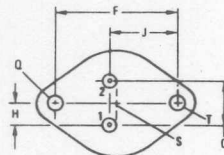
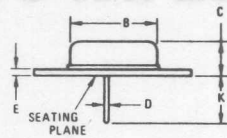
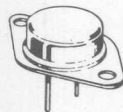
CASE 18 (TO-18)
Plastic Transistor
PDA = 180°C CW

CASE 1 (TO-3)

Metal Package

$R_{\theta JA} = 45^{\circ} \text{ C/W (Typ)}$

$R_{\theta JC} = 5.5^{\circ} \text{ C/W (Typ)}$

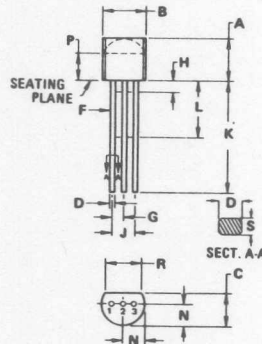


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	—	22.25	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188

CASE 29 (TO-92)

Plastic Transistor

$R_{\theta JA} = 200^{\circ} \text{ C/W}$

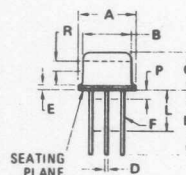
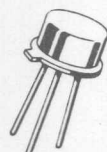


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.54	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.92	0.080	0.115
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

CASE 79 (TO-39)

Metal Package

$R_{\theta JA} = 185^{\circ} \text{ C/W (Typ)}$

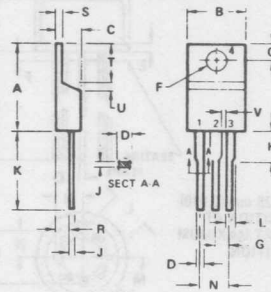
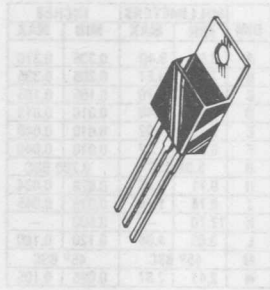


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.02	9.30	0.355	0.366
B	8.00	8.51	0.315	0.335
C	4.19	4.57	0.165	0.180
D	0.43	0.53	0.017	0.021
E	0.43	0.89	0.017	0.035
F	0.41	0.48	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.71	0.86	0.028	0.034
J	0.74	1.02	0.029	0.040
K	12.70	—	0.500	—
M	45° NOM	—	45° NOM	—
N	2.54 TYP	—	0.100 TYP	—
Q	90° NOM	—	90° NOM	—

CASE 221A (TO-220 Type)

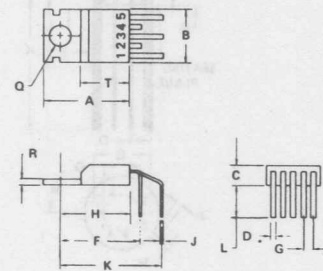
Plastic Power

$R_{\theta JA} = 65^{\circ} \text{ C/W (Typ)}$



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

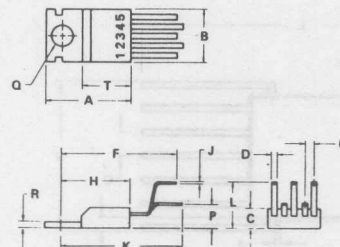
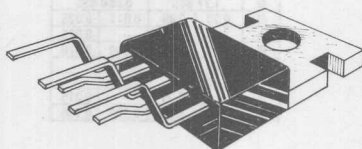
CASE 314A/B (TDA2002)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.49	15.88	0.610	0.625
B	9.91	10.41	0.390	0.410
C	4.32	4.57	0.170	0.180
D	0.71	0.81	0.028	0.032
F	14.48	14.86	0.570	0.585
G	1.45	1.96	0.057	0.077
H	12.70	13.69	0.500	0.539
J	0.38	0.64	0.015	0.025
K	18.54	18.92	0.730	0.745
L	5.33	6.60	0.210	0.260
Q	3.53	3.73	0.139	0.147
R	0.89	1.40	0.035	0.055
T	9.02	9.40	0.355	0.370

H SUFFIX
PLASTIC PACKAGE
CASE 314A

CASE 314A/B (TDA2002)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.49	15.88	0.610	0.625
B	9.91	10.41	0.390	0.410
C	4.32	4.57	0.170	0.180
D	0.71	0.81	0.028	0.032
F	20.83	21.59	0.820	0.850
G	1.45	1.96	0.057	0.077
H	12.70	13.69	0.500	0.539
J	0.38	0.64	0.015	0.025
K	21.46	23.50	0.845	0.925
L	8.00	8.38	0.315	0.330
P	4.32	4.70	0.170	0.185
Q	3.53	3.73	0.139	0.147
R	0.89	1.40	0.035	0.055
T	9.02	9.40	0.355	0.370

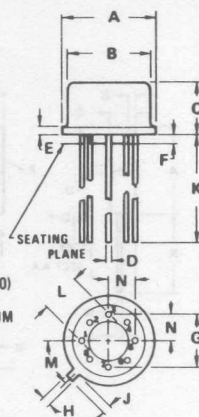
V SUFFIX
PLASTIC PACKAGE
CASE 314B

CASE 601

Metal Package



NOTE:
1. LEADS WITHIN 0.25 mm (0.010)
DIA OF TRUE POSITION AT
SEATING PLANE AT MAXIMUM
MATERIAL CONDITION.

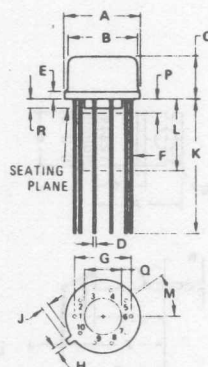


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.48	0.016	0.019
E	0.25	1.02	0.010	0.040
F	0.25	1.02	0.010	0.040
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
L	3.05	4.06	0.120	0.160
M	45° BSC		45° BSC	
N	2.41	2.67	0.095	0.105

CASE 603

Metal Can

$R_{\theta JA} = 160^{\circ} \text{C/W}$



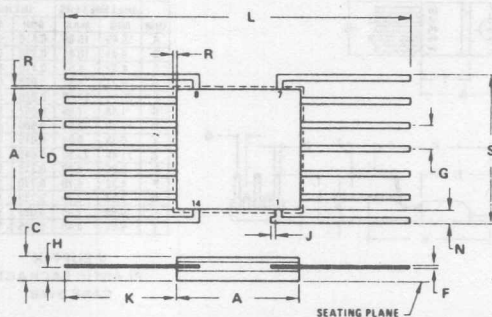
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.407	0.533	0.016	0.021
E	—	1.02	—	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	—	1.27	—	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

Case 603B has tab at pin1.

CASE 607 (TO-86 Type)

Ceramic Package

$R_{\theta JA} = 165^{\circ} \text{C/W(Typ)}$



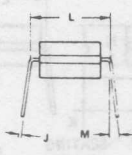
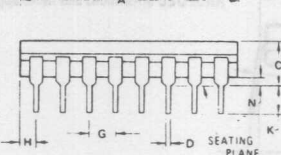
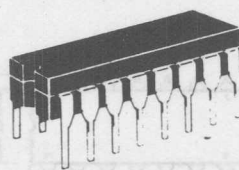
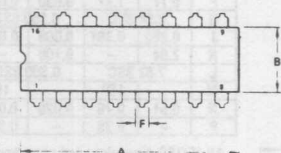
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
C	0.76	1.78	0.030	0.070
D	0.33	0.48	0.013	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.30	0.89	0.012	0.035
J	—	0.38	—	0.015
K	6.35	9.40	0.250	0.370
L	18.80	—	0.740	—
M	0.25	—	0.010	—
R	—	0.38	—	0.015
S	7.62	8.38	0.300	0.330



CASE 620

Ceramic Package

$R_{\theta JA} = 100^{\circ} \text{C/W(Typ)}$



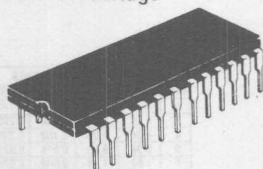
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	15°		15°	
N	0.51	1.02	0.020	0.040

NOTES

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
- PKG INDEX NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

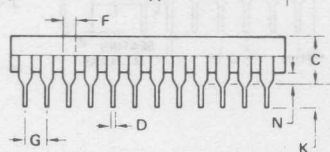
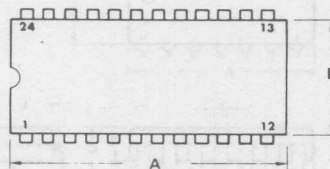
CASE 623

Ceramic Package



NOTES:

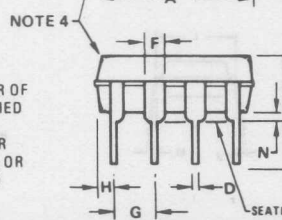
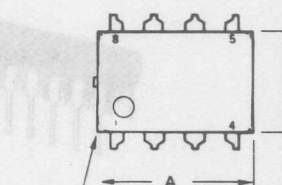
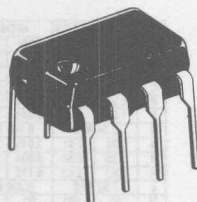
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

CASE 620

Plastic Package

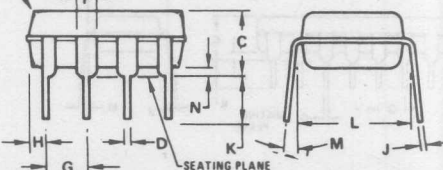


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	10°		10°	
N	0.51	0.76	0.020	0.030

NOTES:

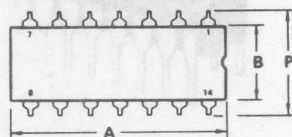
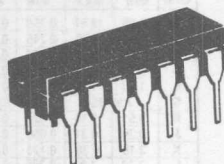
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)

NOTE 4



CASE 632

Ceramic Package

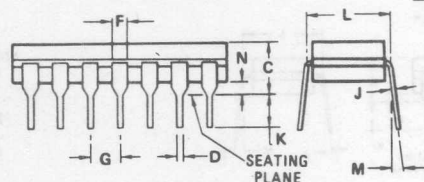


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	—	5.08	—	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	—	0.100	—
L	7.62 BSC		0.300 BSC	
M	—	15°	—	15°
N	0.51	0.76	0.020	0.030
P	—	8.25	—	0.325

All JEDEC dimensions and notes apply.

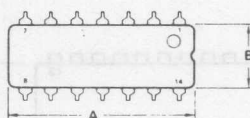
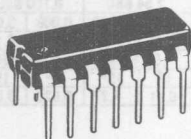
NOTES:

1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.



CASE 646

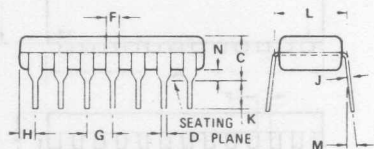
Plastic Package
 $R_{\theta JA} = 100^{\circ} \text{C/W(Typ)}$



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.15	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

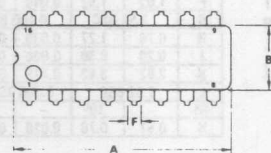
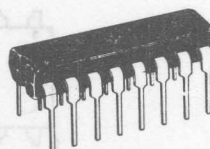
NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

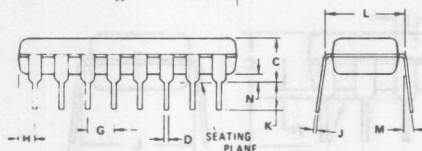


CASE 648

Plastic Package
 $R_{\theta JA} = 100^{\circ} \text{C/W(Typ)}$



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040



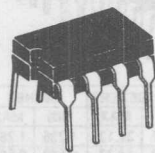
NOTE

1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 693

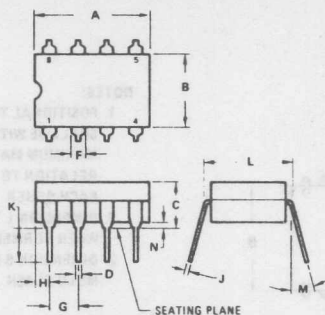
Ceramic Package

$R\theta_{JA} = 100^{\circ} \text{ C/W(Typ)}$



NOTES

1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

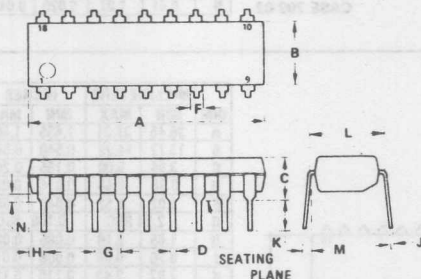
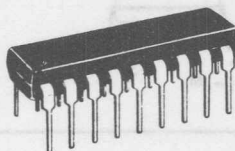


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.06	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	15°		15°	
N	0.51	1.02	0.020	0.040

CASE 701

Plastic Package

$R\theta_{JA} = 100^{\circ} \text{ C/W(Typ)}$



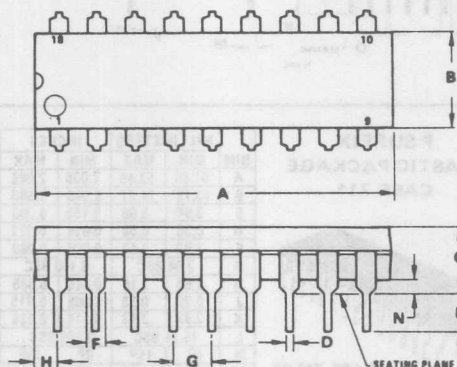
NOTES

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

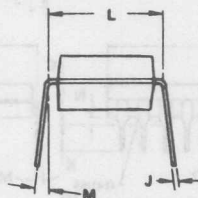
CASE 707

P SUFFIX
PLASTIC PACKAGE



NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



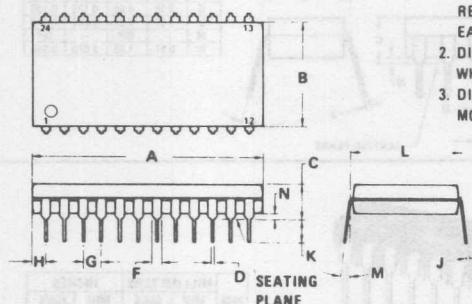
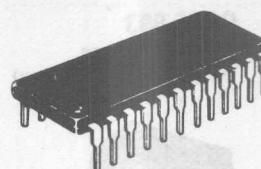
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62	8.30	0.300	0.330
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 707-02

**P SUFFIX
PLASTIC PACKAGE
CASE 709**

NOTES:

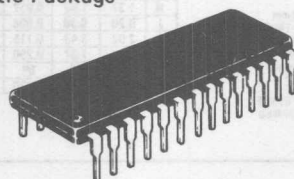
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.78	2.03	0.070	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24	BSC	0.600	BSC
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

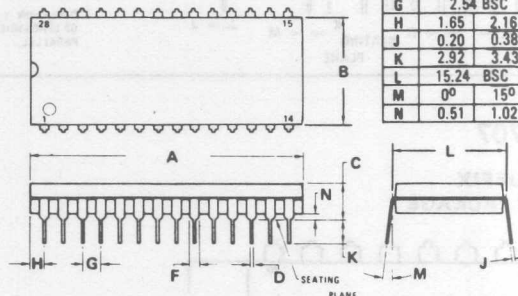
CASE 709-02

**CASE 710-02
Plastic Package**



NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

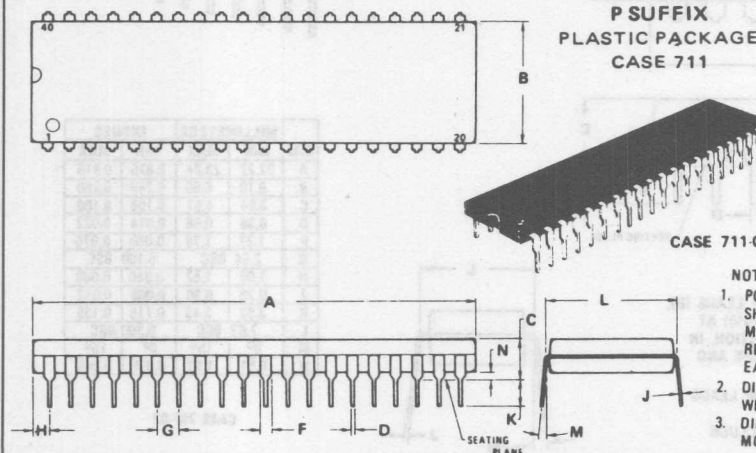


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24	BSC	0.600	BSC
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

**P SUFFIX
PLASTIC PACKAGE
CASE 711**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24	BSC	0.600	BSC
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

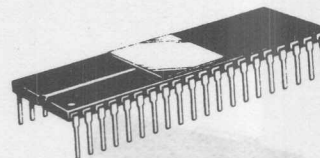
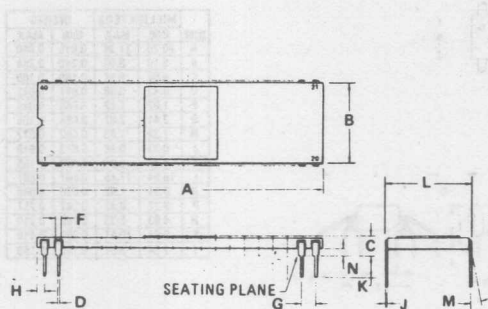
CASE 711-03



NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

**L SUFFIX
CERAMIC PACKAGE
CASE 715**



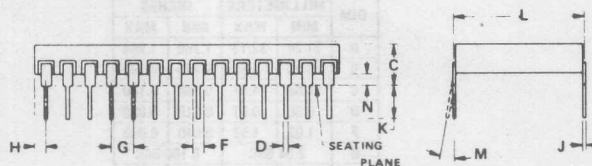
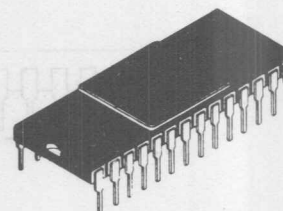
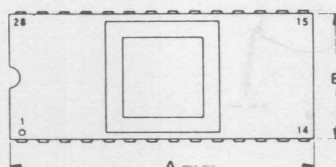
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.94	15.34	0.588	0.604
C	3.05	4.06	0.120	0.160
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	1.02	1.52	0.040	0.060

NOTES:

1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX MAT'L CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 715-03

**L SUFFIX
CERAMIC PACKAGE
CASE 719**



NOTES:

1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIAMETER (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

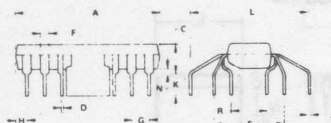
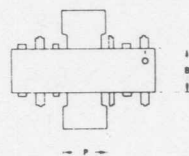
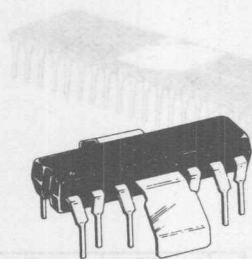
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	35.20	35.92	1.386	1.414
B	14.94	15.34	0.588	0.604
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	1.02	1.52	0.040	0.060

CASE 719-03

CASE 722A

Plastic Package

$R_{\theta JA} = 60^{\circ} \text{ C/W(Typ)}$

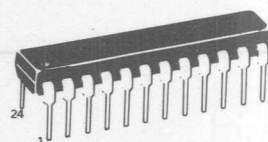
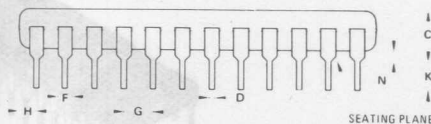
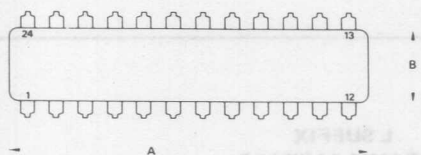


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.43	0.56	0.017	0.022
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.32	1.83	0.052	0.072
J	0.33	0.46	0.013	0.018
K	3.30	3.94	0.130	0.155
L	16.94	17.45	0.667	0.687
N	0.51	1.02	0.020	0.040
P	6.27	6.53	0.247	0.257
R	4.83	5.33	0.190	0.210
S	9.91	10.41	0.390	0.410
T	2.54	3.81	0.100	0.150

CASE 724

Plastic Package

$R_{\theta JA} = 100^{\circ} \text{ C/W(Typ)}$



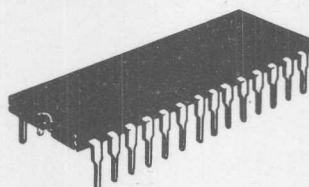
CASE 724 — Plastic package

NOTE:

1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM. "D").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.13	1.260	1.286
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.35	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040

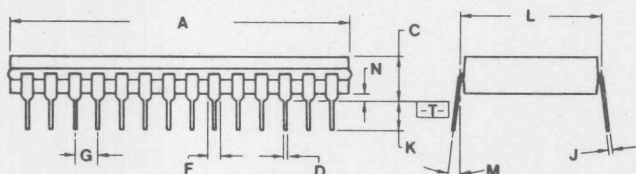
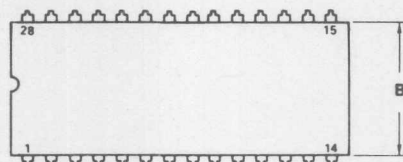
CASE 733-02 Ceramic Package



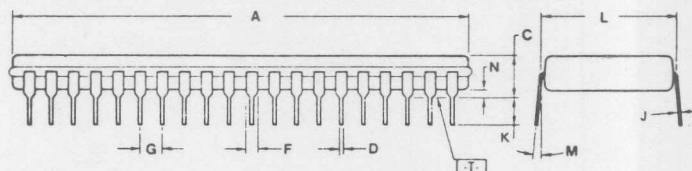
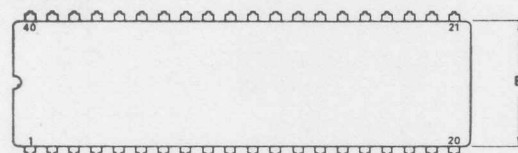
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.85	1.435	1.490
B	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.58	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.06	0.100	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:

1. DIM \bar{A} IS DATUM.
2. POSITIONAL TOL FOR LEADS:
 $\varnothing \pm 0.25 (0.010) \text{ (M) } T \text{ (A) (M)}$
3. \bar{T} IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM \bar{L} TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



S SUFFIX CERDIP PACKAGE CASE 734-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:

1. DIMENSION-A-IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
 $\varnothing \pm 0.25 (0.010) \text{ (M) } T \text{ (A) (M)}$
3. \bar{T} IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSION A AND B INCLUDES MENISCUS.

